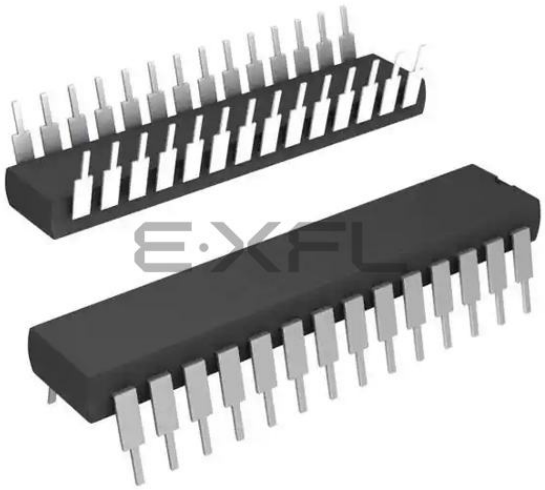
# Analog Devices Inc./Maxim Integrated - ZLF645E0P2864G Datasheet



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## What is "Embedded - Microcontrollers"?

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## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Obsolete |
| Core Processor | Z8 LXMC |
| Core Size | 8-Bit |
| Speed | 8MHz |
| Connectivity | UART/USART |
| Peripherals | Brown-out Detect/Reset, HLVD, POR, WDT |
| Number of I/O | 24 |
| Program Memory Size | 64KB (64K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 1K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.9V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | - |
| Operating Temperature | 0°C ~ 70°C (TA) |
| Mounting Type | Through Hole |
| Package / Case | 28-DIP (0.600", 15.24mm) |
| Supplier Device Package | 28-PDIP |
| Purchase URL | https://www.e-xfl.com/product-detail/analog-devices/zlf645e0p2864g |

## Interrupt Sources

The ZLF645 MCU supports 23 interrupt sources with 6 interrupt vectors, as given below:

- Three external interrupts.
- Two from T8, T16 time-out and capture.
- Three from UART Tx, UART Rx, and UART BRG.
- One from LVD.
- Fourteen from SMR source P20-P27, P30-P33, P00, and P07:
  - Any change in logic from P20-P27, P30-P33 can generate an interrupt or SMR

## Additional Features

The additional features of ZLF645 MCU include:

- IR learning amplifier.
- Low power consumption—11 mW (typical).
- Three standby modes:
  - STOP—1.7 μA (typical)
  - HALT—0.6 mA (typical)
  - Low-voltage reset
- Intelligent counter/timer architecture to automate generation or reception and demodulation of complex waveform, and pulsed signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
  - The UART baud rate generator can be used as another 8-bit timer, when the UART is not in use
- Six priority interrupts:
  - Three external/UART interrupts
  - Two assigned to counter/timers
  - One low-voltage detection interrupt

Figure 3 displays the pin configuration for ZLF645 MCU 20-pin PDIP, SOIC, and SSOP packages.

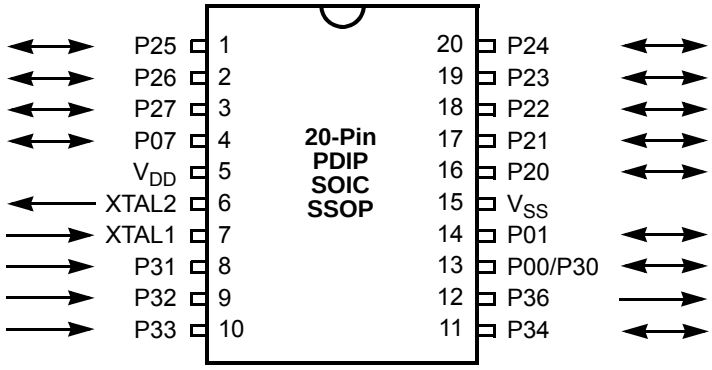


**Figure 3. 20-Pin PDIP/SOIC/SSOP Pin Configuration**

## Port 2

Port 2 is an 8-bit bidirectional CMOS-compatible I/O port. Its eight I/O lines can be independently configured under software control as inputs or outputs. Port 2 is always available for I/O operation. A flash programming option bit is available to connect eight pull-up transistors on this port. Bits programmed as outputs are globally programmed as either push/pull or open-drain. The Power-On Reset function resets with the eight bits of Port 2 [P27:20] configured as inputs.

Port 2 also has an 8-bit input OR and AND gate and edge detection circuitry, which can be used to recover from the STOP mode. P20 can be programmed to access the edge-detection circuitry in DEMODULATION mode. Figure 8 displays the Port 2 configuration.

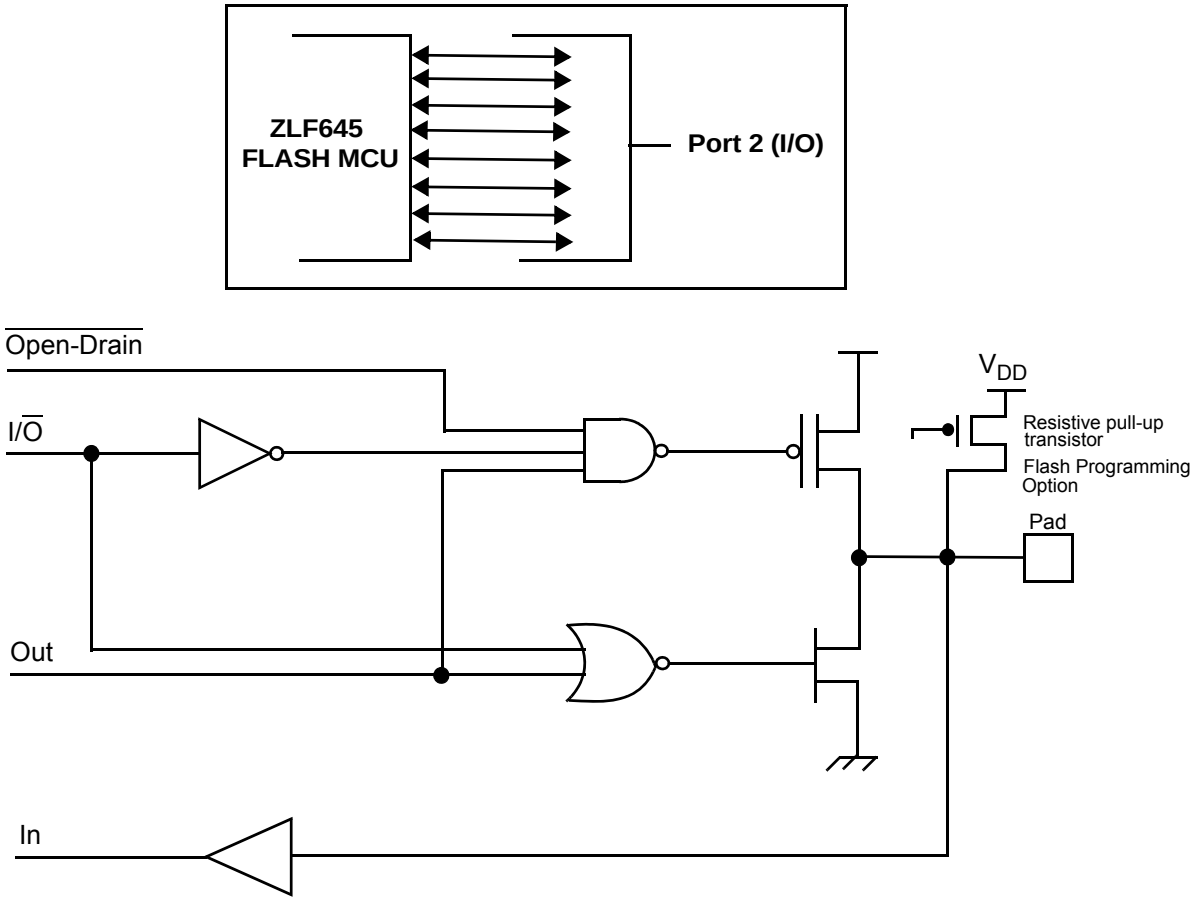


**Figure 8. Port 2 Configuration**

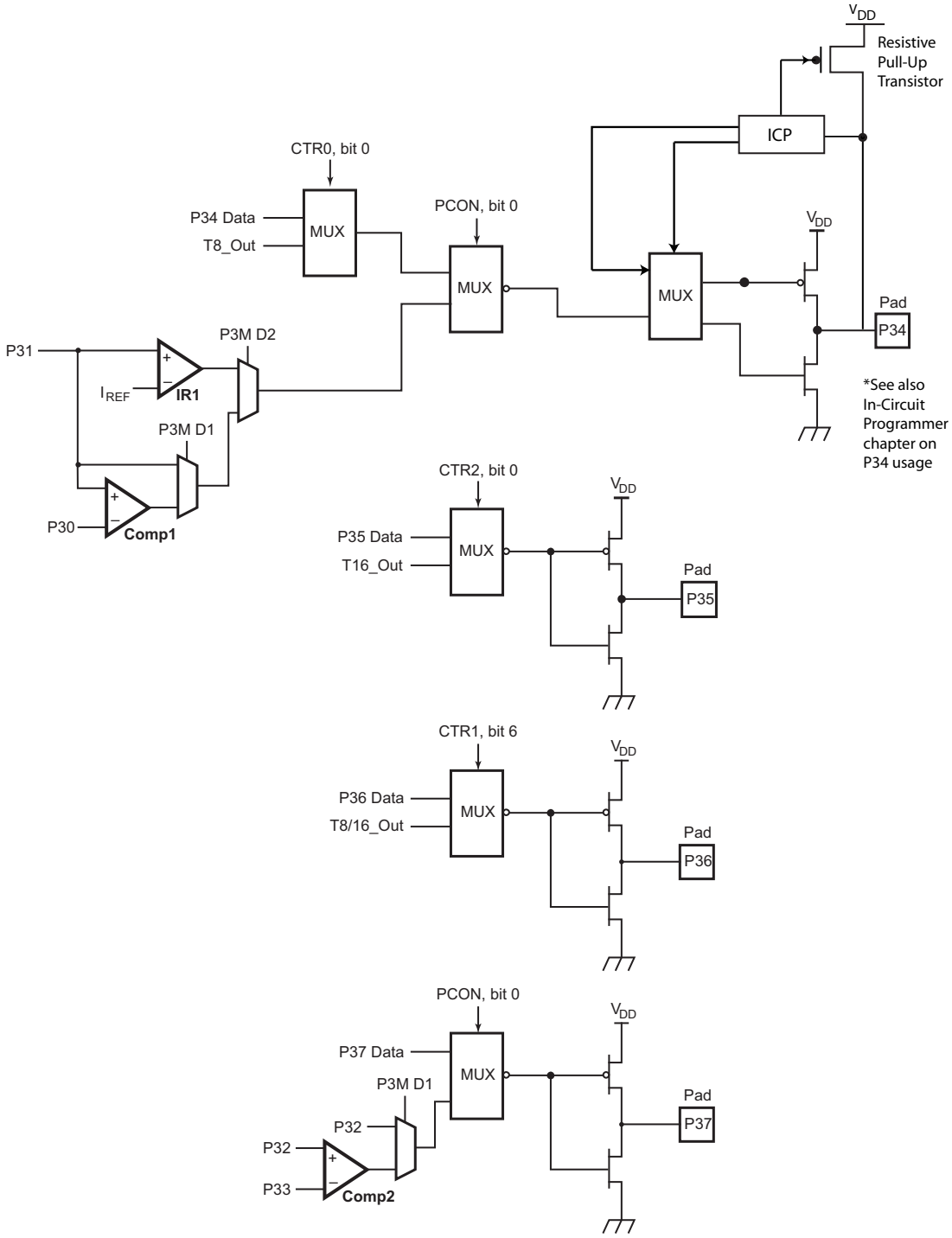


**Figure 10. Port 3 Counter/Timer Output Configuration**

## Port Configuration Register

The Port Configuration register (see Table 13) configures the Port 0 output mode and the comparator output on Port 3. The PCON register is located in expanded register Bank F, address 00h.

**Table 13. Port Configuration Register (PCON)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Reserved | | | | Port 4 Output Mode | Port 0 Output Mode | Port 1 Output Mode | Comp/IR Amp Output Port 3 |
| Reset | X | X | X | X | 1 | 1 | 1 | 0 |
| R/W | — | — | — | — | W | W | W | W |
| Address | Bank F: 00h; Linear: F00h | | | | | | | |

| Bit Position | Value | Description |
|---|---|---|
| [7:4] — | | **Reserved**—Must be written to 1; reads 11111b. |
| [3] | | **Port 4 Output Mode**—Controls the output mode of Port 4. |
| | 0 | Open-drain |
| | 1 | Push/pull |
| [2] | | **Port 0 Output Mode**—Controls the output mode of Port 0.<br>Write only; read returns 1. |
| | 0 | Open-drain |
| | 1 | Push/pull |
| [1] | | **Port 1 Output Mode**—Controls the output mode of Port 1.<br>Write only; read returns 1 |
| | 0 | Open-drain |
| | 1 | Push/pull |
| [0] | | **Comparator or IR Amplifier Output Port 3**—Select digital outputs or comparator, and IR amplifier outputs on P34 and P37.<br>Write only; read returns 1. |
| | 0 | P34 and P37 outputs are digital. |
| | 1 | P34 is Comparator 1 or IR Amplifier output, P37 is Comparator 2 output. |

**Note:** *PCON register is not reset after a Stop Mode Recovery. Also, for package types other than the 48-pin package, writes to bit 3 and bit 1 have no effect.*

# Register File Summary

Table 26 lists each linear (12-bit) register file address to the associated register, mnemonic, and reset value. The table also lists the register bank (or banks) and corresponding 8-bit address (if any) for each register and a page link to the detailed register table.

Throughout this document, an 'X' denotes an undefined digit. A '—' (dash) in a table cell indicates that the corresponding attribute does not apply to the listed item. Reset value digits (highlighted in grey) are not reset by a Stop Mode Recovery. Register bit SMR[7] (shown in **boldface**) is set to 1 instead of reset by a Stop Mode recovery.

**Table 26. Register File Address Summary**

| Address (Hex) | | | | | | |
|---|---|---|---|---|---|---|
| **12-Bit** | **Bank** | **8-Bit** | **Register Description** | **Mnemonic** | **Reset** | **Page No** |
| 000 | 0–3 | 00 | Port 0 Register | P0 | XXh | 32 |
| 001 | 0–3 | 01 | Port 1 Register | P1 | XXh | 33 |
| 002 | 0–3 | 02 | Port 2 Register | P2 | XXh | 35 |
| 003 | 0–3 | 03 | Port 3 Register | P3 | 0Xh | 37 |
| 004 | 0–3 | 04 | Port 4 Register | P4 | XXh | 37 |
| 005–00F | 0 | 05–0F | General-Purpose Registers (Bank 0 Only) | — | XXh | — |
| 010–0EF | 0,D,F | 10–EF | General-Purpose Registers (Banks 0, D, F) | — | XXh | — |
| 0F0 | All | F0 | Reserved | — | — | — |
| 0F1 | All | F1 | UART Receive/Transmit Data Register | URDATA/ UTDATA | XXh | 95 |
| 0F2 | All | F2 | UART Status Register | UST | 0000_0010b | 95 |
| 0F3 | All | F3 | UART Control Register | UCTL | 00h | 97 |
| 0F4 | All | F4 | UART Baud Rate Generator Constant Register | BCNST | FFh | 98 |
| 0F5 | All | F5 | Reserved | — | — | — |
| 0F6 | All | F6 | Port 2 Mode Register | P2M | FFh | 34 |
| 0F7 | All | F7 | Port 3 Mode Register | P3M | XXXX_X000b | 36 |
| 0F8 | All | F8 | Port 0/1 Mode Register | P01M | X1XX_1XX1b | 31 |

This command when executed returns a value of 0132H which is the revision ID assigned for the ZLF645 MCU.

- **Read ICP Status Register (02H)**—The Read ICP Status register command reads the ICPSTAT register.

```
ICP ← 02H
ICP → ICPSTAT[7:0]
```

- **Write ICP Control Register (04H)**—The Write ICP Control register command writes the data that follows the command to the ICPCTL register.

```
ICP ← 04H
ICP ← ICPCTL[7:0]
```

- **Read ICP Control Register (05H)**—The Read ICP Control register command reads the value of the ICPCTL register.

```
ICP ← 05H
ICP → ICPCTL[7:0]
```

- **Write Flash Controller Registers (08H)**—The Write Flash Controller register command allows writes to the Flash Controller registers. This command configures the Flash Controller for Flash memory accesses through the `Write Flash Memory` and `Read Flash Memory` commands. If the device is not in FLASH CONTROL mode, the register address and data values are discarded.

```
ICP ← 08H
ICP ← Register Address[15:0] ("0FH" for all Flash Ctrl Regs)
ICP ← Register Address[7:0]
ICP ← Size[7:0]
ICP ← 1-256 data bytes
```

- **Read Flash Controller Registers (09H)**—The Read Flash Controller command allows reads of the Flash Controller registers. If the device is not in FLASH CONTROL mode this command returns `FFH` for all the register values.

```
ICP ← 09H
ICP ← Register Address[15:0] ("0FH" for all Flash Ctrl Regs)
ICP ← Register Address[7:0]
ICP ← Size[7:0]
ICP → 1-256 data bytes
```

- **Write Flash Memory (0AH)**—The Write Flash Memory command is used to write data to the main memory area or Information Area of the Flash memory. The command has equivalent functionality to the CPU writing the memory through the LDC and LDCI instructions. Data can be written 1 to `memsize` bytes at a time where `memsize` represents the size (32 KB or 64 KB) of the Flash memory for the product option chosen (The `memsize` number of bytes can be written by setting the size to 0). Should a size value greater than the maximum memory size be given by the user, the actual size value

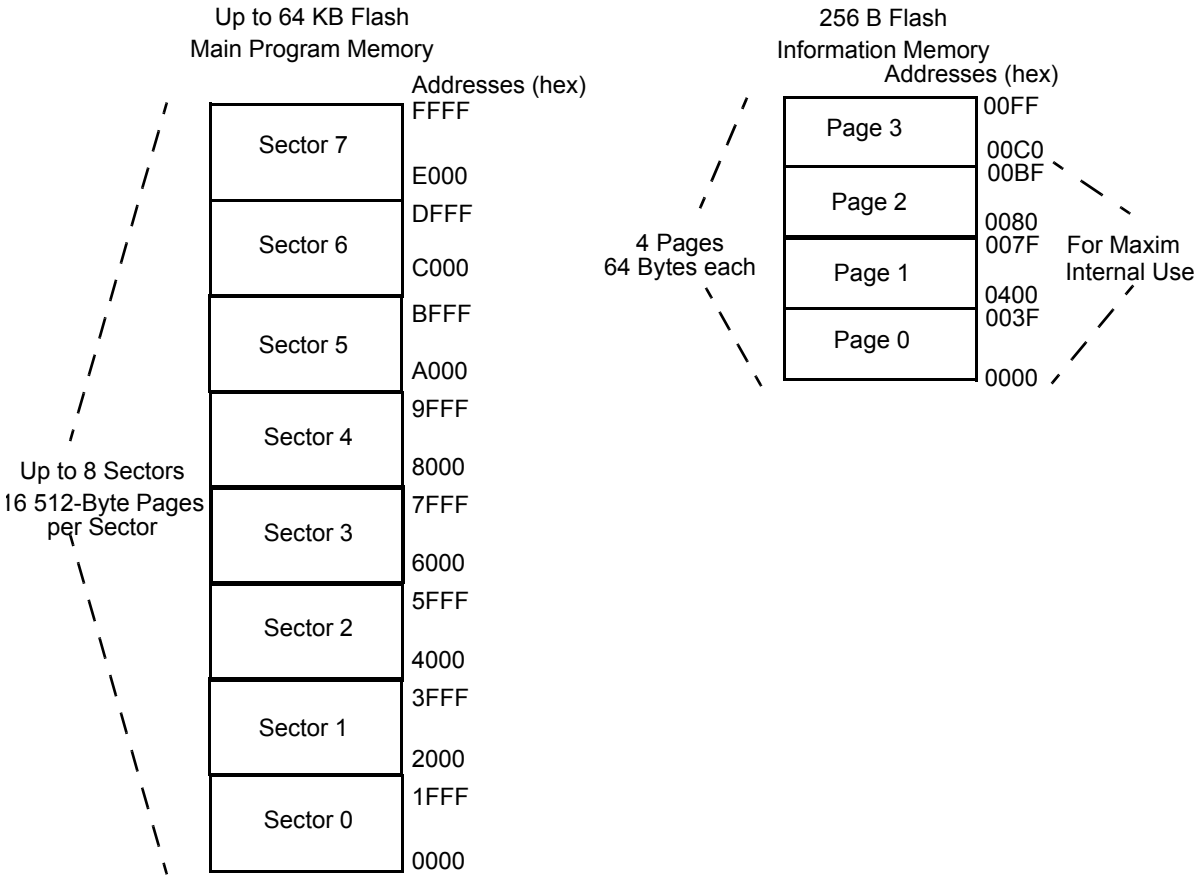


**Figure 19. Flash Memory Arrangement**

## Flash Information Block

The Flash Information Block of Flash memory is divided into two sections. Page 3 of the Information Block is accessible by you or Flash programmer vendor for programming, reading, or erasure through the ZLF645's ICP interface or it's Flash Byte Programming Interface only, as described in the section Flash Byte Programming Interface on page 82. The CPU has no access to this area of memory. User Option Bytes 0 and 1 use addresses `00FE` and `00FF` respectively of the Page 3 area and contain programmable bits with pre-defined functions.

The Flash read/write protect bits in User Option Byte 1 control the level of Page 3 access allowed to you along with the User's level of access to the Flash's main memory. Bytes `00C0` through `00FD` of Page 3 have no pre-defined function and are available to you for other operations.

## UART Receive Data Register/UART Transmit Data Register

The UART Receive/Transmit Data register (see Table 43) is used to send and retrieve data from the UART channel. When the UART receives a data byte, it can be read from this register. The UART receive interrupt is cleared when this register is used. Data written to this register is transmitted by the UART.

**Table 43. UART Receive/Transmit Data Register (URDATA/UTDATA)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | UART Receive/Transmit | | | | | | | |
| Reset | X | X | X | X | X | X | X | X |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Bank Independent: F1h; Linear: 0F1h | | | | | | | |

| Bit Position | Description |
|---|---|
| [7:0] | **UART Receive/Transmit**<br>When read, returns received data.<br>When written, transmits written data. |

## UART Status Register

The UART Status register (see Table 44) displays the status of the UART. Bits [6:3] are cleared by reading the UART Receive/Transmit register (F1h).

**Table 44. UART Status Register (UST)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Receive Status | Parity Error | Overrun Error | Framing Error | Break | Transmit Data | Transmit Complete | Noise Filter |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Bank Independent: F2h; Linear: 0F2h | | | | | | | |

| Bit Position | Value | Description |
|---|---|---|
| [7] | | **Receive Status**—Set when data is received; cleared when URDATA is read. |
| | 0 | UART Receive Data register empty. |
| | 1 | UART Receive Data register full. |

Table 47 summarizes the timer control registers. Some timer functions can also be affected by control registers for other peripheral functions.

**Table 47. Timer Control Registers**

| Address (Hex) | | | | | | |
|---|---|---|---|---|---|---|
| 12-Bit | Bank | 8-Bit | Register Description | Mnemonic | Reset | Page No |
| D00 | D | 00 | Counter/Timer 8 Control Register | CTR0 | 0000_0000b | 119 |
| D01 | D | 01 | Timer 8 and Timer 16 Common Functions | CTR1 | 0000_0000b | 121 |
| D02 | D | 02 | Counter/Timer 16 Control Register | CTR2 | 0000_0000b | 124 |
| D03 | D | 03 | Timer 8/Timer 16 Control Register | CTR3 | 0000_0XXXb | 126 |
| D04 | D | 04 | Counter/Timer 8 Low Hold Register | TC8L | 00h | 118 |
| D05 | D | 05 | Counter/Timer 8 High Hold Register | TC8H | 00h | 117 |
| D06 | D | 06 | Counter/Timer 16 Low Hold Register | TC16L | 00h | 117 |
| D07 | D | 07 | Counter/Timer 16 High Hold Register | TC16H | 00h | 116 |
| D08 | D | 08 | Timer 16 Capture Low Register | LO16 | 00h | 116 |
| D09 | D | 09 | Timer 16 Capture High Register | HI16 | 00h | 115 |
| D0A | D | 0A | Timer 8 Capture Low Register | LO8 | 00h | 115 |
| D0B | D | 0B | Timer 8 Capture High Register | HI8 | 00h | 114 |

# Counter/Timer Functional Blocks

The ZLF645 MCU infrared timer contains a glitch filter for removing noise from the input when demodulating an input carrier. Each timer features its own demodulating mode and can be simultaneously used to generate a signal output. The T8 timer has the ability to capture only one cycle of a carrier wave of a high-frequency waveform.

## Input Circuit

Depending on the setting of register bits P3M[2:1] and CTR1[6], the timer/counter input circuit monitors one of the following conditions:

- The P31 digital signal, if CTR1[6]=0 and P3M[2:1]=00.
- The P31 analog comparator output, if CTR1[6]=0 and P3M[2:1]=01.
- The P31 IR amplifier output, if CTR1[6]=0 and P3M[2]=1.
- The P20 digital signal, if CTR1[6]=1.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, bit 1). If the initial value (CTR1, bit 1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter.

In SINGLE-PASS mode (CTR0, bit 6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, bit 5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, bit 1).

In MODULO-N mode, on reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, bit 5), thereby generating an interrupt if enabled (CTR0, bit 1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 29.

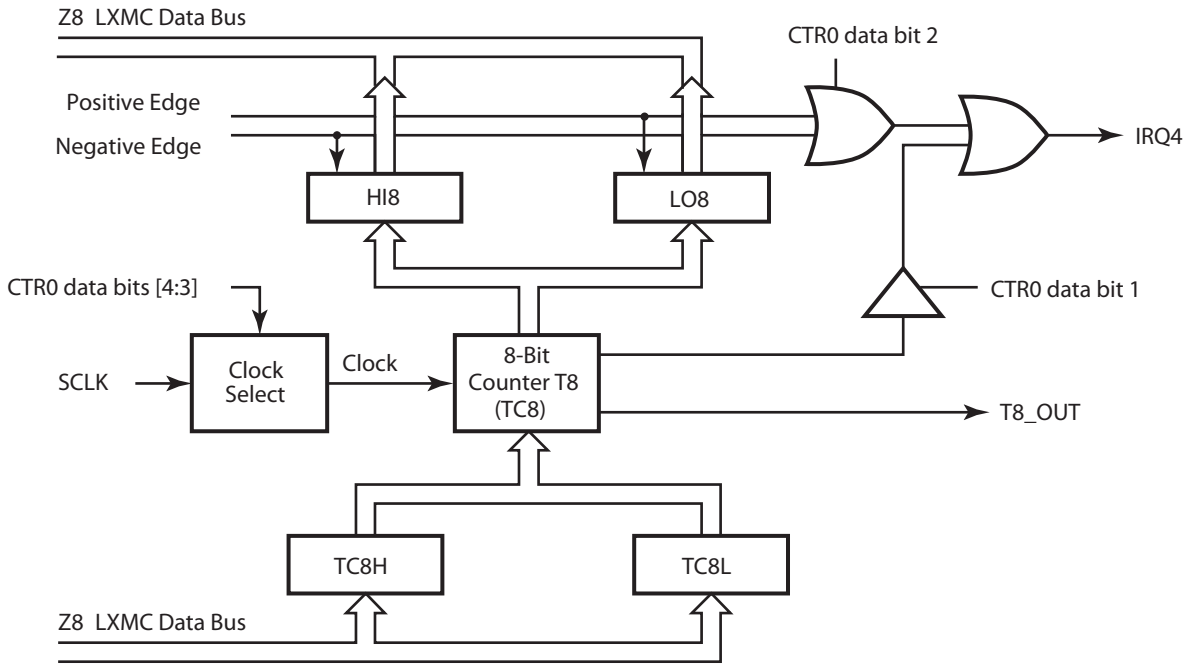


**Figure 29. 8-Bit Counter/Timer Circuits**

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

**Caution:** *An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFh to FEh.*

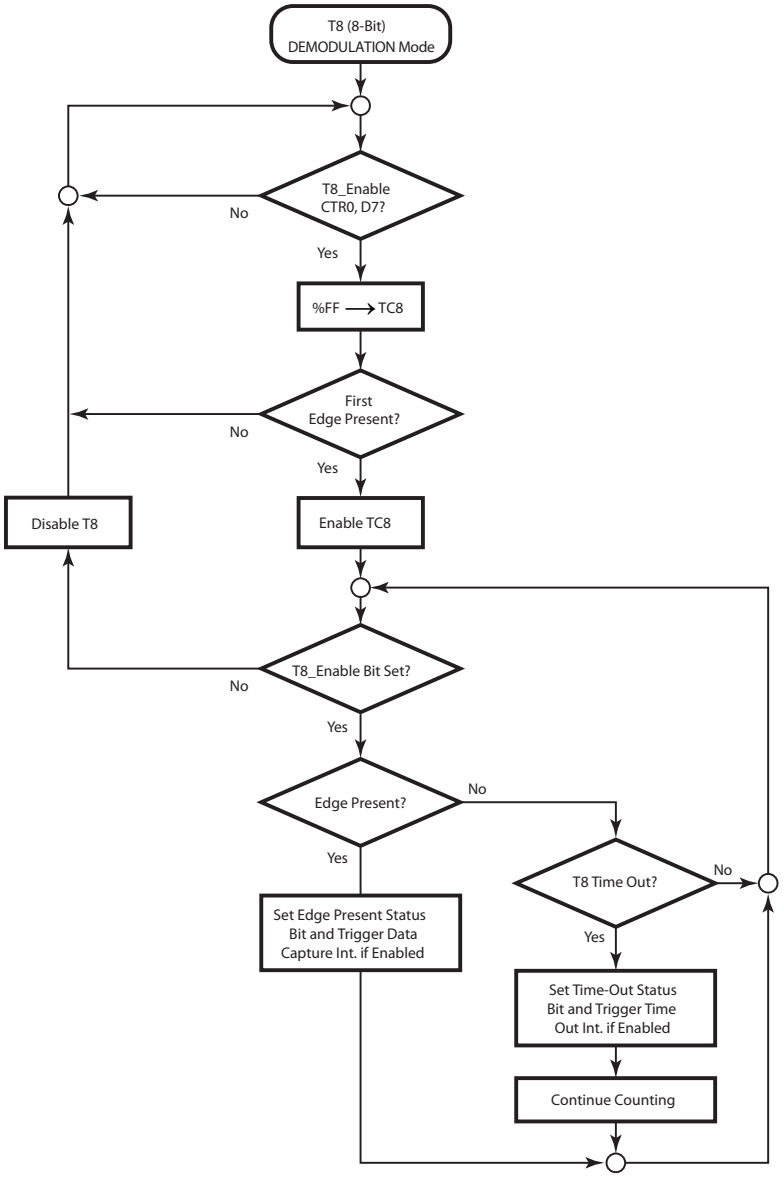


**Figure 33. DEMODULATION Mode Flowchart**

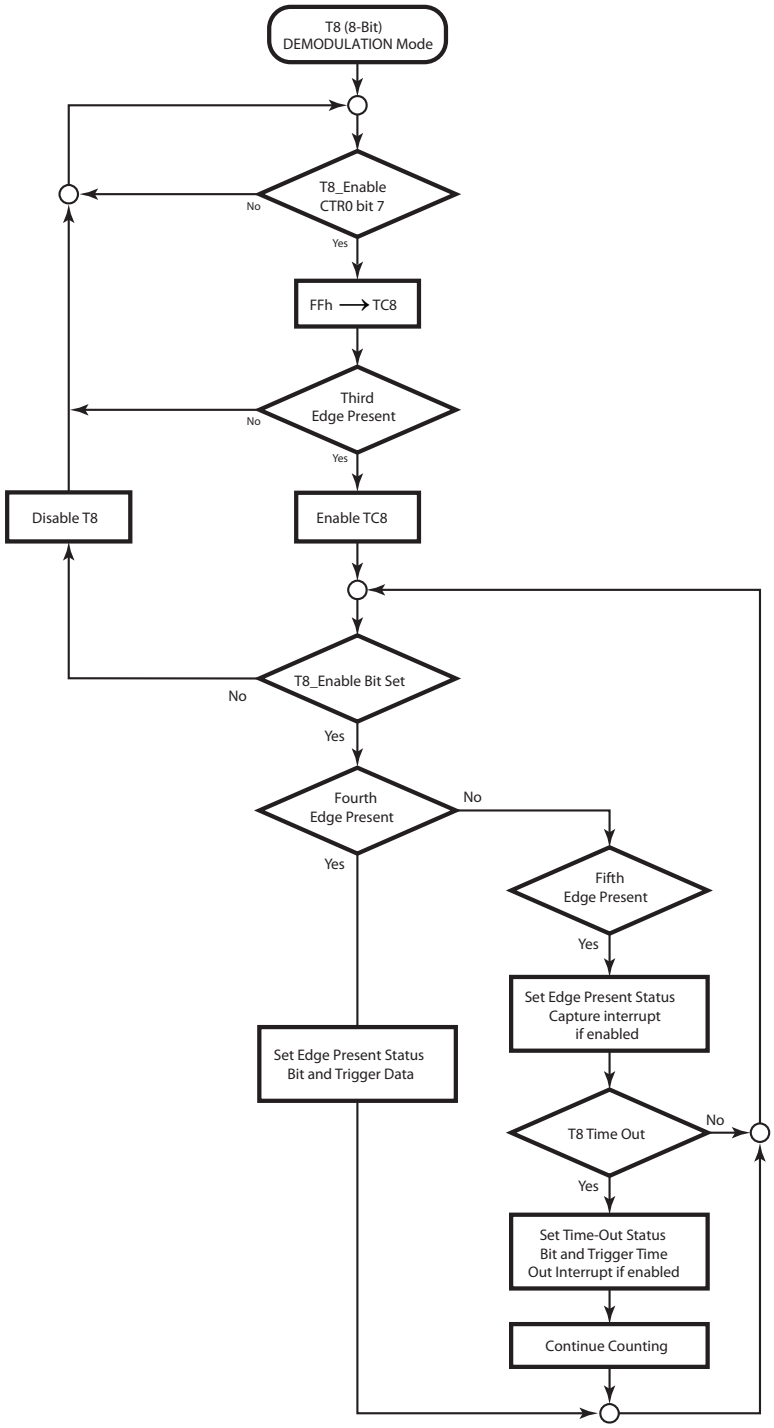


**Figure 34. DEMODULATION Mode Flowchart with Bit 4 of CTR3 Set**

## Counter/Timer 16 Low Hold Register

The Counter/Timer 16 Low Hold register (see Table 53) contains the low byte of the value loaded into the T16 timer.

**Note:** *This register is not reset after a Stop Mode Recovery.*

**Table 53. Counter/Timer 16 Low Hold Register (TC16L)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | T16_Data_LO | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Bank D: 06h; Linear: D06h | | | | | | | |

| Bit Position | Value | Description |
|---|---|---|
| [7:0] | 0hh–FFh | **T16_Data_LO**—Read/Write Data. |

## Counter/Timer 8 High Hold Register

The Counter/Timer 8 High Hold register (see Table 54) contains the value to be counted while the T8 output is 1.

**Note:** *This register is not reset after a Stop Mode Recovery.*

**Table 54. Counter/Timer 8 High Hold Register (TC8H)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | T8_Level_HI | | | | | | | |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Bank D: 05h; Linear: D05h | | | | | | | |

| Bit Position | Value | Description |
|---|---|---|
| [7:0] | 0hh–FFh | **T8_Level_HI**—Read/Write Data. |

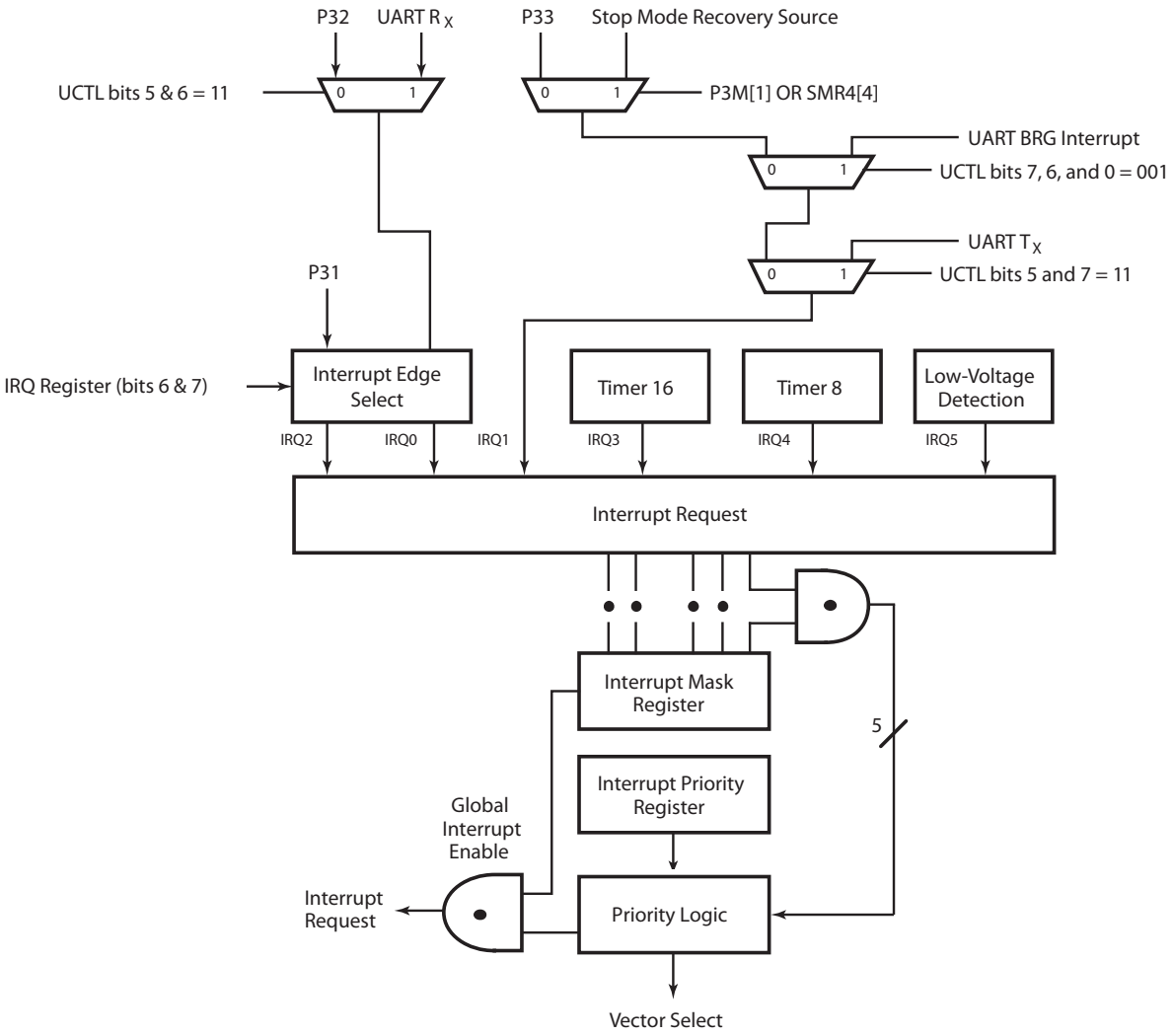


**Figure 40. Interrupt Block Diagram**

| Bit Position | Value | Description |
|---|---|---|
| {[4:3], [0]} | | **Group Priority** |
| | 000 | Reserved |
| | 001 | C > A > B |
| | 010 | A > B > C |
| | 011 | A > C > B |
| | 100 | B > C > A |
| | 101 | C > B > A |
| | 110 | B > A > C |
| | 111 | Reserved |
| [2] | | **Group B Priority (IRQ0, IRQ2)** |
| | 0 | IRQ2 > IRQ0 |
| | 1 | IRQ0 > IRQ2 |
| [1] | | **Group C Priority (IRQ1, IRQ4)** |
| | 0 | IRQ1 > IRQ4 |
| | 1 | IRQ4 > IRQ1 |

## Interrupt Request Register

Bit 7 and Bit 6 of the Interrupt Request register (see Table 64) are used to configure the edge detection of the interrupts for Port 3, bit 1 and Port 3, bit 2. The remaining bits (5 through 0) indicate the status of the interrupt. When an interrupt is serviced, the hardware automatically clears the bit to 0. Writing 1 to any of these bits generates an interrupt if the appropriate bits in the Interrupt Mask register are enabled. Writing 0 to these bits clears the interrupts.

**Table 64. Interrupt Request Register (IRQ)**

| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| Field | Interrupt Edge | | IRQ5 | IRQ4 | IRQ3 | IRQ2 | IRQ1 | IRQ0 |
| Reset | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W | R/W |
| Address | Bank Independent: FAh; Linear: 0FAh | | | | | | | |

| Bit Position | Value | Description |
|---|---|---|
| [7:6] | | **Interrupt Edge** |
| | 00 | P31↓ P32↓ |
| | 01 | P31↓ P32↑ |
| | 10 | P31↑ P32↓ |
| | 11 | P31↑↓ P32↑↓ |

# Reset and Power Management

The ZLF645 MCU provides the following reduced-power modes, power monitoring, and reset features:

- **Voltage Brownout Standby**—Stops the oscillator and internal clock when the power level drops below the VBO low voltage detect point. Initiates a power-on reset when power is restored above the VBO detect point.
- **STOP Mode**—Stops the clock and oscillator, reduces the MCU supply current to a very low level until a power-on reset or Stop Mode Recovery occurs.
- **HALT Mode**—Stops the internal clock to the CPU until an enabled interrupt request is received.
- **Voltage Detection**—Optionally sets a flag if a low- or high-voltage condition occurs. The low-voltage detection flag can generate an interrupt request, if enabled.
- **Power-On Reset**—Starts the oscillator and internal clock, and initializes the system to its power-on reset defaults.
- **Watchdog Timer**—Optionally generates a Power-On Reset if the program fails to execute the WDT instruction within a specified time interval.
- **Stop Mode Recovery**—Restarts the oscillator and internal clock, and initializes most of the system to its power-on reset defaults. Some register values are not reset by a Stop Mode Recovery.

**Note:** *For supply current values under various conditions, see* DC Characteristics *on page 165.*

Figure 43 on page 138 displays the Power-On Reset sources. Table 66 lists control registers for reset and power management features. Some features are affected by registers described in other chapters.

**Table 66. Reset and Power Management Registers**

| Address (Hex) | | | | | | |
|---|---|---|---|---|---|---|
| 12-Bit | Bank | 8-Bit | Register Description | Mnemonic | Reset | Page No |
| D0C | D | 0C | Low-Voltage Detection Register | LVD | 1111_1000b | 140 |
| F0A | F | 0A | Stop Mode Recovery Register 4 | SMR4 | XXX0_0000b | 156 |
| F0B | F | 0B | Stop Mode Recovery Register | SMR | 0010_0000b | 146 |
| F0C | F | 0C | Stop Mode Recovery Register 1 | SMR1 | 00h | 150 |
| F0D | F | 0D | Stop Mode Recovery Register 2 | SMR2 | X0X0_00XXb | 152 |

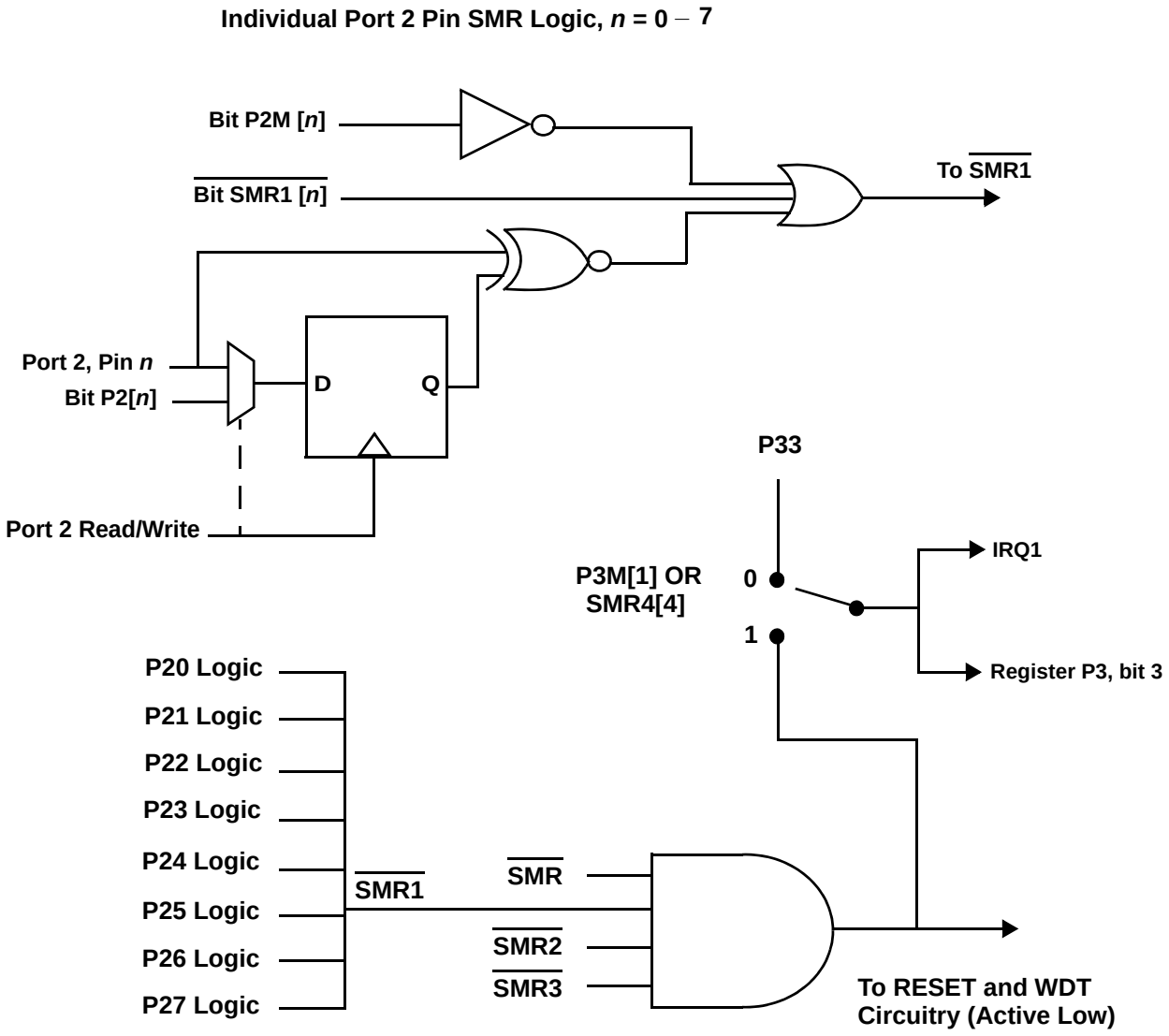


**Figure 45. SMR1 Register-Controlled Event Sources**

**Table 81. Clock, Reset, Timers, and SMR Timing (Continued)**

| No | Symbol | Parameter | $V_{CC}$ | $T_A$ = 0 °C to +70 °C 8.0 MHz Min | $T_A$ = 0 °C to +70 °C 8.0 MHz Max | Units | WDTMR (Bits 6, 5, 4, 1, 0) |
|---|---|---|---|---|---|---|---|
| 13 | $T_{POR}$ | Power-on reset | 1.9–3.6 | 2.5 | $10^5$ | ms | — |
| 14 | $f_{iramp}$ | Frequency of input signal for IR amplifier | — | 0 | 500 | kHz | — |

**Notes**
1. Timing Reference uses 0.9 $V_{CC}$ for a logic 1 and 0.1 $V_{CC}$ for a logic 0.
2. Interrupt request through Port 3 (P33:P31).
3. SMR – bit 5 = 1.
4. SMR – bit 5 = 0.
5. If bit 1 of the SMR register is programmed to 1, this value is 2.5 ms as measured from the time the oscillator input to XTAL1 reaches a peak to peak voltage oscillation of at least 300 mV.

**Table 82. Flash Memory Electrical Characteristics and Timing**

| No | Symbol | Parameter | $T_A$ = 0 °C to +70 °C 8.0 MHz Min | $T_A$ = 0 °C to +70 °C 8.0 MHz Max | Units | Condition |
|---|---|---|---|---|---|---|
| 1 | $I_{FLP}$ | Flash Memory Programming Current | — | 10 | mA | — |
| 2 | $I_{FLE}$ | Flash Memory Page/Mass Erase Current | — | 6 | mA | — |
| 3 | $I_{RD}$ | Flash Dynamic Read Current | — | 420 | a | Assumes reads every clock cycle with a 1 MHz clock |
| 4 | $V_{FLPE}$ | Flash Memory Program/ Erase Voltage | 2.3 | 3.6 | V | — |
| 5 | $V_{FLR}$ | Flash Memory Read Voltage | 1.8 | 3.6 | V | — |
| 6 | $T_{PROG}$ | Flash Programming Time | 30 | 60 | us | — |
| 7 | Tpe | Flash Page Erase Time | 10 | — | ms | — |
| 8 | Tme | Flash Mass Erase Time | 10 | — | ms | — |
| 9 | Tdr | Flash Data Retention Time | 10 | — | years | Temp=25 °C |
| 10 | Fen | Flash Program/Erase Endurance | 20,000 | — | cycles | — |

## D



## E



## F



## H



## I