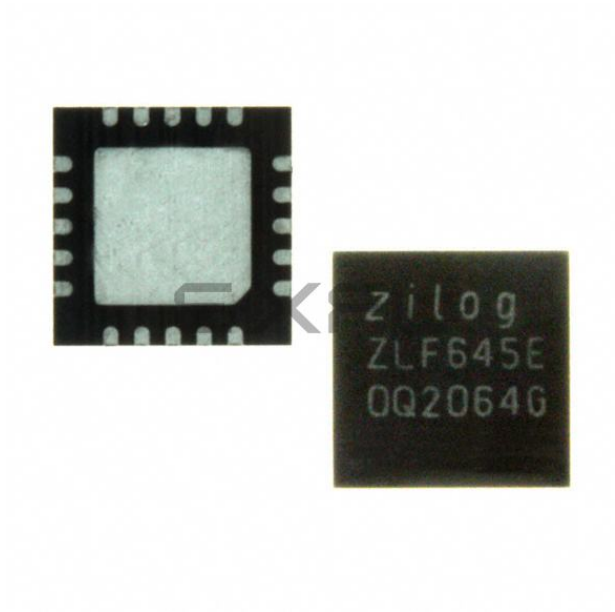
Analog Devices Inc./Maxim Integrated - ZLF645E0Q2064G Datasheet



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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8 LXMC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	16
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 3.6V
Data Converters	-
Oscillator Type	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	20-VQFN Exposed Pad
Supplier Device Package	20-QFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlf645e0q2064g

Architectural Overview

Maxim's ZLF645 Series of Flash MCU's are members of the Crimzon® family of infrared microcontrollers. This series provides a directly-compatible code upgrade path to other Crimzon MCUs, offers a robust learning function, and features up to 64 KB Flash memory and 1K general-purpose Random Access Memory (RAM). Two timers allow the generation of complex signals while performing other counting operations.

A Universal Asynchronous Receiver/Transmitter (UART) allows the ZLF645 MCU to function as a slave/master database chip. When the UART is not in use, the Baud Rate Generator (BRG) can be used as a third timer. Enhanced Stop Mode Recovery features allow the ZLF645 MCU to recover from STOP mode on any change of logic and on any combination of the 12 SMR inputs. The SMR source can also be used as an interrupt source.

Many high-end remote control units offer a learning function. A learning function allows a replacement remote unit to learn infrared signals from the original remote unit and regenerate the signal. However, the amplifying circuits of many learning remotes are expensive and are not tuned well. The ZLF645 MCU is the first chip to offer a built-in tuned amplification circuit in a wide range of positions and battery voltages. The only external component required is a photodiode.

The ZLF645 MCU greatly reduces the system cost and improves learning function reliability. With all new features, the ZLF645 MCU is excellent for infrared remote control and other MCU applications.

Features

Table 1 lists the memory, I/O, and power features of the ZLF645 Flash MCU. Additional features are listed below the table.

Table 1. ZLF645 Flash MCU Features

Device	Flash (KB)	RAM*	I/O Lines	Voltage Range
ZLF645 Flash MCU	32 or 64	512 B or 1 K	16, 24, or 40	2.0 V–3.6 V

*General-purpose registers implemented as RAM.

Interrupt Sources

The ZLF645 MCU supports 23 interrupt sources with 6 interrupt vectors, as given below:

- Three external interrupts.
- Two from T8, T16 time-out and capture.
- Three from UART Tx, UART Rx, and UART BRG.
- One from LVD.
- Fourteen from SMR source P20-P27, P30-P33, P00, and P07:
  - Any change in logic from P20-P27, P30-P33 can generate an interrupt or SMR

Additional Features

The additional features of ZLF645 MCU include:

- IR learning amplifier.
- Low power consumption—11 mW (typical).
- Three standby modes:
  - STOP—1.7 μA (typical)
  - HALT—0.6 mA (typical)
  - Low-voltage reset
- Intelligent counter/timer architecture to automate generation or reception and demodulation of complex waveform, and pulsed signals:
  - One programmable 8-bit counter/timer with two capture registers and two load registers
  - One programmable 16-bit counter/timer with one 16-bit capture register pair and one 16-bit load register pair
  - Programmable input glitch filter for pulse reception
  - The UART baud rate generator can be used as another 8-bit timer, when the UART is not in use
- Six priority interrupts:
  - Three external/UART interrupts
  - Two assigned to counter/timers
  - One low-voltage detection interrupt

Table 5 lists the function and signal directions of each pin within the 20-pin PDIP, SOIC, and SSOP packages sequentially by pin number.

Table 5. 20-Pin PDIP/SOIC/SSOP Sequential Pin Identification

Pin No	Symbol	Function	Signal Direction
1	P25	Port 2, bit 5	Input/Output
2	P26	Port 2, bit 6	Input/Output
3	P27	Port 2, bit 7	Input/Output
4	P07	Port 0, bit 7	Input/Output
5	V_{DD}	Power Supply	Input
6	XTAL2	Crystal oscillator	Output
7	XTAL1	Crystal oscillator	Input
8	P31	Port 3, bit 1	Input
9	P32	Port 3, bit 2	Input
10	P33	Port 3, bit 3	Input
11	P34	Port 3, bit 4	Input/Output
12	P36	Port 3, bit 6	Output
13	P00	Port 0, bit 0	Input/Output
	P30	Port 3, bit 0	Input
14	P01	Port 0, bit 1	Input/Output
15	V_{SS}	Ground In	put
16	P20	Port 2, bit 0	Input/Output
17	P21	Port 2, bit 1	Input/Output
18	P22	Port 2, bit 2	Input/Output
19	P23	Port 2, bit 3	Input/Output
20	P24	Port 2, bit 4	Input/Output

Note: When the Port 0 low-nibble pull-up option is enabled and the P30 input is Low, current flows through the pull-up to Ground.

Port 2 Mode Register

The Port 2 Mode register (see Table 17) determines the I/O direction of each bit on Port 2. Bit 0 of the Port 3 Mode register determines whether the output drive is push/pull or open-drain.

Table 17. Port 2 Mode Register (P2M)

Bit	7	6	5	4	3	2	1	0
Field	P27 I/O Definition	P26 I/O Definition	P25 I/O Definition	P24 I/O Definition	P23 I/O Definition	P22 I/O Definition	P21 I/O Definition	P20 I/O Definition
Reset	1	1	1	1	1	1	1	1
R/W	W	W	W	W	W	W	W	W
Address	Bank Independent: F6h; Linear: 0F6h							

Bit Position	Value	Description
[7]	0 1	Defines P27 as output. Defines P27 as input.
[6]	0 1	Defines P26 as output. Defines P26 as input.
[5]	0 1	Defines P25 as output. Defines P25 as input.
[4]	0 1	Defines P24 as output. Defines P24 as input.
[3]	0 1	Defines P23 as output. Defines P23 as input.
[2]	0 1	Defines P22 as output. Defines P22 as input.
[1]	0 1	Defines P21 as output. Defines P21 as input.
[0]	0 1	Defines P20 as output. Defines P20 as input.

Note: *Port 2 Mode register is not reset after a Stop Mode Recovery.*

Port 4 Mode Register

The Port 4 Mode register (see Table 21) determines the I/O direction of each bit on Port 4. Bit 3 of the Port Configuration register (PCON) determines whether the output drive is push/pull or open-drain.

Table 21. Port 4 Mode Register (P4M)

Bit	7	6	5	4	3	2	1	0
Field	P47 I/O Definition	P46 I/O Definition	P45 I/O Definition	P44 I/O Definition	P43 I/O Definition	P42 I/O Definition	P41 I/O Definition	P40 I/O Definition
Reset	1	1	1	1	1	1	1	1
R/W	W	W	W	W	W	W	W	W
Address	Bank F: 09h; Linear: F09h							

Bit Position	Value	Description
[7]	0 1	Defines P47 as output. Defines P47 as input.
[6]	0 1	Defines P46 as output. Defines P46 as input.
[5]	0 1	Defines P45 as output. Defines P45 as input.
[4]	0 1	Defines P44 as output. Defines P44 as input.
[3]	0 1	Defines P43 as output. Defines P43 as input.
[2]	0 1	Defines P42 as output. Defines P42 as input.
[1]	0 1	Defines P41 as output. Defines P41 as input.
[0]	0 1	Defines P40 as output. Defines P40 as input.

Note: *Port 4 Mode register is not reset after a Stop Mode Recovery.*

Memory and Registers

The Z8® LXMC CPU used in the ZLF645 Series of Flash MCUs incorporates special features to extend the available memory space while maintaining the benefits of a Z8® CPU core in battery-operated applications.

Flash Program/Constant Memory

The ZLF645 Series of Flash MCUs can address up to 64 KB of Flash memory for object code (program instructions and immediate data) and constant data (ROM tables and data constants). The first 12 bytes of the memory are reserved for the six available 16-bit interrupt request (IRQ) vectors. On reset, program execution begins at address 000Ch in the memory. Execution rolls over to the beginning of the memory if the program counter address exceeds the Flash memory size.

The entire Flash memory is available for either program code or constant data. Outside of normal instruction fetches, the CPU can access the Flash memory by using LDC and LDCI instructions. The LDC and LDCI instructions use 16-bit addresses to access the memory. Figure 12 displays the Program/Constant memory map for the device.

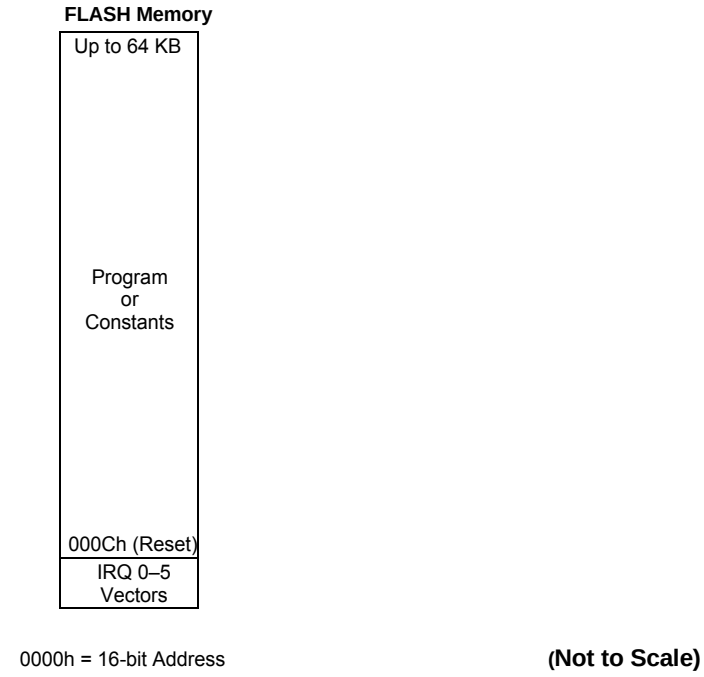


Figure 12. Program/Constant Memory Map

Table 28. In-Circuit Programmer Commands (Continued)

ICP Command	Command Byte	Enabled when NOT in FLASH CONTROL mode?	Disabled by Flash Read/Write Protect Option Bits (FLRWP and/or FLPROT1)
Read Flash Controller Registers	09H	No	—
Write Flash Memory	0AH	No	If FLRWP enabled, command is disabled for entire Flash main memory and page 3 of the Information Area. If FLPROT1 enabled, command disabled for page 3 of the Information Area and lower half of main memory only.
Read Flash Memory	0BH	No	If FLRWP enabled, command is disabled for the Flash main memory. If FLPROT1 enabled, command disabled for the lower half of main memory only.
Reserved	0CH – 0DH	—	Disabled
Read Program Memory CRC	0EH	No	—
Reserved	0FH –1AH	—	—
Read ICP Autobaud Register	1BH	Yes	—
Reserved	1CH – EFH	—	—
Write Test Mode Register	F0H	Yes	—
Read Test Mode Register	F1H	Yes	—
Reserved	F2H – FFH	—	—

In the following bulleted list of ICP commands, data and commands sent from the host to the ICP are identified by '`ICP ← Command/Data`'. Data sent from the ICP back to the host is identified by '`ICP → Data`':

- **Read ICP Revision (00H)**—The Read ICP Revision command determines the version of the ICP. If ICP commands are added, removed, or changed, the revision number changes.

```
ICP ← 00H
ICP → ICPRev[15:8] (Major revision number)
ICP → ICPRev[7:0] (Minor revision number)
```

programmed in this case a higher Baud rate can be used. Considering the ZLF645's system clock is of high frequency to support higher ICP Baud rates. The Baud rate necessary to support maximum programming efficiency is calculated as follows:

$$\text{Max Baud Rate} = 6 \text{ ICP byte} \times 10 \text{ ICP bits/byte} / 65 \text{ µs/byte} = 922.8 \text{ kbaud}$$

- The **Read Flash Memory** command can be used in the same two ways as described above for the **Write Flash Memory** command. When using the command to read multiple bytes of data from sequential address locations within the Flash memory, every byte read requires only 1 byte be received across the ICP interface. As described for the **Write Flash Memory**, there is no buffering of data that takes place between the ICP interface and the Flash Memory during memory reads. This means, as described for the **Write Flash Memory** command, the maximum Baud rate that memory read operations can occur at is dependent upon how quickly the ZLF645 completes a Flash Memory read operation, once it is initiated by the ICP. A ZLF645 memory read operation requires two system clock cycles to complete. Considering a ZLF645 system clock period of 250 ns, the theoretical maximum Baud rate reduces to the maximum Baud rate supported by the devices system clock frequency, which is calculated as follows:

$$\text{Max Baud Rate} = 1 / (500 \text{ ns/bit}) = 2 \text{ Mbaud}$$

The ICP baud rate for read operations is significantly higher than for programming operations.

3. The CPU writes to the Page Select (PGS) register.

Figure 20 displays the basic Flash Controller operation considering code based CPU Flash accesses and based upon the programming of the Flash Controllers Flash Control (FCTL), Sector Protect (FSEC), and Page Select (FPS) Registers. As mentioned previously for ICP based Flash accesses, the only modification to Figure 20 is that the programming of the Sector Protect (FSEC) register is ignored and the ICP has programming and erase access to a page independent of whether it resides in a protected sector. Figure 20 does not display the effects of the Flash read/write protect bits of User Option byte 1.

If either of these bits is enabled, their function takes priority over the operation description displayed in Figure 20 in terms of when a page erase or byte programming access is allowed (for more details, see Flash Code Protection Against External Access on page 73).

Table 33. Flash Control Register (FCTL)

Bits	7	6	5	4	3	2	1	0
Field	FCMD							
Reset	0	0	0	0	0	0	0	0
R/W	W	W	W	W	W	W	W	W
Address	Bank F, Register address: 01H							

Bit Position	Value	Description
[7:0]		**FCMD—Flash Command**
	73H	First unlock command.
	8CH	Second unlock command.
	95H	Page Erase command (From Flash Controller ‘Locked’ state, must be the third command written to this register to initiate Page Erase).
	63H	Mass Erase command (Ignored by Flash Controller if written by the CPU and executed by Flash Controller if ICP writes the command. From Flash Controller ‘Locked’ state, must be the third command written to this register to initiate Mass Erase).
	5EH	Enable Flash Sector Protect Register Access.

immediately if there is no valid data in the Receive Data register. If data is present in the Receive Data register, an interrupt will occur after the UART Receive Data register is read.

- **An overrun is detected—**An overrun occurs when a byte of data is received while there is valid data in the UART Receive Data register that has not been read by the user. The interrupt will be generated when the user reads the UART Receive Data register. The interrupt is cleared by reading the UART Receive Data register. When an overrun error occurs, the additional data byte will not overwrite the data currently stored in the UART Receive Data register.
- **A data framing error is detected**—A data framing error is detected when the first stop bit is 0 instead of 1. When configured for 2 stop bits, a data framing error is only detected when the first stop bit is 0. A framing error interrupt is generated when the framing error is detected. Reading the UART Receive Data register clears the interrupt.

Note: *Ensure that the transmitter uses the same stop bit configuration as the receiver.*

UART Overrun Errors

When an overrun error condition occurs the UART prevents overwriting of the valid data currently in the Receive Data register. The Break Detect and Overrun status bits are not displayed until after the valid data has been read.

After the valid data has been read, the UART Status (UST) register is updated to indicate the overrun condition (and Break Detect, if applicable). The UST[7] bit is set to 1 to indicate that the Receive Data register contains a data byte. However, because the overrun error occurred, this byte may not contain valid data and must be ignored. The Break Detect bit, UST[3], indicates if the overrun was caused by a break condition on the line. After reading the status byte indicating an overrun error, the Receive Data register must be read again to clear the error bits is the UART Status 0 register. Updates to the Receive Data register occur only when the next data word is received.

UART Data and Error Handling Procedure

Figure 25 on page 92 displays the recommended procedure for use in UART receiver interrupt service routine.

When T8 is enabled, the output T8_OUT switches to the initial value (CTR1, bit 1). If the initial value (CTR1, bit 1) is 0, TC8L is loaded; otherwise, TC8H is loaded into the counter.

In SINGLE-PASS mode (CTR0, bit 6), T8 counts down to 0 and stops, T8_OUT toggles, the time-out status bit (CTR0, bit 5) is set, and a time-out interrupt can be generated if it is enabled (CTR0, bit 1).

In MODULO-N mode, on reaching terminal count, T8_OUT is toggled, but no interrupt is generated. From that point, T8 loads a new count (if the T8_OUT level now is 0), TC8L is loaded; if it is 1, TC8H is loaded. T8 counts down to 0, toggles T8_OUT, and sets the time-out status bit (CTR0, bit 5), thereby generating an interrupt if enabled (CTR0, bit 1). One cycle is thus completed. T8 then loads from TC8H or TC8L according to the T8_OUT level and repeats the cycle. See Figure 29.

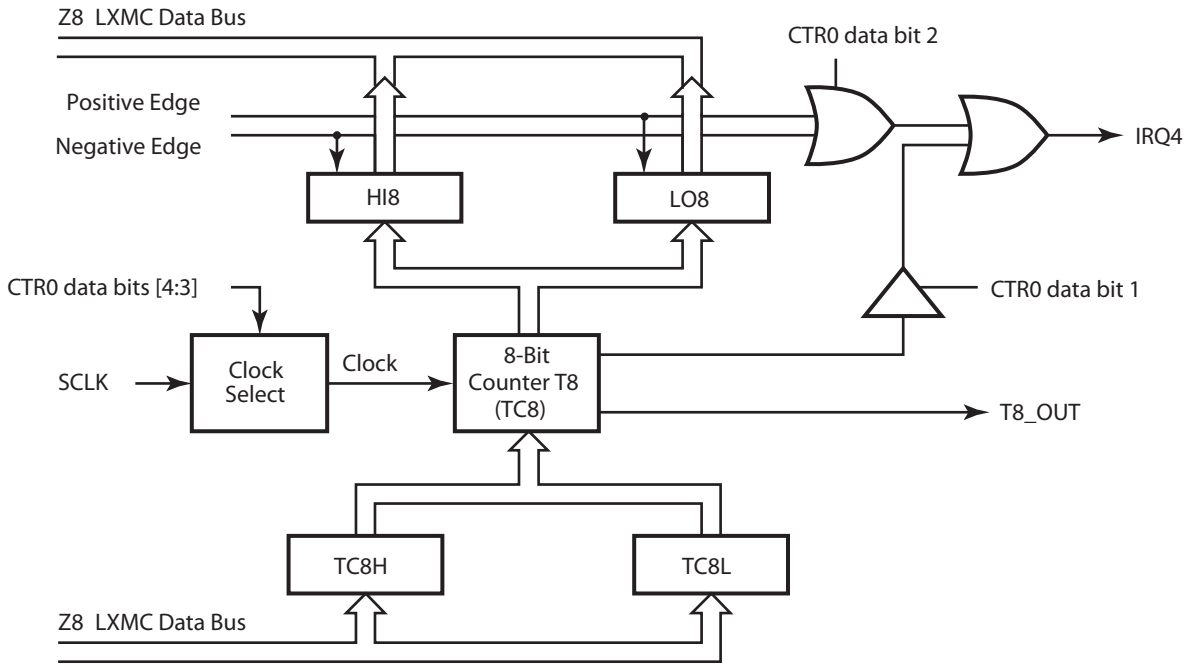


Figure 29. 8-Bit Counter/Timer Circuits

You can modify the values in TC8H or TC8L at any time. The new values take effect when they are loaded.

Caution: *An initial count of 1 is not allowed (a non-function occurs). An initial count of 0 causes TC8 to count from 0 to FFh to FEh.*

Bit Position	Value	Description
[5]	Read	**IRQ5 (Low-Voltage Detection)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[4]	Read	**IRQ4 (T8 Counter)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[3]	Read	**IRQ3 (T16 Counter)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[2]	Read	**IRQ2 (Port 3 Bit 1 Input)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[1]	Read	**IRQ1 (Port 3 Bit 3 Input/SMR Event/UART T_X/UART BRG)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[0]	Read	**IRQ0 (Port 3 Bit 2 Input/UART R_X)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.

Note: *The IRQ register is protected from change until an EI instruction is executed once.*

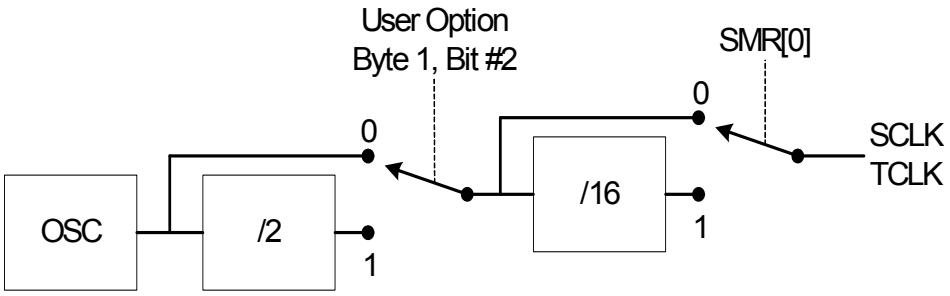


Figure 42. SCLK/TCLK Circuit

Note: *SMR[5] must be set to 1 if using a crystal or resonator clock source. The T_{POR} delay allows the clock source to stabilize before executing instructions.*

Stop Mode Recovery Interrupt

Software can set register bit SMR4[4] = 1 to enable routing of Stop Mode Recovery events to IRQ1 and to Port 3, Pin 3. In this configuration, if an IRQ1 interrupt occurs, register bit P3[3] = 0 indicates that a Stop Mode Recovery event is occurring.

Stop Mode Recovery Event Sources

Any Port 2 or Port 3 input pin can be configured to generate a Stop Mode Recovery event, either individually or in various logical combinations. The ZLF645 MCU provides the following registers for Stop Mode Recovery source configuration and status:

- **SMR Register**—Selects one Port 3, Pin 1–3 pin state or one of three Port 2 pin logical combinations to generate an event when a defined 0 or 1 level occurs.
- **SMR1 Register**—Configures one or more Port 2 input pins (0–7) to latch the latest read or write value and generate an event when the pin state changes.
- **SMR2 Register**—Selects one of seven Port 2 and 3 pin logical combinations to generate an event when a defined 0 or 1 level occurs.
- **SMR3 Register**—Configures one or more Port 3 input pins (0–3) to latch the latest read or write value and generates an event when the pin state changes.
- **SMR4 Register**—Enables routing of SMR events to IRQ1. Indicates whether port data has been latched for SMR1 or SMR3 event monitoring, and whether the latch was on a port read or write.

A Stop Mode Recovery event occurs if any of the sources defined in the SMR, SMR1, SMR2, and SMR3 registers are active.

SMR Register Events

The SMR register function is similar to the standard Stop Mode Recovery feature used in previous Z8® CPU-compatible parts. Register bits SMR[4:2] are set to select one of six event modes, as displayed in Figure 44 on page 145. The output of the corresponding logic is compared to the state of SMR[6]; when they are the same, a Stop Mode Recovery event is generated. If SMR[4:2]=000, no event source is selected by SMR.

The state SMR[4:2]=001 is reserved and selects no event in this device. The logic configured by the SMR register ignores any port pins that are configured as output or selected as source pins in registers SMR1 or SMR3. The SMR register is summarized in Table 69 on page 146.

Electrical Characteristics

Absolute Maximum Ratings

A stress greater than listed in Table 78 may cause permanent damage to the device. Functional operation of the device at any condition outside those indicated in the operational sections of these specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For improved reliability, unused inputs must be tied to one of the supply voltages (V_{DD} or V_{SS}).

Table 78. Absolute Maximum Ratings

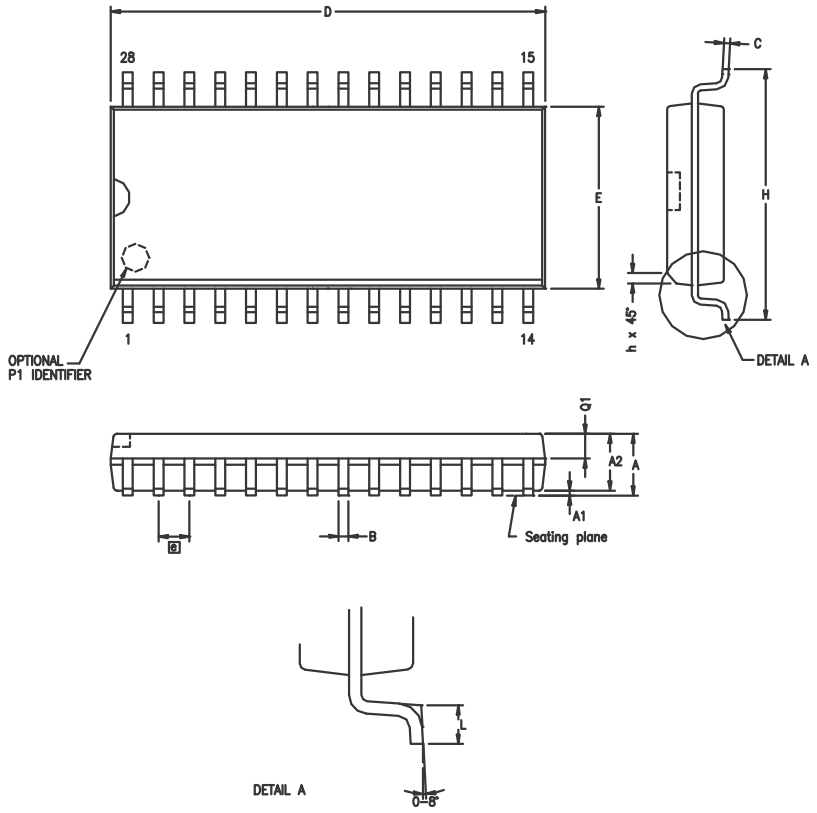
Parameter	Min	Max	Units
Ambient temperature under bias	0	+70	C
Storage temperature	–65	+150	C
Voltage on any pin with respect to V_{SS}*	–0.3	+4.0	V
Voltage on V_{DD} pin with respect to V_{SS}	–0.3	+3.6	V
Maximum current on input and/or inactive output pin	–5	+5	µA
Maximum output current from active output pin	–25	+25	mA
Maximum current into V_{DD} or out of V_{SS}	—	75	mA

*This voltage applies to all pins except V_{DD}, P32, and P33.

Table 81. Clock, Reset, Timers, and SMR Timing

No	Symbol	Parameter	V_{CC}	T_A = 0 °C to +70 °C 8.0 MHz		Units	WDTMR (Bits 6, 5, 4, 1, 0)
				Min	Max		
1	T_pC	Input Clock Period[1]	1.9–3.6	121	DC	ns	—
2	T_RC, T_FC	Clock Input Rise and Fall Times[1]	1.9–3.6	—	25	ns	—
3	T_WC	Input Clock Width[1]	1.9–3.6	37	—	ns	—
4	$T_WT_{IN}L$	Timer Input Low Width[1]	1.9	100	—	ns	—
			3.6	70	—	ns	—
5	$T_WT_{IN}H$	Timer Input High Width[1]	1.9–3.6	$3T_PC$	—	—	—
6	T_PT_{IN}	Timer Input Period[1]	1.9–3.6	$8T_PC$	—	—	—
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise and Fall Timers[1]	1.9–3.6	—	100	ns	—
8	T_WIL	Interrupt Request Low Time[1,2]	1.9	100	—	ns	—
			3.6	70	—	ns	—
9	T_WIH	Interrupt Request Input High Time[1,2]	1.9–3.6	$5T_PC$	—	—	—
10	T_{WSM}	Stop Mode Recovery Width Spec	1.9–3.6	12[3] 10 T_PC[4]	—	ns	—
11	T_{OST}	Oscillator Startup Time[4]	1.9–3.6	—	$5T_PC$	—	—
12	T_{WDT}	Watchdog Timer Delay Time	1.9–3.6	5	—	ms	0, 0, 0, 0, 0
			1.9–3.6	10	—	ms	0, 0, 0, 0, 1
			1.9–3.6	20	—	ms	0, 0, 0, 1, 0
			1.9–3.6	80	—	ms	0, 0, 0, 1, 1
			1.9–3.6	320	—	ms	0, 0, 1, X, X
			1.9–3.6	1, 280	—	ms	0, 1, 0, X, X
			1.9–3.6	5, 120	—	ms	1, 0, 0, X, X

Figure 55 displays the 28-pin small outline integrated circuit (SOIC) package for the ZLF645 Series of Flash MCUs.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.40	2.64	.094	.104
A1	0.10	0.30	.004	.012
A2	2.24	2.44	.088	.096
B	0.36	0.46	.014	.018
C	0.23	0.30	.009	.012
D	17.78	18.00	.700	.710
E	7.40	7.60	.291	.299
e	1.27 BSC		.050 BSC	
H	10.00	10.65	.394	.419
h	0.30	0.71	.012	.028
L	0.61	1.00	.024	.039
Q1	0.97	1.09	.038	.043

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH.

Figure 55. 28-Pin SOIC Package Diagram

U

V

W

X

Z