Analog Devices Inc./Maxim Integrated - ZLF645E0S2864G Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Z8 LXMC
Core Size	8-Bit
Speed	8MHz
Connectivity	UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, WDT
Number of I/O	24
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	1.9V ~ 3.6V
Data Converters	-
Oscillator Type	-
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/zlf645e0s2864g

Port 3 Mode Register

The Port 3 Mode register (see Table 19) is used to configure the functionality of Port 3 inputs and the output mode of Port 2. When bit 2 is set, the IR Learning Amplifier is used instead of the COMP1 comparator, regardless of the value of bit 1.

Table 19. Port 3 Mode Register (P3M)

Bit	7	6	5	4	3	2	1	0
Field	Reserved					IR Learning Amplifier	DIGITAL/ ANALOG Mode	Port 2 Open-Drain
Reset	X	X	X	X	X	0	0	0
R/W	—	—	—	—	—	W	W	W
Address	Bank Independent: F7h; Linear: 0F7h							

Bit Position	R/W	Value	Description
[7:3]	—	—	**Reserved**—Must be written to 1. Reads return 11111b.
[2]	W	0 1	IR Learning Amplifier disabled. IR Learning Amplifier enabled with P31 configured as amplifier input.
[1]	W		**DIGITAL/ANALOG Mode**
		0	P30, P31, P32, P33 are digital inputs.
		1	P30, P32, and P33 are comparator inputs. If P3M[2]=0, P31 also function as a comparator input. If P3M[2]=1, P31 is the IR amplifier input.
[0]	W	0 1	Port 2 open-drain. Port 2 push/pull.

Note: *Port 3 Mode register is not reset after a Stop Mode Recovery.*

shadow registers implemented within the RAM memory. This enables the entire 1K or 512 B, depending on the product, of the RAM memory to be used for the stack.

8-bit Stack Addressability

For 8-bit stack addressability, only the SPL register is used for stack addressing and stack operations that use the stack pointer always address Bank 0, independent of the RP[3:0] setting. For more details on the stack, refer to *Z8® LXMC CPU Core User Manual (UM0215)*.

When in 8-bit stack addressability mode, the Bank 0 register FEh can be used to store user data. See Stack Pointer Register on page 48.

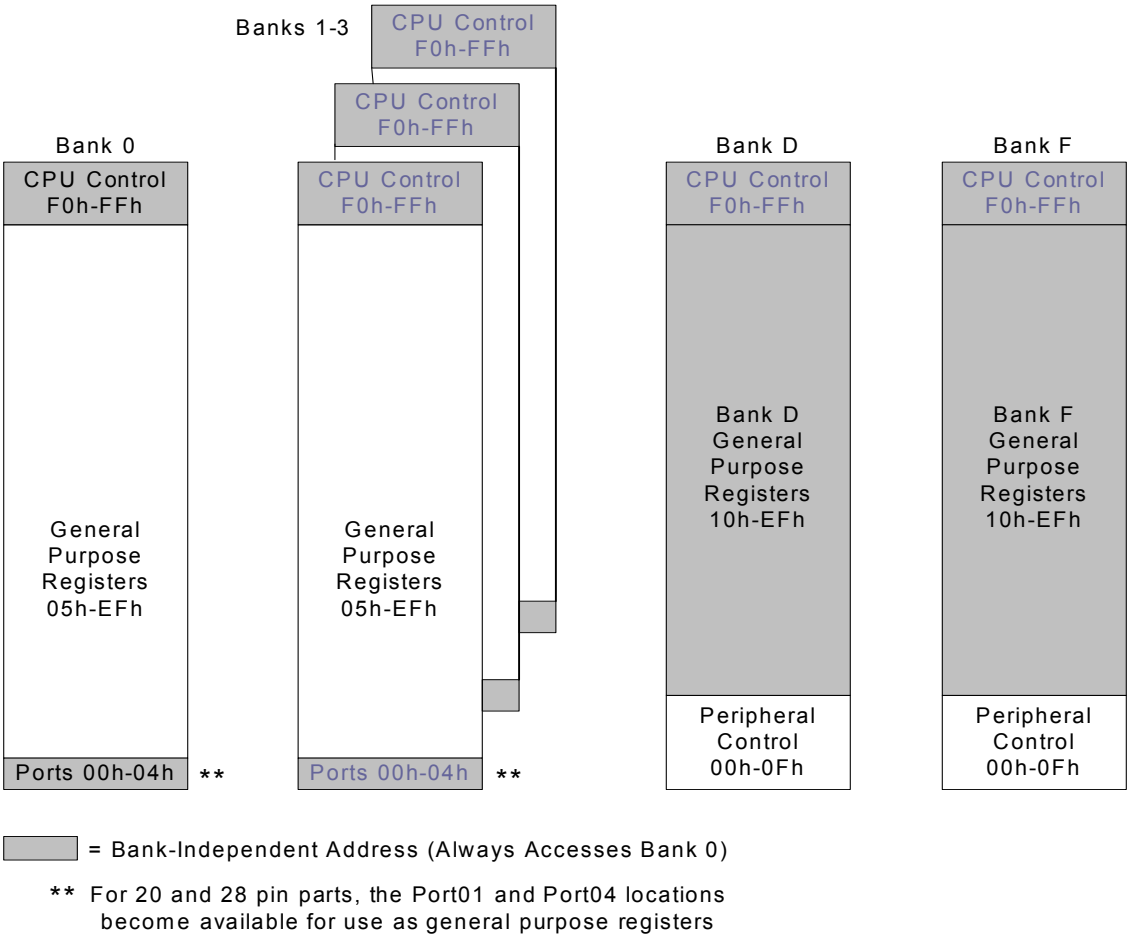


Figure 13. Register File 8-Bit Banked Address Map

As the ICP interface uses a single pin for both receive and transmit, it can only receive or transmit at a given time. For the most part, this is not a problem, as the ICP uses a host driven protocol (Z8® does not send any data without the host asking for it).

To aid the ICP in avoiding collisions, the transmitter waits an additional 1/2 bit times after a Stop bit is fully received or transmitted before it starts transmission of a character. On the other hand, the receiver starts searching for a Start bit as soon as the middle of the Stop bit has been sampled and is valid. The transmitter does not start if another character is being received.

ICP In-Circuit Programming Commands

The host communicates to the ICP by sending ICP commands using the ICP interface. During normal operation, only a subset of the ICP commands are available. In FLASH CONTROL mode, all ICP commands are available, but for few commands their access to the Flash is qualified based upon the programming of the Flash Read/Write Protect Option bit (FLRWP) or the Lower Half Flash Read/Write Protect Option bit (FLPROT1). When either of these bits is enabled, some of the ICP commands will have reduced Flash memory access or will be disabled completely.

Table 28 is a summary of the ICP commands. Each ICP command is described in further detail in the bulleted list following this table. Table 28 also indicates those commands that operate when the device is not in FLASH CONTROL mode (normal operation) and how those commands are effected by programming of the FLRWP and FLPROT1 Option bits.

Table 28. In-Circuit Programmer Commands

ICP Command	Command Byte	Enabled when NOT in FLASH CONTROL mode?	Disabled by Flash Read/Write Protect Option Bits (FLRWP and/or FLPROT1)
Read ICP Revision	00H	Yes	—
Reserved	01H	—	
Read ICP Status Register	02H	Yes	—
Reserved	03H	No	—
Write ICP Control Register	04H	Yes	—
Read ICP Control Register	05H	Yes	—
Reserved	06H – 07H	No	
Write Flash Controller Registers	08H	No	—

Flash Status Register

The Flash Status (FSTAT) register (see Table 34) indicates the current state of the Flash Controller. This register can be read any time. The read-only Flash Status (FSTAT) register shares its Register File address with the Write-only Flash Control (FCTL) register.

Table 34. Flash Status Register (FSTAT)

Bits	7	6	5	4	3	2	1	0
Field	Reserved		FSTAT					
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	Bank F, Register address: 01H							

Bit Position	Value	Description
[7:6]	—	**Reserved**—Reads as 0's.
[5:0]		**FSTAT**—Flash Controller Status
	000000	Flash Controller locked.
	000001	First unlock command received (73H written).
	000010	Second unlock command received (8CH written).
	000011	Flash Controller unlocked.
	000100	Sector protect register selected.
	001xxx	Program operation in progress.
	010xxx	Page erase operation in progress.
	100xxx	Mass erase operation in progress.

Flash Page Select Register

The Flash Page Select (FPS) register (see Table 35) shares address space with the Flash Sector Protect (FSEC) register. Unless the Flash Controller is in 'locked' state and its Flash Control (FCTL) register is written with 5EH, writes to this address target the Flash Page Select (FPS) register.

The FPS register is used to select one page within the Flash Main Memory or Information Block for programming or erasure depending upon whether its IFEN bit is 0 or 1 respectively. Each Flash Main Memory Page contains 512 bytes of Flash memory. During a Page Erase operation to the Main Memory, the page that will be erased is the one containing the 512 Flash memory locations where bits 15 through 9 of their addresses is equal to bits 6 through 0 of FPS register. For Main Memory programming operations, bits 15 through 9 of the address to be programmed must equal bits 6 through 0 of the FPS register for the Flash Controller to execute the operation. For page erase or programming operations to the Flash's Information Block as indicated by the IFEN bit being 1, the programming or

Flash Byte Programming Interface

Using the ZLF645's Flash Byte Programming interface, the on-chip Flash controller can be bypassed, allowing direct control of the Flash signals through registered values of certain of the ZLF645's GPIO pins. Bypassing the Flash controller allows faster row programming algorithms to be used by controlling the Flash programming signals directly. This method is beneficial when programming a large number of devices and can be used for Flash programming by third party vendors who manufacture gang programmers. For more information on how to use this interface, refer to *Third-Party Flash Programming Support for Z8 Crimzon Flash Parts*, available for download at www.maxim-ic.com.

Enabling The Flash Byte Programming Interface

The Flash Byte Programming Interface is enabled by writing three bytes to the ICP interface:

1. 80H — initiates auto-baud calculation of the ICP interface data and clock rate.
2. F0H — ICP Write Test Mode Register command.
3. 04H — Data to be written to the Test Mode Register. This enables the Flash Byte Programming interface.

Note: *Since Flash Byte Programming Interface is enabled with the ZLF645 MCU in ICP mode, the CPU clock will stop and no CPU accesses to the Flash memory will occur.*

Flash Byte Programming Interface Flash Access Restrictions

The types of Flash access allowed to the Flash memory through the Flash Byte Programming interface is qualified similar to the ICP, by the settings of the Flash Memory Protection Bits in User Option Byte 1. If either of the Flash protect bits are set, the program memory has to be mass erased before full read/program access is allowed to either the main memory or Information area page 3 sections of the Flash memory, respectively. Flash memory access allowed through the Flash Byte Programming interface is summarized in Table 40.

Table 40.Flash Byte Programming Functions Summary

Flash Memory Block	Program	Read	Page Erase	Mass Erase	Flash Protect Option Bits
Main Memory	Yes	Yes	Yes	Yes	FLRWP=1, FLPROT1=1
Main Memory	No	No	No	Yes	FLRWP=0, FLPROT1=X
Main Memory	Yes[1]	Yes[1]	Yes[1]	Yes	FLRWP=1, FLPROT1=0
Information Area	Yes[2]	Yes[2]	Yes[2]	Yes	FLRWP=1, FLPROT1=1
Information Area	No	Yes[2]	No	Yes	FLRWP=1, FLPROT1=0
Information Area	No	Yes[2]	No	Yes	FLRWP=0, FLPROT1=1

Notes

1. Program, Read, and Page Erase access is limited to the upper half address space of the main memory only.
2. Only Page 3 of the Information Area is accessible for Program, Read, and Page Erase operations.

Architecture

The UARTs consist of three primary functional blocks: **transmitter**, **receiver**, and **Baud Rate Generator**. The UART transmitter and receiver function independently, but employ the same baud rate and data format. Figure 22 displays the UART architecture.

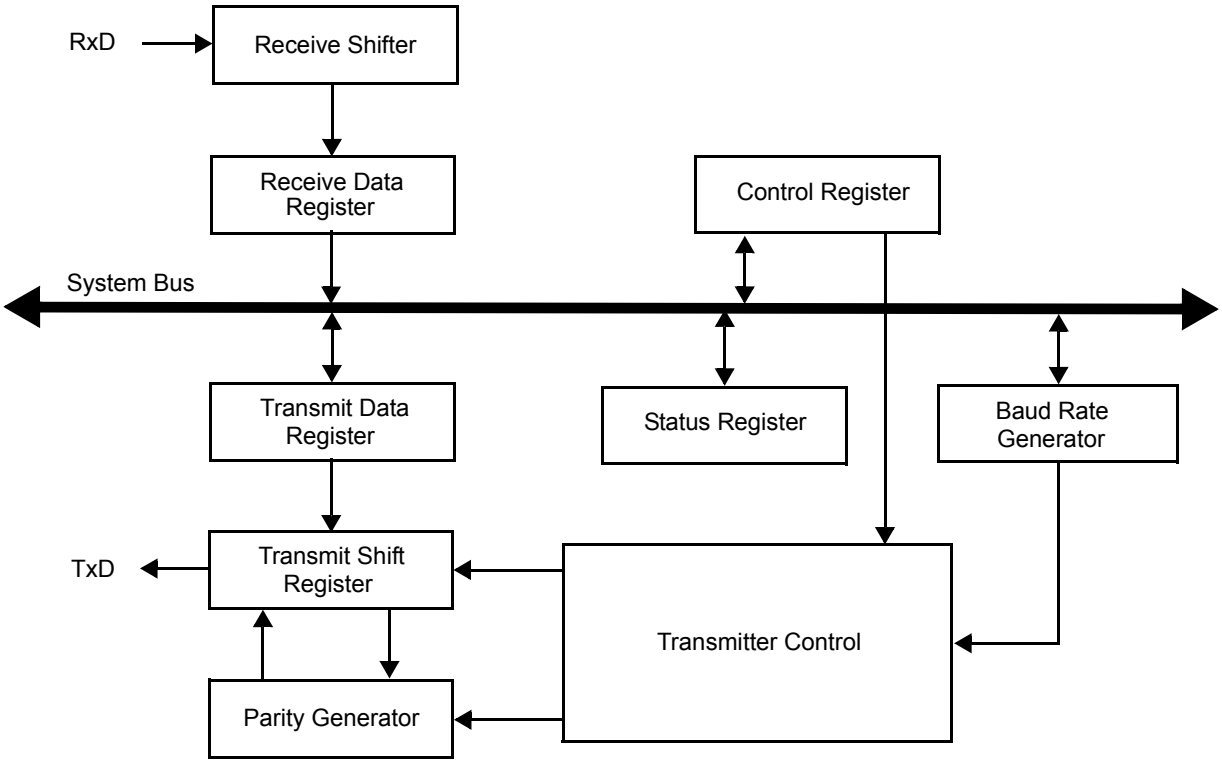


Figure 22. UART Block Diagram

Operation

The UART channel can be used to communicate with a master microprocessor or a slave microprocessor, both of which exhibit transmit and receive functionality. You can either operate the UART channel by polling the UART Status register or via interrupts. The UART remains active during HALT mode. If neither the transmitter nor the receiver is enabled, the UART baud rate generator can be used as an additional timer. The UART contains a noise filter for the receiver that can be enabled by the user.

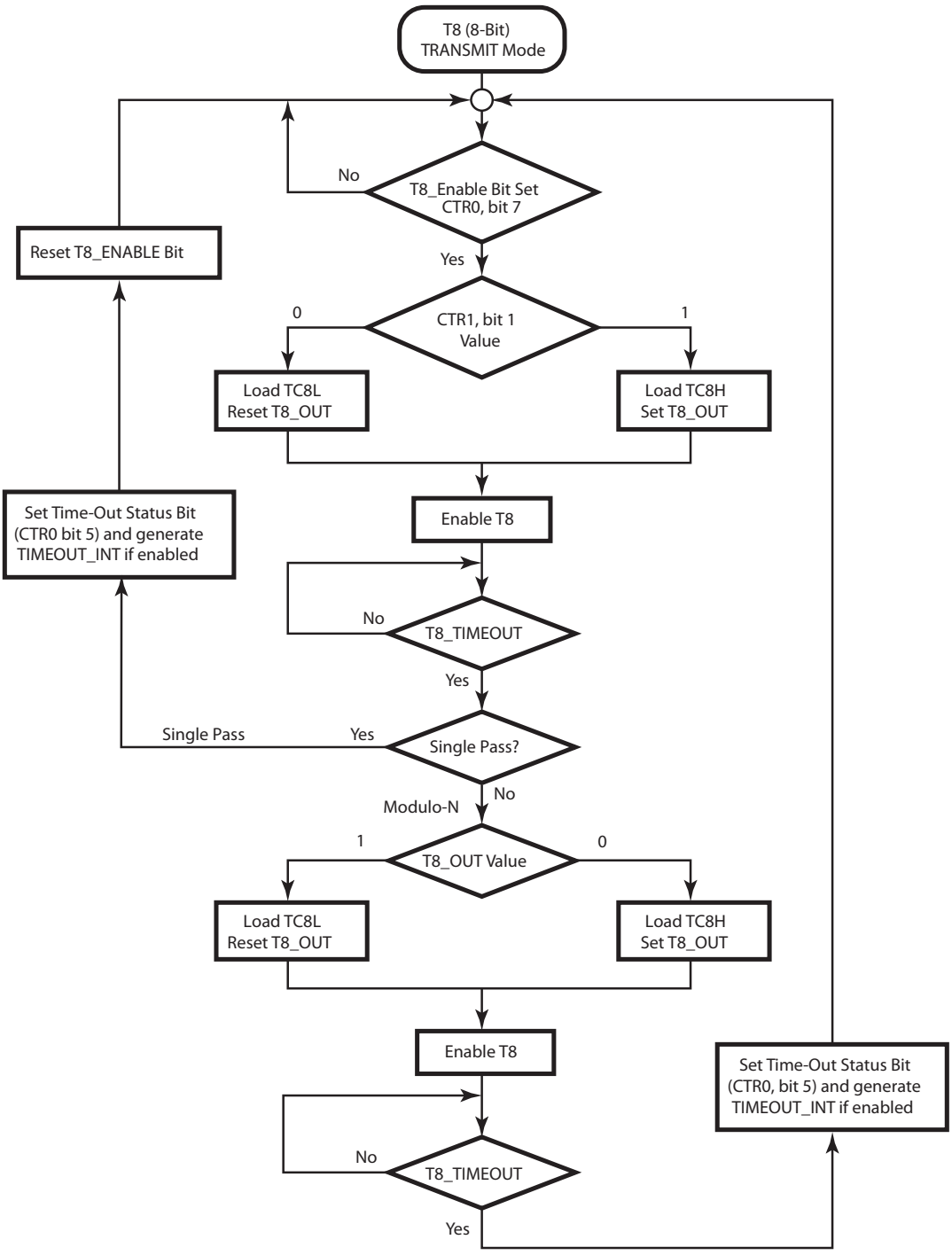


Figure 28. TRANSMIT Mode Flowchart

Timer 16 Capture Low Register

The Timer 16 Capture Low register (see Table 51) holds the captured data from the output of the 16-bit Counter/Timer 16. This register contains the least significant byte (LSB) of the data.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 51. Timer 16 Capture Low Register (LO16)

Bit	7	6	5	4	3	2	1	0
Field	T16_Capture_LO							
Reset	0	0	0	0	0	0	0	0
R/W	R	R	R	R	R	R	R	R
Address	Bank D: 08h; Linear: D08h							

Bit Position	Value	Description
[7:0]	0hh–FFh	**T16_Capture_LO**—Read returns captured data. Writes have no effect.

Counter/Timer 16 High Hold Register

The Counter/Timer 16 High Hold register (see Table 52) contains the high byte of the value loaded into the T16 timer.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 52. Counter/Timer 16 High Hold Register (TC16H)

Bit	7	6	5	4	3	2	1	0
Field	T16_Data_HI							
Reset	0	0	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Address	Bank D: 07h; Linear: D07h							

Bit Position	Value	Description
[7:0]	0hh–FFh	**T16_Data_HI**—Read/Write Data.

Counter/Timer 8 Low Hold Register

The Counter/Timer 8 Low Hold register (see Table 55) contains the value to be counted while the T8 output is 0.

Note: *This register is not reset after a Stop Mode Recovery.*

Table 55. Counter/Timer 8 Low Hold Register (TC8L)

Bit	7	6	5	4	3	2	1	0
Field	T8_Level_LO							
Reset	0	0	0	0	0	0	0	0
R/W	Bank D: 04h; Linear: D04h							
Address	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit Position	Value	Description
[7:0]	0hh–FFh	**T8_Level_LO**—Read/Write Data.

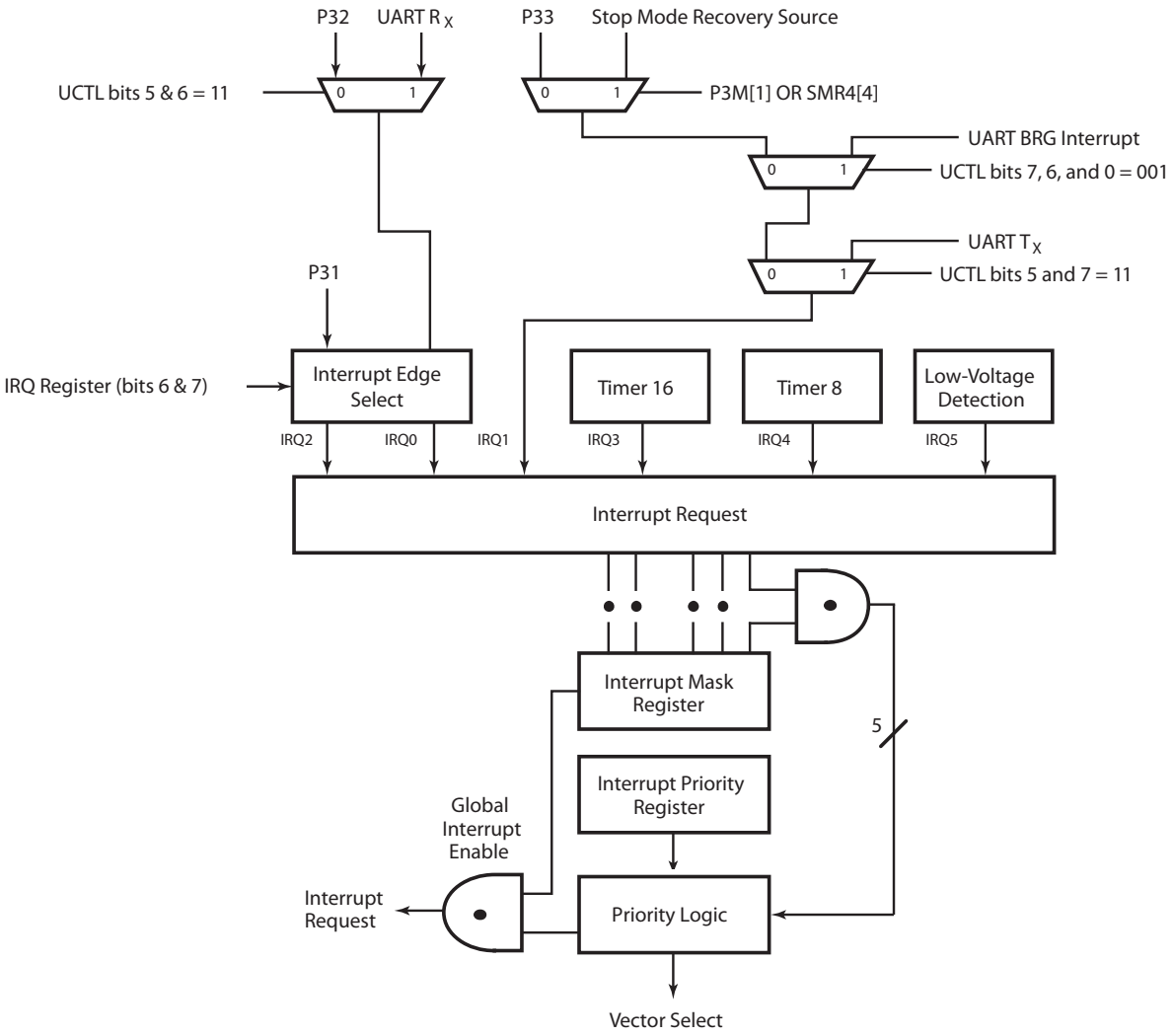


Figure 40. Interrupt Block Diagram

Bit Position	Value	Description
[5]	Read	**IRQ5 (Low-Voltage Detection)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[4]	Read	**IRQ4 (T8 Counter)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[3]	Read	**IRQ3 (T16 Counter)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[2]	Read	**IRQ2 (Port 3 Bit 1 Input)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[1]	Read	**IRQ1 (Port 3 Bit 3 Input/SMR Event/UART T_X/UART BRG)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.
[0]	Read	**IRQ0 (Port 3 Bit 2 Input/UART R_X)**
	0	Interrupt did not occur.
	1	Interrupt occurred.
	Write	
	0	Clear interrupt.
	1	Set interrupt.

Note: *The IRQ register is protected from change until an EI instruction is executed once.*

Voltage Brownout Standby

An on-chip voltage comparator circuit (VBO) checks that the V_{DD} is at the required level for correct operation of the device in terms of Flash memory reads. A second on-chip comparator circuit (subVBO) checks that the V_{DD} level is high enough for proper operation of the VBO circuit. If the V_{DD} level drops below the VBO trip point, the ZLF645 will be held in a reset state as long as V_{DD} remains below this trip point value, and the XTAL1 and XTAL2 oscillator circuitry will be disabled thereby stopping the clock input to the ZLF645 and saving power. If the V_{DD} level continues to drop below the subVBO trip point, the ZLF645 will remain in a reset state and the VBO comparator circuit will be disabled for further power savings. When the power level returns to a value above the VBO trip point, the device performs a power-on reset and functions normally.

STOP Mode

`STOP` instruction turns OFF the internal clock and external crystal oscillation, thus reducing the MCU supply current to a very low level. For STOP mode current specifications, see Table 80 on page 165.

To enter STOP mode, first flush the instruction pipeline to avoid suspending execution in mid-instruction. Execute a NOP instruction (OpCode = `FFh`) immediately before the appropriate sleep instruction, as given below:

```
FF          NOP         ; clear the pipeline
6F          STOP        ; enter STOP mode
```

STOP mode is terminated only by a reset, such as WDT time-out, POR, or one of the Stop Mode Recovery events as described in Stop Mode Recovery Event Sources on page 144. This condition causes the processor to restart the application program at address `000Ch`.

Unlike a normal POR or WDT reset, a Stop Mode Recovery reset does not reset the contents of some registers and bits. Register bits not reset by a Stop Mode Recovery are highlighted in grey in the register tables. Register bit SMR[7] is set to 1 by a Stop Mode Recovery.

HALT Mode

`HALT` instruction turns off the internal CPU clock, but not the XTAL oscillation.
The counter/timers, UART, and interrupts (IRQ0, IRQ1, IRQ2, IRQ3, IRQ4, and IRQ5) remain active. The devices are recovered by interrupts, either externally or internally generated. An interrupt request must be executed (enabled) to exit HALT mode. After the interrupt service routine, the program continues from the instruction after HALT mode.

After the following example code is executed, a 1 on P20 will wake the part from STOP mode:

```
LD P2M, #%FF     ;Set Port 2 to inputs.
SRP #%0F         ;Point to expanded bank F
LD SMR1, #%01    ;Select P20 for SMR1.
SRP #%00         ;Point to bank 0
LD P2, #%00      ;Write 00h to Port 2, so the P20 reference
                 ;value is 0, and a 1 on P20 wakes the part.
NOP
STOP
```

After the following example code is executed when the value of P2 is 00h, a 1 on P20 will wake the part from STOP mode:

```
LD P2M, #%FF     ;Set ports to inputs.
SRP #%0F         ;Point to expanded bank F
LD SMR1, #%01    ;Select P20 for SMR1.
SRP #%00         ;Point to bank 0
LD R6, P2        ;If a 0 is read from Port 2, the P20 reference
                 ;value is 0, so a 1 on P20 wakes the part.
NOP
STOP
```

Table 72. Stop Mode Recovery Register 3 (SMR3)

Bit	7	6	5	4	3	2	1	0
Field	—				P33 SMR Select	P32 SMR Select	P31 SMR Select	P30 SMR Select
Reset	X	X	X	X	0	0	0	0
R/W	—	—	—	—	W	W	W	W
Address	Bank F: 0Eh; Linear: F0Eh							

Bit Position	Value	Description
[7:4]	—	**Reserved**—Reads undefined; Must be written to 1.
[3]	0 1	P33 not selected. P33 SMR source selected.
[2]	0 1	P32 not selected. P32 SMR source selected.
[1]	0 1	P31 not selected. P31 SMR source selected.
[0]	0 1	P30 not selected. P30 SMR source selected.

Note: *This register is not reset after a Stop Mode Recovery.*

Standard Test Conditions

The characteristics listed in this product specification apply for standard test conditions. All voltages are referenced to Ground. Positive current flows into the referenced pin (see Figure 48).

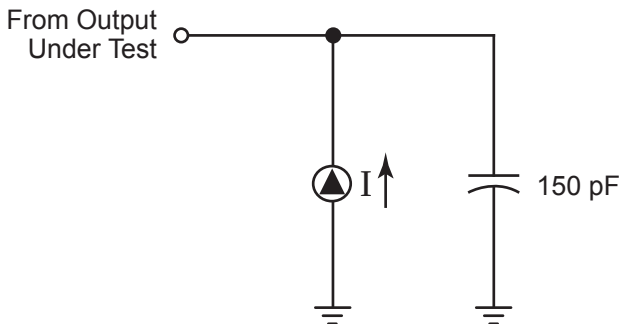


Figure 48. Test Load Diagram

Capacitance

Table 79 lists the capacitance.

Table 79. Capacitance

Parameter	Maximum
Input capacitance	12 pF
Output capacitance	12 pF
I/O capacitance	12 pF

Note: T_A = 25 °C, V_{CC} = GND = 0 V, f = 1.0 MHz, unmeasured pins return to GND. This voltage applies to all pins except V_{DD}, P32, and P33.

DC Characteristics

Table 80 describes the direct current (DC) characteristics of the ZLF645 Flash MCU.

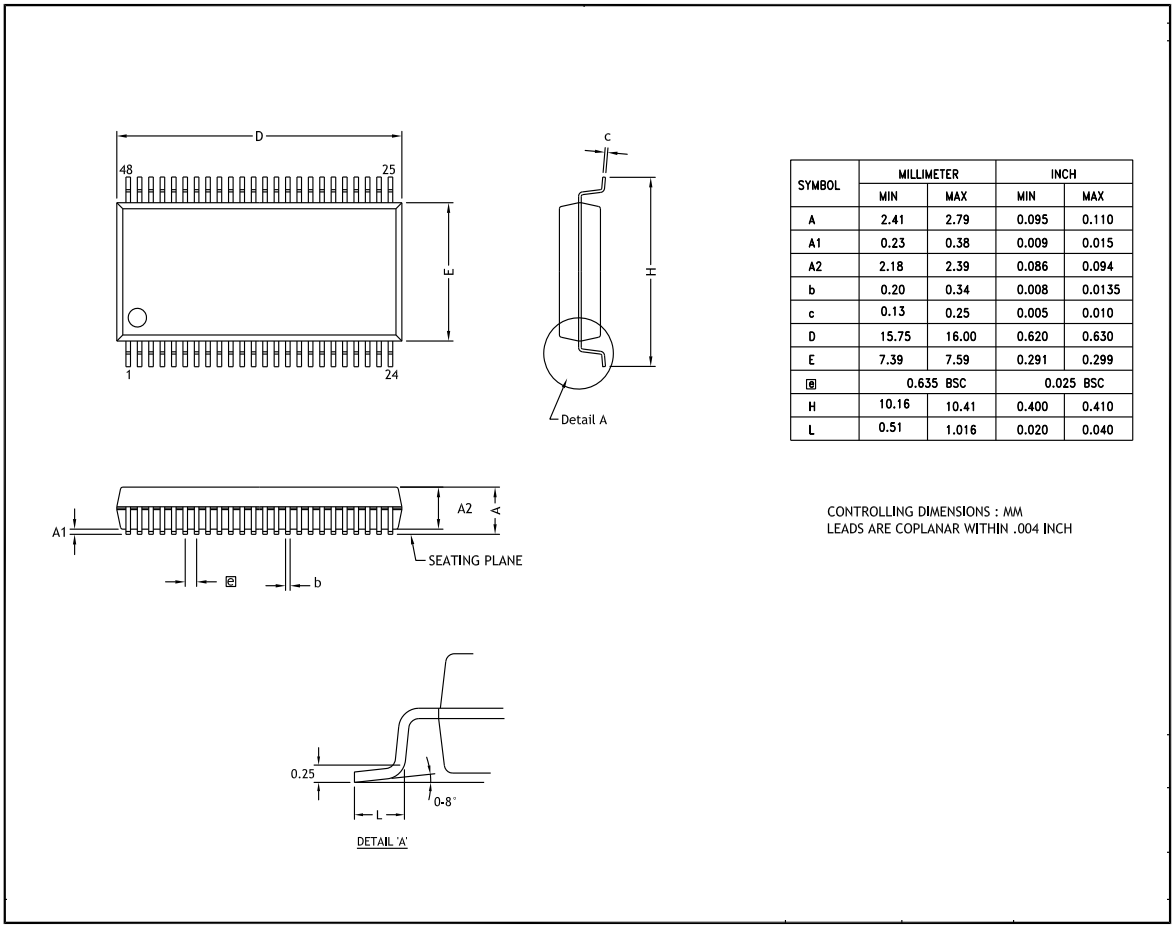
Table 80. DC Characteristics

			T_A = 0 °C to +70 °C				
Symbol	**Parameter**	**V_{CC}**	**Min**	**Typ**	**Max**	**Units**	**Conditions**
V_{CC}	Supply Voltage[1]	—	1.9	—	3.6	V	See Note 5.
V_{CH}	Clock Input High Voltage	1.9–3.6	0.8 V_{CC}	—	V_{CC} + 0.3	V	Driven by External Clock Generator
V_{CL}	Clock Input Low Voltage	1.9–3.6	V_{SS}–0.3	—	0.4	V	Driven by External Clock Generator
V_{IH}	Input High Voltage	1.9–3.6	0.7 V_{CC}	—	V_{CC} + 0.3	V	—
V_{IL}	Input Low Voltage	1.9–3.6	V_{SS}–0.3	—	0.2 V_{cc}	V	—
V_{OH1}	Output High Voltage	1.9–3.6	V_{CC}–0.4	—	—	V	I_{OH} = -0.5 mA
V_{OH2}	Output High Voltage (P36, P37, P00, and P01)	1.9–3.6	V_{CC}–0.8	—	—	V	I_{OH} = -7 mA
V_{OL1}	Output Low Voltage	1.9–3.6	—	—	0.4	V	I_{OL} = 4.0 mA
V_{OL2}	Output Low Voltage (P00, P01, P36, and P37)	1.9–3.6	—	—	0.8	V	I_{OL} = 10 mA
V_{OFFSET}	Comparator Input Offset Voltage	1.9–3.6	—	—	25	mV	—
V_{REF}	Comparator Reference Voltage	1.9–3.6	0	—	V_{CC} -1.75	V	—
I_{IL}	Input Leakage	1.9–3.6	-1	—	1	µA	V_{IN} = 0 V, V_{CC}; pull-ups disabled
I_{IL1}	Input Leakage IR Amp (P31)	1.9–3.6	-2.5	—	-12	µA	V_{IN} = 0 V, IR amp enabled
I_{OL}	Output Leakage	1.9–3.6	-1	—	1	µA	V_{IN} = 0 V, V_{CC}
I_{CC}	Supply Current[2, 3]	1.9	—	1	2	mA	See Note 7.
		3.6	—	2	4	mA	
		1.9	—	2	3	mA	See Note 8.
		3.6	—	4	6	mA	

Table 81. Clock, Reset, Timers, and SMR Timing

No	Symbol	Parameter	V_{CC}	T_A = 0 °C to +70 °C 8.0 MHz		Units	WDTMR (Bits 6, 5, 4, 1, 0)
				Min	Max		
1	T_pC	Input Clock Period[1]	1.9–3.6	121	DC	ns	—
2	T_RC, T_FC	Clock Input Rise and Fall Times[1]	1.9–3.6	—	25	ns	—
3	T_WC	Input Clock Width[1]	1.9–3.6	37	—	ns	—
4	$T_WT_{IN}L$	Timer Input Low Width[1]	1.9	100	—	ns	—
			3.6	70	—	ns	—
5	$T_WT_{IN}H$	Timer Input High Width[1]	1.9–3.6	$3T_PC$	—	—	—
6	T_PT_{IN}	Timer Input Period[1]	1.9–3.6	$8T_PC$	—	—	—
7	T_RT_{IN}, T_FT_{IN}	Timer Input Rise and Fall Timers[1]	1.9–3.6	—	100	ns	—
8	T_WIL	Interrupt Request Low Time[1,2]	1.9	100	—	ns	—
			3.6	70	—	ns	—
9	T_WIH	Interrupt Request Input High Time[1,2]	1.9–3.6	$5T_PC$	—	—	—
10	T_{WSM}	Stop Mode Recovery Width Spec	1.9–3.6	12[3] 10 T_PC[4]	—	ns	—
11	T_{OST}	Oscillator Startup Time[4]	1.9–3.6	—	$5T_PC$	—	—
12	T_{WDT}	Watchdog Timer Delay Time	1.9–3.6	5	—	ms	0, 0, 0, 0, 0
			1.9–3.6	10	—	ms	0, 0, 0, 0, 1
			1.9–3.6	20	—	ms	0, 0, 0, 1, 0
			1.9–3.6	80	—	ms	0, 0, 0, 1, 1
			1.9–3.6	320	—	ms	0, 0, 1, X, X
			1.9–3.6	1, 280	—	ms	0, 1, 0, X, X
			1.9–3.6	5, 120	—	ms	1, 0, 0, X, X

Figure 57 displays the 48-pin shrink small outline package (SSOP) for the ZLF645 Series of Flash MCUs.



SYMBOL	MILLIMETER		INCH	
	MIN	MAX	MIN	MAX
A	2.41	2.79	0.095	0.110
A1	0.23	0.38	0.009	0.015
A2	2.18	2.39	0.086	0.094
b	0.20	0.34	0.008	0.0135
c	0.13	0.25	0.005	0.010
D	15.75	16.00	0.620	0.630
E	7.39	7.59	0.291	0.299
e	0.635 BSC		0.025 BSC	
H	10.16	10.41	0.400	0.410
L	0.51	1.016	0.020	0.040

CONTROLLING DIMENSIONS : MM
LEADS ARE COPLANAR WITHIN .004 INCH

Figure 57. 48-Pin SSOP Package Diagram