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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f805fv80

Part 1 Overview

1.1 56F805 Features

1.1.1 Processing Core

- Efficient 16-bit 56800 family processor engine with dual Harvard architecture
- As many as 40 Million Instructions Per Second (MIPS) at 80MHz core frequency
- Single-cycle 16 × 16-bit parallel Multiplier-Accumulator (MAC)
- Two 36-bit accumulators, including extension bits
- 16-bit bidirectional barrel shifter
- Parallel instruction set with unique processor addressing modes
- Hardware DO and REP loops
- Three internal address buses and one external address bus
- Four internal data buses and one external data bus
- Instruction set supports both DSP and controller functions
- Controller style addressing modes and instructions for compact code
- Efficient C compiler and local variable support
- Software subroutine and interrupt stack with depth limited only by memory
- JTAG/OnCE debug programming interface

1.1.2 Memory

- Harvard architecture permits as many as three simultaneous accesses to Program and Data memory
- On-chip memory including a low-cost, high-volume Flash solution
  - 31.5K × 16 bit words of Program Flash
  - 512 × 16-bit words of Program RAM
  - 4K× 16-bit words of Data Flash
  - 2K × 16-bit words of Data RAM
  - 2K × 16-bit words of Boot Flash
- Off-chip memory expansion capabilities programmable for 0, 4, 8, or 12 wait states
  - As much as 64K × 16 bits of Data memory
  - As much as 64K × 16 bits of Program memory

1.1.3 Peripheral Circuits for 56F805

- Two Pulse Width Modulator modules each with six PWM outputs, three Current Sense inputs, and four Fault inputs, fault tolerant design with dead time insertion; supports both center- and edge-aligned modes
- Two 12-bit Analog-to-Digital Converters (ADC) which support two simultaneous conversions; ADC and PWM modules can be synchronized
- Two Quadrature Decoders each with four inputs or two additional Quad Timers

Part 2 Signal/Connection Descriptions

2.1 Introduction

The input and output signals of the 56F805 are organized into functional groups, as shown in **Table 2-1** and as illustrated in **Figure 2-1**. In **Table 2-2** through **Table 2-18**, each table row describes the signal or signals present on a pin.

Table 2-1 Functional Group Pin Allocations

Functional Group	Number of Pins	Detailed Description
Power (V_{DD} or V_{DDA})	9	**Table 2-2**
Ground (V_{SS} or V_{SSA})	9	**Table 2-3**
Supply Capacitors and V_{PP}	3	**Table 2-4**
PLL and Clock	3	**Table 2-5**
Address Bus[1]	16	**Table 2-6**
Data Bus	16	**Table 2-7**
Bus Control	4	**Table 2-8**
Interrupt and Program Control	5	**Table 2-9**
Dedicated General Purpose Input/Output	14	**Table 2-10**
Pulse Width Modulator (PWM) Port	26	**Table 2-11**
Serial Peripheral Interface (SPI) Port[1]	4	**Table 2-12**
Quadrature Decoder Port[2]	8	**Table 2-13**
Serial Communications Interface (SCI) Port[1]	4	**Table 2-14**
CAN Port	2	**Table 2-15**
Analog to Digital Converter (ADC) Port	9	**Table 2-16**
Quad Timer Module Ports	6	**Table 2-17**
JTAG/On-Chip Emulation (OnCE)	6	**Table 2-18**

1. Alternately, GPIO pins
2. Alternately, Quad Timer pins

2.10 Serial Communications Interface (SCI) Signals

Table 2-14 Serial Communications Interface (SCI0 and SCI1) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TXD0** **GPIOE0**	Output Input/Output	Input Input	**Transmit Data (TXD0)**—SCI0 transmit data output **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI output.
1	**RXD0** **GPIOE1**	Input Input/Output	Input Input	**Receive Data (RXD0)**— SCI0 receive data input **Port E GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as input or output pin. After reset, the default state is SCI input.
1	**TXD1** **GPIOD6**	Output Input/Output	Input Input	**Transmit Data (TXD1)**—SCI1 transmit data output **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI output.
1	**RXD1** **GPIOD7**	Input Input/Output	Input Input	**Receive Data (RXD1)**—SCI1 receive data input **Port D GPIO**—This pin is a General Purpose I/O (GPIO) pin that can individually be programmed as an input or output pin. After reset, the default state is SCI input.

2.11 CAN Signals

Table 2-15 CAN Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**MSCAN_ RX**	Input (Schmitt)	Input	**MSCAN Receive Data**—This is the MSCAN input. This pin has an internal pull-up resistor.
1	**MSCAN_ TX**	Output	Output	**MSCAN Transmit Data**—MSCAN output. CAN output is open-drain output and a pull-up resistor is needed.

2.12 Analog-to-Digital Converter (ADC) Signals

Table 2-16 Analog to Digital Converter Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
4	**ANA0–3**	Input	Input	**ANA0–3**—Analog inputs to ADC channel 1
4	**ANA4–7**	Input	Input	**ANA4–7**—Analog inputs to ADC channel 2
1	**VREF**	Input	Input	**VREF**—Analog reference voltage for ADC. Must be set to V_{DDA} - 0.3V for optimal performance.

2.13 Quad Timer Module Signals

Table 2-17 Quad Timer Module Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
2	**TC0-1**	Input/Output	Input	**TC0–1**—Timer C Channels 0 and 1
4	**TD0-3**	Input/Output	Input	**TD0–3**—Timer D Channels 0, 1, 2, and 3

2.14 JTAG/OnCE

Table 2-18 JTAG/On-Chip Emulation (OnCE) Signals

No. of Pins	Signal Name	Signal Type	State During Reset	Signal Description
1	**TCK**	Input (Schmitt)	Input, pulled low internally	**Test Clock Input**—This input pin provides a gated clock to synchronize the test logic and shift serial data to the JTAG/OnCE port. The pin is connected internally to a pull-down resistor.
1	**TMS**	Input (Schmitt)	Input, pulled high internally	**Test Mode Select Input**—This input pin is used to sequence the JTAG TAP controller's state machine. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor. **Note:** Always tie the TMS pin to V_{DD} through a 2.2K resistor.
1	**TDI**	Input (Schmitt)	Input, pulled high internally	**Test Data Input**—This input pin provides a serial input data stream to the JTAG/OnCE port. It is sampled on the rising edge of TCK and has an on-chip pull-up resistor.
1	**TDO**	Output	Tri-stated	**Test Data Output**—This tri-statable output pin provides a serial output data stream from the JTAG/OnCE port. It is driven in the Shift-IR and Shift-DR controller states, and changes on the falling edge of TCK.
1	**$\overline{\text{TRST}}$**	Input (Schmitt)	Input, pulled high internally	**Test Reset**—As an input, a low signal on this pin provides a reset signal to the JTAG TAP controller. To ensure complete hardware reset, $\overline{\text{TRST}}$ should be asserted at power-up and whenever $\overline{\text{RESET}}$ is asserted. The only exception occurs in a debugging environment when a hardware device reset is required and it is necessary not to reset the OnCE/JTAG module. In this case, assert $\overline{\text{RESET}}$, but do not assert $\overline{\text{TRST}}$. **Note:** For normal operation, connect $\overline{\text{TRST}}$ directly to V_{SS}. If the design is to be used in a debugging environment, $\overline{\text{TRST}}$ may be tied to V_{SS} through a 1K resistor.
1	**$\overline{\text{DE}}$**	Output	Output	**Debug Event**—$\overline{\text{DE}}$ provides a low pulse on recognized debug events.

Part 3 Specifications

3.1 General Characteristics

The 56F805 is fabricated in high-density CMOS with 5V-tolerant TTL-compatible digital inputs. The term "5V-tolerant" refers to the capability of an I/O pin, built on a 3.3V-compatible process technology, to withstand a voltage up to 5.5V without damaging the device. Many systems have a mixture of devices designed for 3.3V and 5V power supplies. In such systems, a bus may carry both 3.3V and 5V-compatible I/O voltage levels (a standard 3.3V I/O is designed to receive a maximum voltage of 3.3V ± 10% during

normal operation without causing damage). This 5V-tolerant capability therefore offers the power savings of 3.3V I/O levels while being able to receive 5V levels without being damaged.

Absolute maximum ratings given in **Table 3-1** are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond these ratings may affect device reliability or cause permanent damage to the device.

The 56F805 DC/AC electrical specifications are preliminary and are from design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. Finalized specifications will be published after complete characterization and device qualifications have been completed.

CAUTION

This device contains protective circuitry to guard against damage due to high static voltage or electrical fields. However, normal precautions are advised to avoid application of any voltages higher than maximum rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate voltage level.

Table 3-1 Absolute Maximum Ratings

Characteristic	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	V_{SS} – 0.3	V_{SS} + 4.0	V
All other input voltages, excluding Analog inputs, EXTAL and XTAL	V_{IN}	V_{SS} – 0.3	V_{SS} + 5.5V	V
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	- 0.3	0.3	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	- 0.3	0.3	V
Analog inputs, ANA0-7 and VREF	V_{IN}	V_{SSA} – 0.3	V_{DDA} + 0.3	V
Analog inputs EXTAL and XTAL	V_{IN}	V_{SSA}– 0.3	V_{SSA}+ 3.0	V
Current drain per pin excluding V_{DD}, V_{SS}, PWM outputs, TCS, V_{PP}, V_{DDA}, V_{SSA}	I	—	10	mA

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Supply voltage, digital	V_{DD}	3.0	3.3	3.6	V
Supply Voltage, analog	V_{DDA}	3.0	3.3	3.6	V

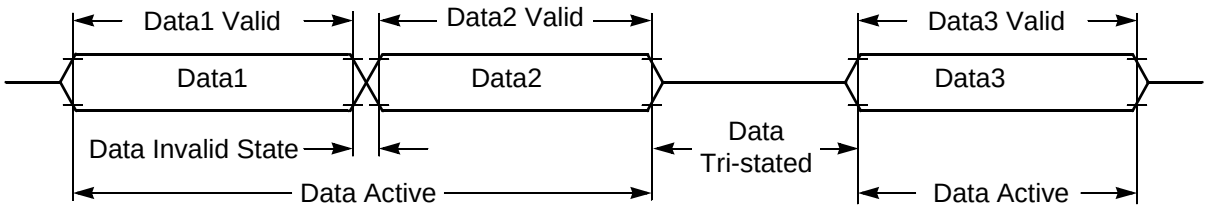


Figure 3-3 Signal States

3.4 Flash Memory Characteristics

Table 3-5 Flash Memory Truth Table

Mode	XE[1]	YE[2]	SE[3]	OE[4]	PROG[5]	ERASE[6]	MAS1[7]	NVSTR[8]
Standby	L	L	L	L	L	L	L	L
Read	H	H	H	H	L	L	L	L
Word Program	H	H	L	L	H	L	L	H
Page Erase	H	L	L	L	L	H	L	H
Mass Erase	H	L	L	L	L	H	H	H

1. X address enable, all rows are disabled when XE = 0
2. Y address enable, YMUX is disabled when YE = 0
3. Sense amplifier enable
4. Output enable, tri-state Flash data out bus when OE = 0
5. Defines program cycle
6. Defines erase cycle
7. Defines mass erase cycle, erase whole block
8. Defines non-volatile store cycle

Table 3-6 IFREN Truth Table

Mode	IFREN = 1	IFREN = 0
Read	Read information block	Read main memory block
Word program	Program information block	Program main memory block
Page erase	Erase information block	Erase main memory block
Mass erase	Erase both block	Erase main memory block

Table 3-7 Flash Timing Parameters

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Typ	Max	Unit	Figure
Program time	T_{prog}*	20	–	–	us	Figure 3-4
Erase time	T_{erase}*	20	–	–	ms	Figure 3-5
Mass erase time	T_{me}*	100	–	–	ms	Figure 3-6
Endurance[1]	E_{CYC}	10,000	20,000	–	cycles	
Data Retention[1]	D_{RET}	10	30	–	years	
The following parameters should only be used in the Manual Word Programming Mode						
PROG/ERASE to NVSTR set up time	T_{nvs}*	–	5	–	us	Figure 3-4, Figure 3-5, Figure 3-6
NVSTR hold time	T_{nvh}*	–	5	–	us	Figure 3-4, Figure 3-5
NVSTR hold time (mass erase)	T_{nvh1}*	–	100	–	us	Figure 3-6
NVSTR to program set up time	T_{pgs}*	–	10	–	us	Figure 3-4
Recovery time	T_{rcv}*	–	1	–	us	Figure 3-4, Figure 3-5, Figure 3-6
Cumulative program HV period[2]	T_{hv}	–	3	–	ms	Figure 3-4
Program hold time[3]	T_{pgh}	–	–	–		Figure 3-4
Address/data set up time[3]	T_{ads}	–	–	–		Figure 3-4
Address/data hold time[3]	T_{adh}	–	–	–		Figure 3-4

1. One cycle is equal to an erase program and read.

2. Thv is the cumulative high voltage programming time to the same row before next erase. The same address cannot be programmed twice before next erase.

3. Parameters are guaranteed by design in smart programming mode and must be one cycle or greater.

*The Flash interface unit provides registers for the control of these parameters.

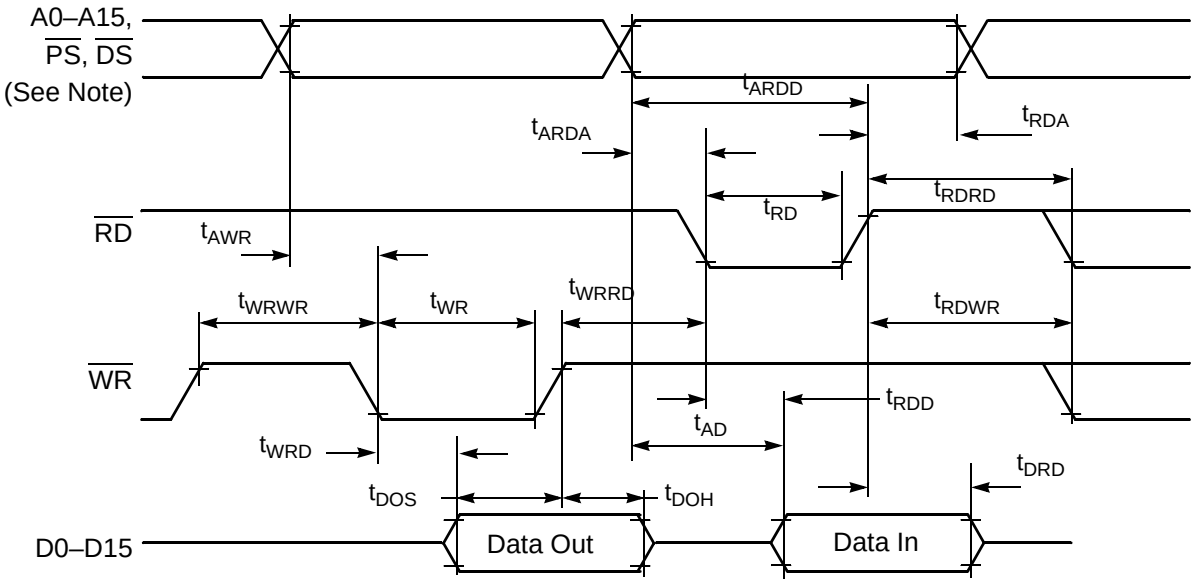
1. Timing is both wait state- and frequency-dependent. In the formulas listed, WS = the number of wait states and T = Clock Period. For 80MHz operation, T = 12.5ns.
2. Parameters listed are guaranteed by design.

To calculate the required access time for an external memory for any frequency < 80Mhz, use this formula:

Top = Clock period @ desired operating frequency

WS = Number of wait states

Memory Access Time = (Top*WS) + (Top- 11.5)



Note: During read-modify-write instructions and internal instructions, the address lines do not change state.

Figure 3-11 External Bus Asynchronous Timing

3.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 3-11 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 6]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 3-12
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 3-12
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 3-12
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 3-13
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	15T	—	ns	Figure 3-14
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	16T	—	ns	Figure 3-14
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	13T	—	ns	Figure 3-15
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	2T	—	ns	Figure 3-16
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 3-16
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 3-17
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 3-17
$\overline{\text{RSTO}}$ pulse width[5] normal operation internal reset mode	t_{RSTO}	 63ET 2,097,151ET		 ns ns	Figure 3-18

1. In the formulas, T = clock cycle. For an operating frequency of 80MHz, T = 12.5ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   • After power-on reset
   • When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125ns.
6. Parameters listed are guaranteed by design.

3.8 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure **3-22**
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure **3-22**
Clock (SCLK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figure **3-22**
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure **3-22**
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure **3-22**
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**

1. Parameters listed are guaranteed by design.

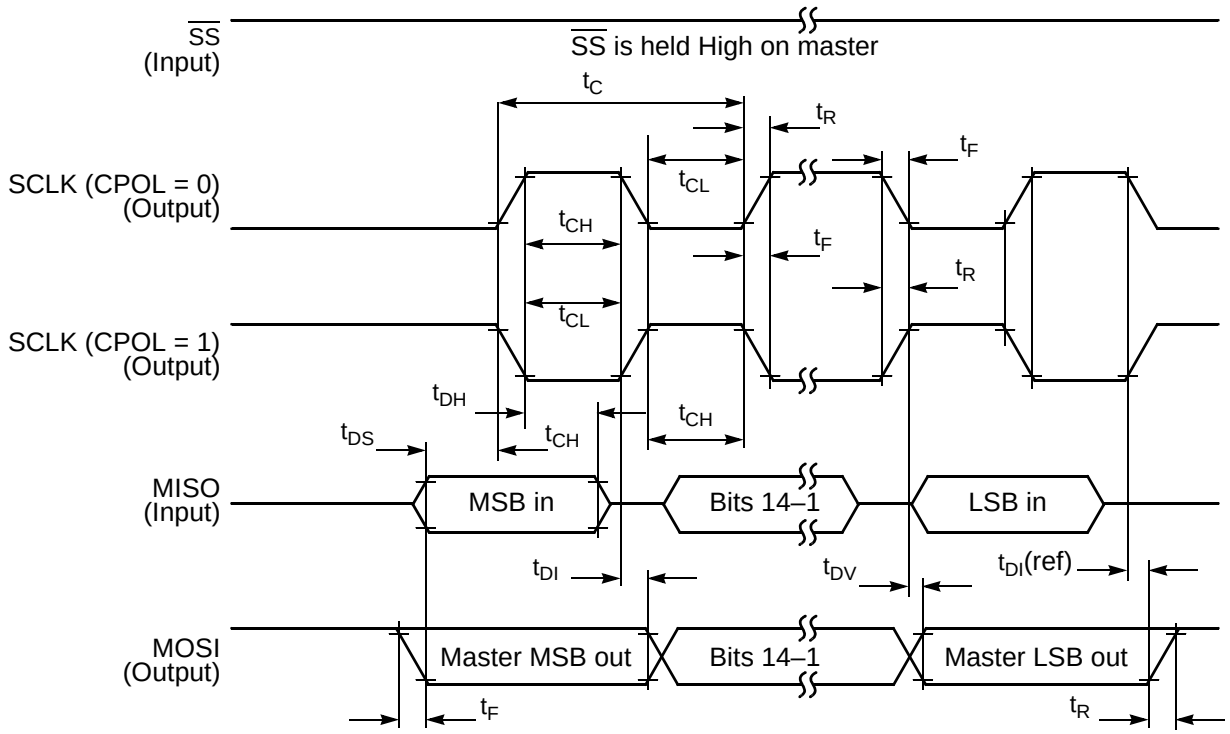


Figure 3-19 SPI Master Timing (CPHA = 0)

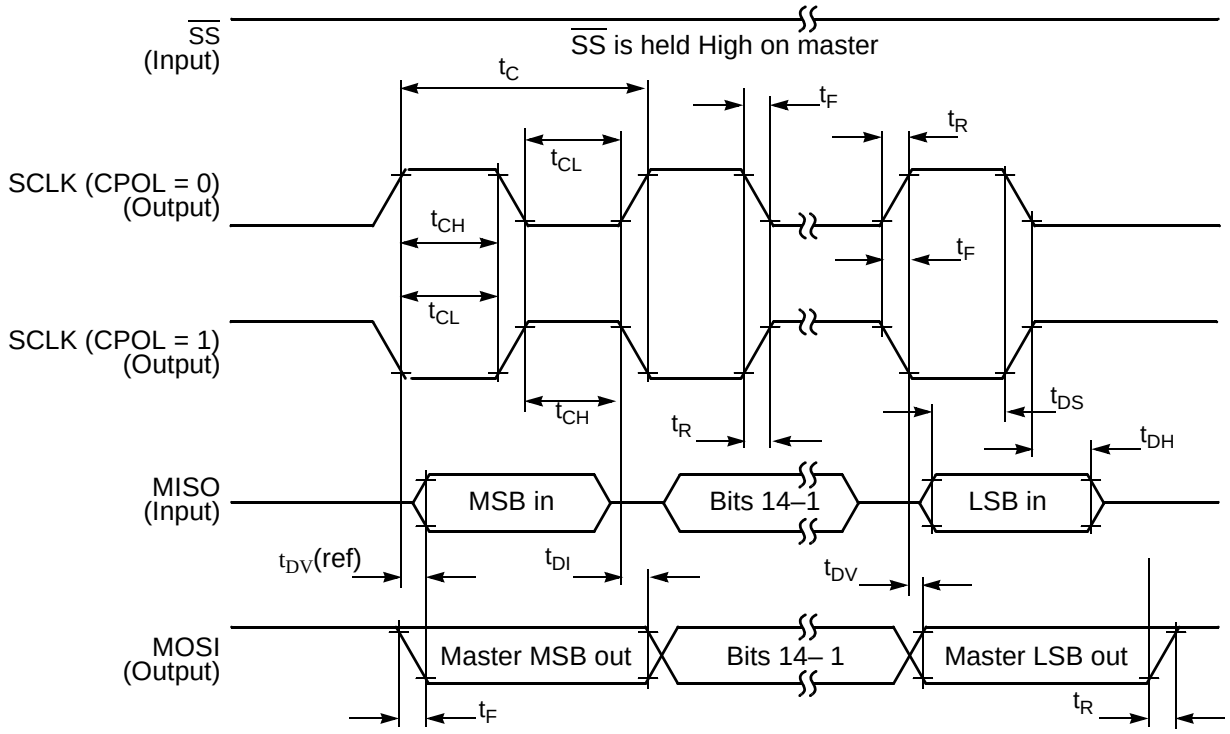


Figure 3-20 SPI Master Timing (CPHA = 1)

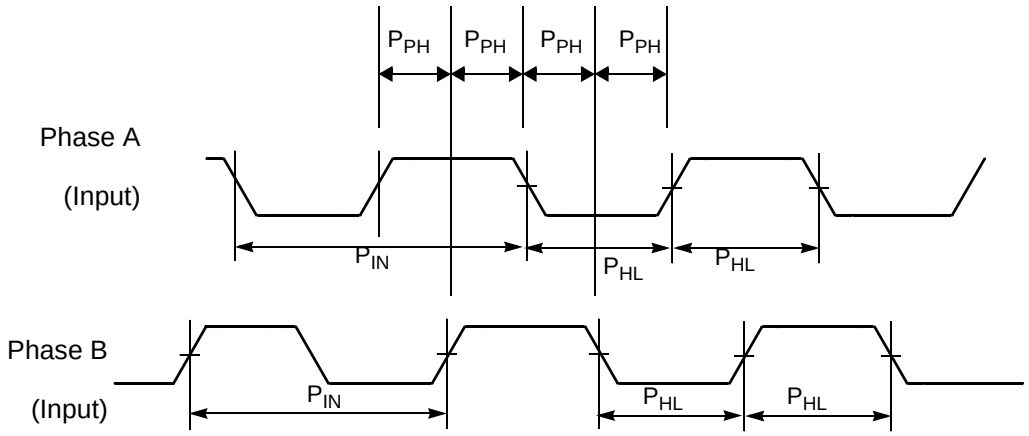


Figure 3-24 Quadrature Decoder Timing

3.11 Serial Communication Interface (SCI) Timing

Table 3-15 SCI Timing[4]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate[1]	BR	—	(f_{MAX}*2.5)/(80)	Mbps
RXD[2] Pulse Width	RXD_{PW}	0.965/BR	1.04/BR	ns
TXD[3] Pulse Width	TXD_{PW}	0.965/BR	1.04/BR	ns

1. f_{MAX} is the frequency of operation of the system clock in MHz.
2. The RXD pin in SCI0 is named RXD0 and the RXD pin in SCI1 is named RXD1.
3. The TXD pin in SCI0 is named TXD0 and the TXD pin in SCI1 is named TXD1.
4. Parameters listed are guaranteed by design.

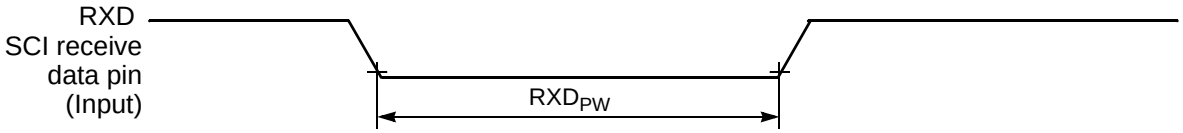
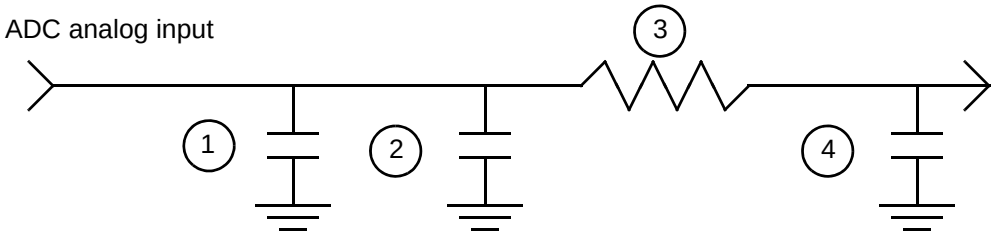


Figure 3-25 RXD Pulse Width

Table 3-16 ADC Characteristics (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ADC Quiescent Current (both ADCs)	I_{ADC}	—	50	—	mA
V_{REF} Quiescent Current (both ADCs)	I_{VREF}	—	12	16.5	mA

1. For optimum ADC performance, keep the minimum V_{ADCIN} value ≥ 25mV. Inputs less than 25mV may convert to a digital output code of 0.
2. V_{REF} must be equal to or less than V_{DDA} and must be greater than 2.7V. For optimal ADC performance, set V_{REF} to V_{DDA}-0.3V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.
6. $t_{AIC} = 1/f_{ADIC}$



1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. (1pf)

Figure 3-27 Equivalent Analog Input Circuit

3.13 Controller Area Network (CAN) Timing

Table 3-17 CAN Timing[2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, MSCAN Clock = 30MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wakeup detection [1]	T_{WAKEUP}	5	—	us

1. If Wakeup glitch filter is enabled during the design initialization and also CAN is put into Sleep mode then, any bus event (on MSCAN_RX pin) whose duration is less than 5 microseconds is filtered away. However, a valid CAN bus wakeup detection takes place for a wakeup pulse equal to or greater than 5 microseconds. The number 5 microseconds originates from the fact that the CAN wakeup message consists of 5 dominant bits at the highest possible baud rate of 1Mbps.
2. Parameters listed are guaranteed by design.

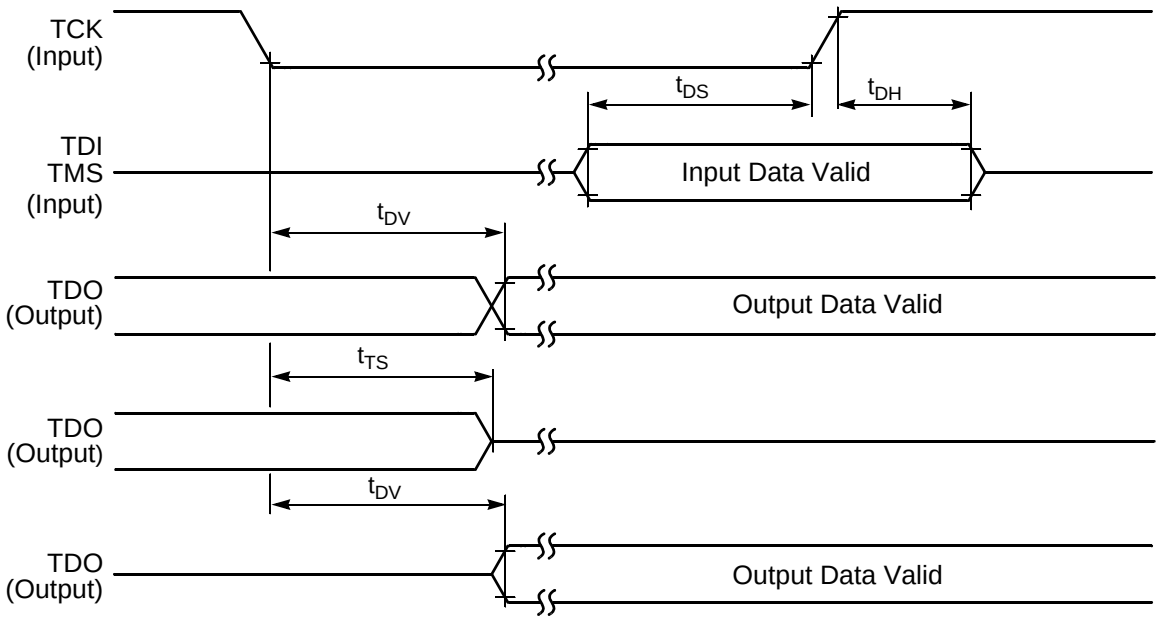


Figure 3-30 Test Access Port Timing Diagram

Figure 3-31 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-32 OnCE—Debug Event

Table 4-1 56F805 Pin Identification by Pin Number (Continued)

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
31	FAULTB1	67	FAULTA3	103	PWMA3	139	D4
32	A12	68	VREF	104	GPIOD2	140	D5
33	A13	69	ANA0	105	PWMA4	141	D6
34	V_{DD}	70	ANA1	106	PWMA5	142	D7
35	$\overline{PS}$	71	ANA2	107	TXD0	143	D8
36	$\overline{DS}$	72	ANA3	108	RXD0	144	D9

Part 5 Design Considerations

5.1 Thermal Design Considerations

An estimation of the chip junction temperature, T_J, in °C can be obtained from the equation:

Equation 1: $T_J = T_A + (P_D \times R_{\theta JA})$

Where:

T_A = ambient temperature °C
$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
P_D = power dissipation in package

Historically, thermal resistance has been expressed as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

Equation 2: $R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$

Where:

$R_{\theta JA}$ = package junction-to-ambient thermal resistance °C/W
$R_{\theta JC}$ = package junction-to-case thermal resistance °C/W
$R_{\theta CA}$ = package case-to-ambient thermal resistance °C/W

$R_{\theta JC}$ is device-related and cannot be influenced by the user. The user controls the thermal environment to change the case-to-ambient thermal resistance, $R_{\theta CA}$. For example, the user can change the air flow around the device, add a heat sink, change the mounting arrangement on the Printed Circuit Board (PCB), or otherwise change the thermal dissipation capability of the area surrounding the device on the PCB. This model is most useful for ceramic packages with heat sinks; some 90% of the heat flow is dissipated through the case to the heat sink and out to the ambient environment. For ceramic packages, in situations where the heat flow is split between a path to the case and an alternate path through the PCB, analysis of the device thermal performance may need the additional modeling capability of a system level thermal simulation tool.

The thermal performance of plastic packages is more dependent on the temperature of the PCB to which the package is mounted. Again, if the estimations obtained from $R_{\theta JA}$ do not satisfactorily answer whether the thermal performance is adequate, a system level model may be appropriate.

Definitions:

A complicating factor is the existence of three common definitions for determining the junction-to-case thermal resistance in plastic packages:

- Measure the thermal resistance from the junction to the outside surface of the package (case) closest to the chip mounting area when that surface has a proper heat sink. This is done to minimize temperature variation across the surface.
- Measure the thermal resistance from the junction to where the leads are attached to the case. This definition is approximately equal to a junction to board thermal resistance.

- Because the processor's output signals have fast rise and fall times, PCB trace lengths should be minimal.
- Consider all device loads as well as parasitic capacitance due to PCB traces when calculating capacitance. This is especially critical in systems with higher capacitive loads that could create higher transient currents in the V_{DD} and V_{SS} circuits.
- Take special care to minimize noise levels on the V_{REF}, V_{DDA} and V_{SSA} pins.
- Designs that utilize the $\overline{\text{TRST}}$ pin for JTAG port or OnCE module functionality (such as development or debugging systems) should allow a means to assert $\overline{\text{TRST}}$ whenever $\overline{\text{RESET}}$ is asserted, as well as a means to assert $\overline{\text{TRST}}$ independently of $\overline{\text{RESET}}$. $\overline{\text{TRST}}$ must be asserted at power up for proper operation. Designs that do not require debugging functionality, such as consumer products, $\overline{\text{TRST}}$ should be tied low.
- TRST must be externally asserted even when the user relies on the internal power on reset for functional test purposes.
- Because the Flash memory is programmed through the JTAG/OnCE port, designers should provide an interface to this port to allow in-circuit Flash programming.

How to Reach Us:

Home Page:
www.freescale.com

E-mail:
support@freescale.com

USA/Europe or Locations Not Listed:
Freescale Semiconductor
Technical Information Center, CH370
1300 N. Alma School Road
Chandler, Arizona 85224
+1-800-521-6274 or +1-480-768-2130
support@freescale.com

Europe, Middle East, and Africa:
Freescale Halbleiter Deutschland GmbH
Technical Information Center
Schatzbogen 7
81829 Muenchen, Germany
+44 1296 380 456 (English)
+46 8 52200080 (English)
+49 89 92103 559 (German)
+33 1 69 35 48 48 (French)
support@freescale.com

Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064, Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

Asia/Pacific:
Freescale Semiconductor Hong Kong Ltd.
Technical Information Center
2 Dai King Street
Tai Po Industrial Estate
Tai Po, N.T., Hong Kong
+800 2666 8080
support.asia@freescale.com

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