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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

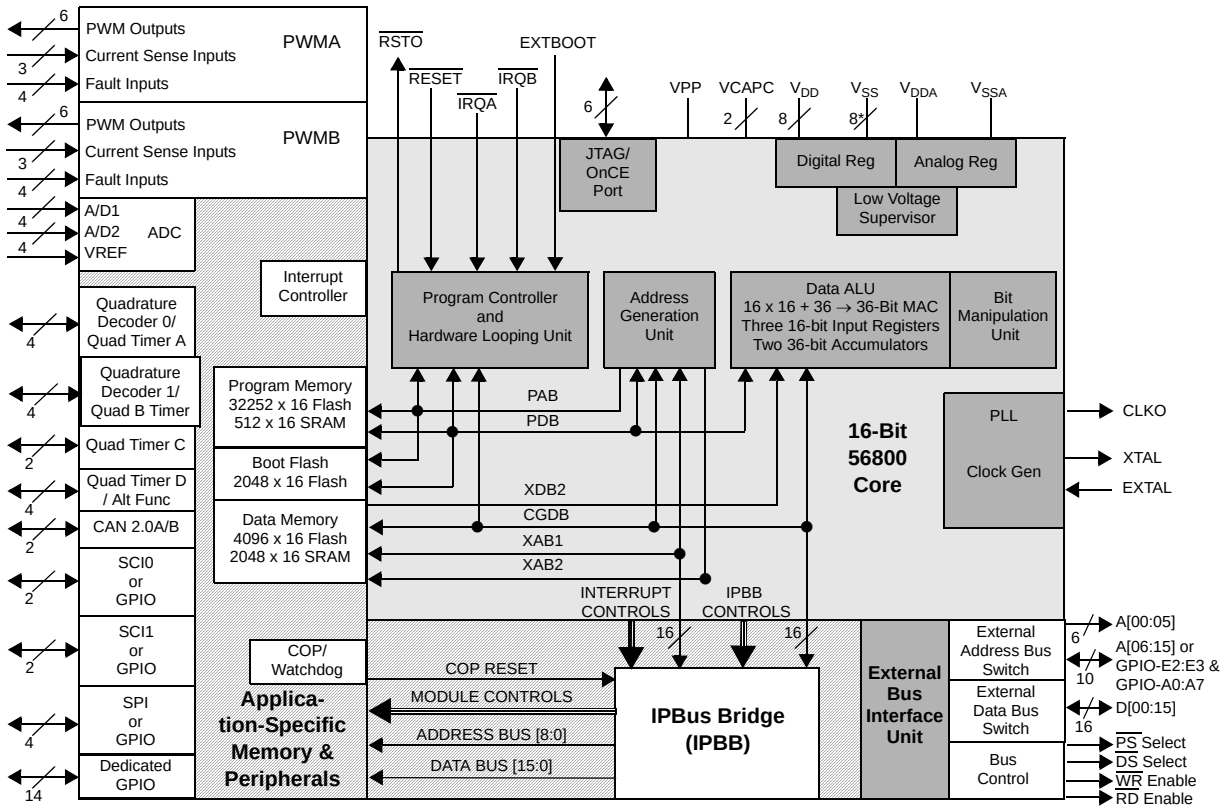
Details	
Product Status	Active
Core Processor	56800
Core Size	16-Bit
Speed	80MHz
Connectivity	CANbus, EBI/EMI, SCI, SPI
Peripherals	POR, PWM, WDT
Number of I/O	32
Program Memory Size	64KB (32K x 16)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 16
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/dsp56f805fv80e

Document Revision History

Version History	Description of Change
Rev. 16	Added revision history. Added this text to footnote 2 in **Table 3-8**: “However, the high pulse width does not have to be any particular percent of the low pulse width.”

56F805 General Description

- Up to 40 MIPS at 80MHz core frequency
- DSP and MCU functionality in a unified, C-efficient architecture
- Hardware DO and REP loops
- MCU-friendly instruction set supports both DSP and controller functions: MAC, bit manipulation unit, 14 addressing modes
- 31.5K × 16-bit words (64KB) Program Flash
- 512 × 16-bit words (1KB) Program RAM
- 4K × 16-bit words (8KB) Data Flash
- 2K × 16-bit words (4KB) Data RAM
- 2K × 16-bit words (4KB) Boot Flash
- Up to 64K × 16-bit words (128KB) each of external Program and Data memory
- Two 6-channel PWM Modules
- Two 4-channel, 12-bit ADCs
- Two Quadrature Decoders
- CAN 2.0 B Module
- Two Serial Communication Interfaces (SCIs)
- Serial Peripheral Interface (SPI)
- Up to four General Purpose Quad Timers
- JTAG/OnCE™ port for debugging
- 14 Dedicated and 18 Shared GPIO lines
- 144-pin LQFP Package



56F805 Block Diagram

*includes TCS pin which is reserved for factory use and is tied to VSS

Table 3-2 Recommended Operating Conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Voltage difference V_{DD} to V_{DDA}	ΔV_{DD}	-0.1	-	0.1	V
Voltage difference V_{SS} to V_{SSA}	ΔV_{SS}	-0.1	-	0.1	V
ADC reference voltage	VREF	2.7	–	V_{DDA}	V
Ambient operating temperature	T_A	–40	–	85	°C

Table 3-3 Thermal Characteristics[6]

Characteristic	Comments	Symbol	Value	Unit	Notes
			144-pin LQFP		
Junction to ambient Natural convection		$R_{\theta JA}$	47.1	°C/W	2
Junction to ambient (@1m/sec)		$R_{\theta JMA}$	43.8	°C/W	2
Junction to ambient Natural convection	Four layer board (2s2p)	$R_{\theta JMA}$ (2s2p)	40.8	°C/W	1,2
Junction to ambient (@1m/sec)	Four layer board (2s2p)	$R_{\theta JMA}$	39.2	°C/W	1,2
Junction to case		$R_{\theta JC}$	11.8	°C/W	3
Junction to center of case		Ψ_{JT}	1	°C/W	4, 5
I/O pin power dissipation		$P_{I/O}$	User Determined	W	
Power dissipation		P_D	$P_D = (I_{DD} \times V_{DD} + P_{I/O})$	W	
Junction to center of case		P_{DMAX}	(TJ - TA) /RθJA	W	7

Notes:

1. Theta-JA determined on 2s2p test boards is frequently lower than would be observed in an application. Determined on 2s2p thermal test board.
2. Junction to ambient thermal resistance, Theta-JA ($R_{\theta JA}$) was simulated to be equivalent to the JEDEC specification JESD51-2 in a horizontal configuration in natural convection. Theta-JA was also simulated on a thermal test board with two internal planes (2s2p where “s” is the number of signal layers and “p” is the number of planes) per JESD51-6 and JESD51-7. The correct name for Theta-JA for forced convection or with the non-single layer boards is Theta-JMA.
3. Junction to case thermal resistance, Theta-JC ($R_{\theta JC}$), was simulated to be equivalent to the measured values using the cold plate technique with the cold plate temperature used as the “case” temperature. The basic cold plate measurement technique is described by MIL-STD 883D, Method 1012.1. This is the correct thermal metric to use to calculate thermal performance when the package is being used with a heat sink.

Table 3-4 DC Electrical Characteristics (Continued)

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{op} = 80$MHz

Characteristic	Symbol	Min	Typ	Max	Unit
Output Low Voltage (at IOL)	V_{OL}	—	—	0.4	V
Output source current	I_{OH}	4	—	—	mA
Output sink current	I_{OL}	4	—	—	mA
PWM pin output source current[3]	I_{OHP}	10	—	—	mA
PWM pin output sink current[4]	I_{OLP}	16	—	—	mA
Input capacitance	C_{IN}	—	8	—	pF
Output capacitance	C_{OUT}	—	12	—	pF
V_{DD} supply current	I_{DDT}[5]				
Run [6]		—	126	152	mA
Wait[7]		—	105	129	mA
Stop		—	60	84	mA
Low Voltage Interrupt, external power supply[8]	V_{EIO}	2.4	2.7	3.0	V
Low Voltage Interrupt, internal power supply[9]	V_{EIC}	2.0	2.2	2.4	V
Power on Reset[10]	V_{POR}	—	1.7	2.0	V

1. Schmitt Trigger inputs are: EXTBOOT, IRQA, IRQB, RESET, ISA0-2, FAULTA0-3, ISB0-2, FAULT0B-3, TCS, TCK, TRST, TMS, TDI, and MSCAN_RX

2. Analog inputs are: ANA[0:7], XTAL and EXTAL. Specification assumes ADC is not sampling.

3. PWM pin output source current measured with 50% duty cycle.

4. PWM pin output sink current measured with 50% duty cycle.

5. $I_{DDT} = I_{DD} + I_{DDA}$ (Total supply current for $V_{DD} + V_{DDA}$)

6. Run (operating) I_{DD} measured using 8MHz clock source. All inputs 0.2V from rail; outputs unloaded. All ports configured as inputs; measured with all modules enabled.

7. Wait I_{DD} measured using external square wave clock source (f_{osc} = 8MHz) into XTAL; all inputs 0.2V from rail; no DC loads; less than 50pF on all outputs. C_L = 20pF on EXTAL; all ports configured as inputs; EXTAL capacitance linearly affects wait I_{DD}; measured with PLL enabled.

8. This low voltage interrupt monitors the V_{DDA} external power supply. V_{DDA} is generally connected to the same potential as V_{DD} via separate traces. If V_{DDA} drops below V_{EIO}, an interrupt is generated. Functionality of the device is guaranteed under transient conditions when $V_{DDA} \geq V_{EIO}$ (between the minimum specified V_{DD} and the point when the V_{EIO} interrupt is generated).

9. This low voltage interrupt monitors the internally regulated core power supply. If the output from the internal voltage is regulator drops below V_{EIC}, an interrupt is generated. Since the core logic supply is internally regulated, this interrupt will not be generated unless the external power supply drops below the minimum specified value (3.0V).

10. Power–on reset occurs whenever the internally regulated 2.5V digital supply drops below 1.5V typical. While power is ramping up, this signal remains active as long as the internal 2.5V is below 1.5V typical, no matter how long the ramp-up rate is. The internally regulated voltage is typically 100mV less than V_{DD} during ramp-up until 2.5V is reached, at which time it self-regulates.

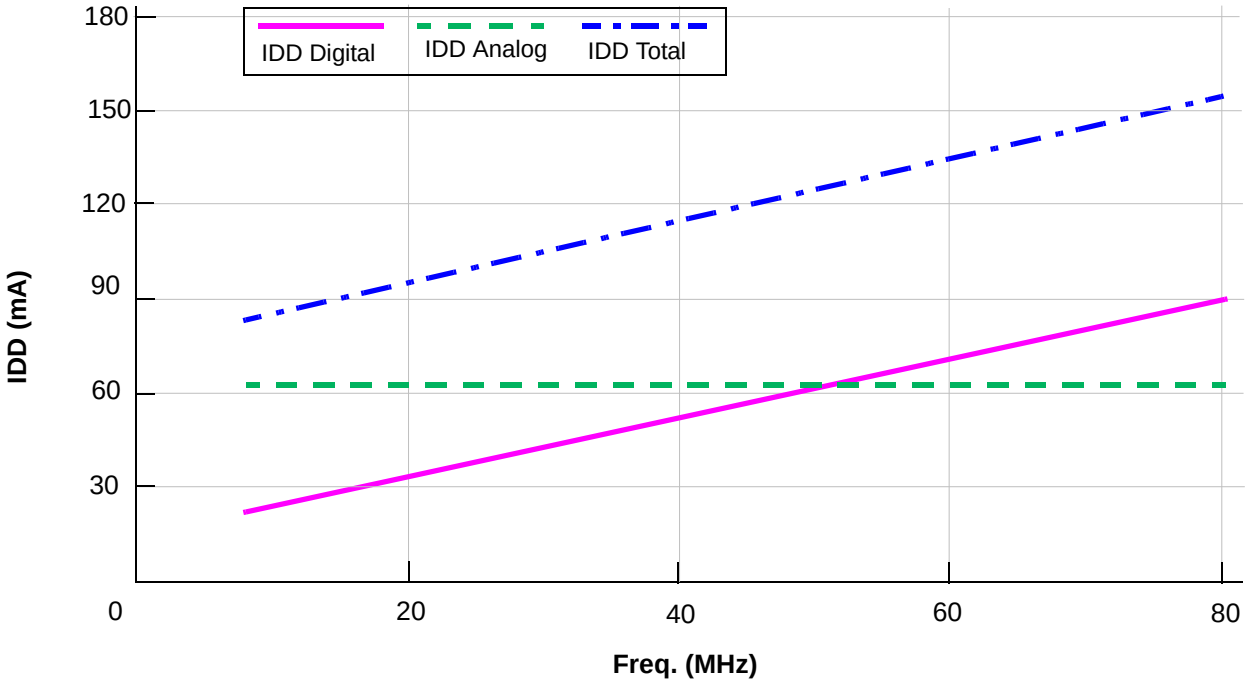
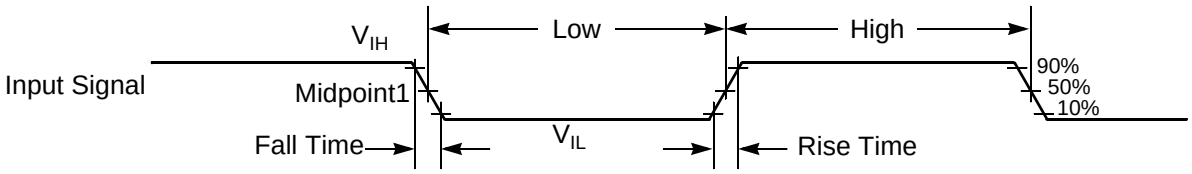


Figure 3-1 Maximum Run IDD vs. Frequency (see Note 6. in Figure 3-14)

3.3 AC Electrical Characteristics

Timing waveforms in Section 3.3 are tested using the V_{IL} and V_{IH} levels specified in the DC Characteristics table. In Figure 3-2 the levels of V_{IH} and V_{IL} for an input signal are shown.



Note: The midpoint is $V_{IL} + (V_{IH} - V_{IL})/2$.

Figure 3-2 Input Signal Measurement References

Figure 3-3 shows the definitions of the following signal states:

- Active state, when a bus or signal is driven, and enters a low impedance state
- Tri-stated, when a bus or signal is placed in a high impedance state
- Data Valid state, when a signal level has reached V_{OL} or V_{OH}
- Data Invalid state, when a signal level is in transition between V_{OL} and V_{OH}

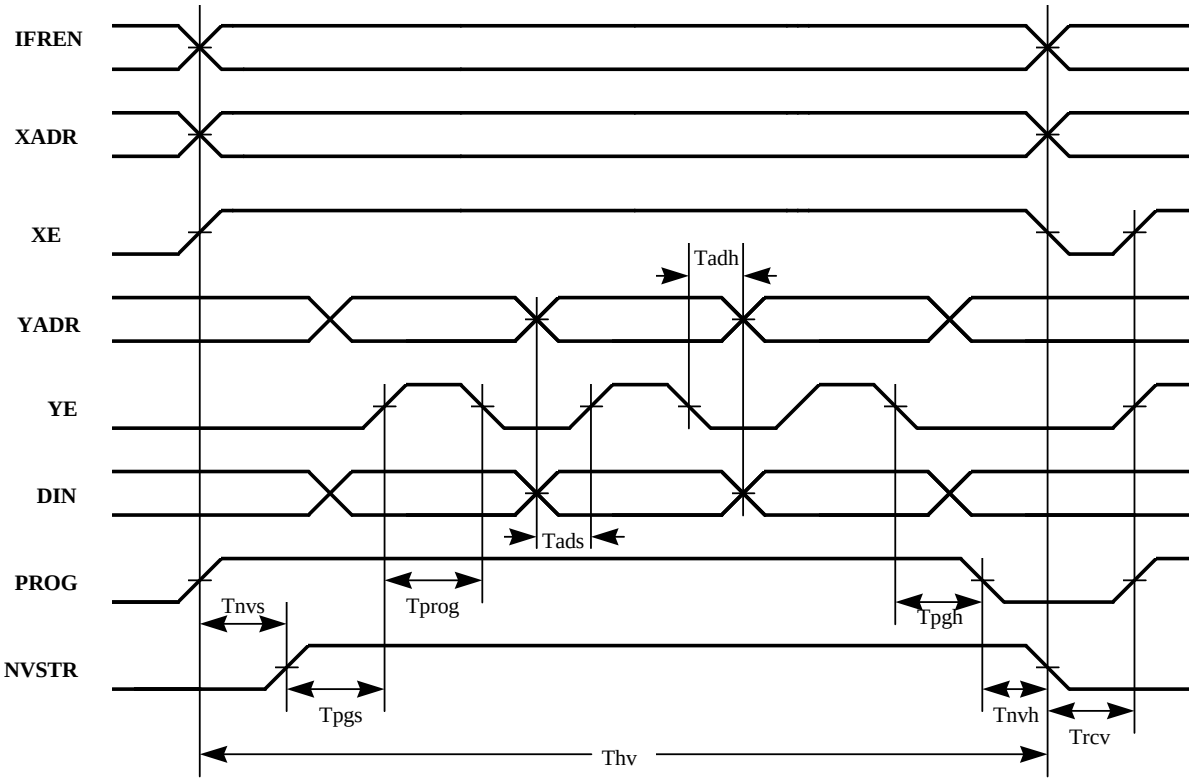


Figure 3-4 Flash Program Cycle

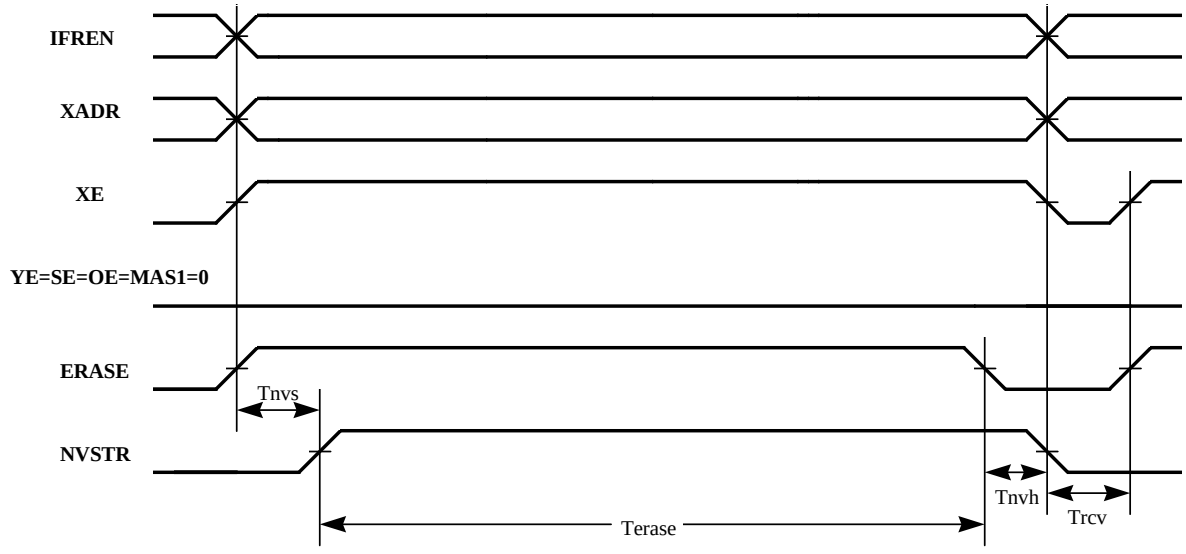


Figure 3-5 Flash Erase Cycle

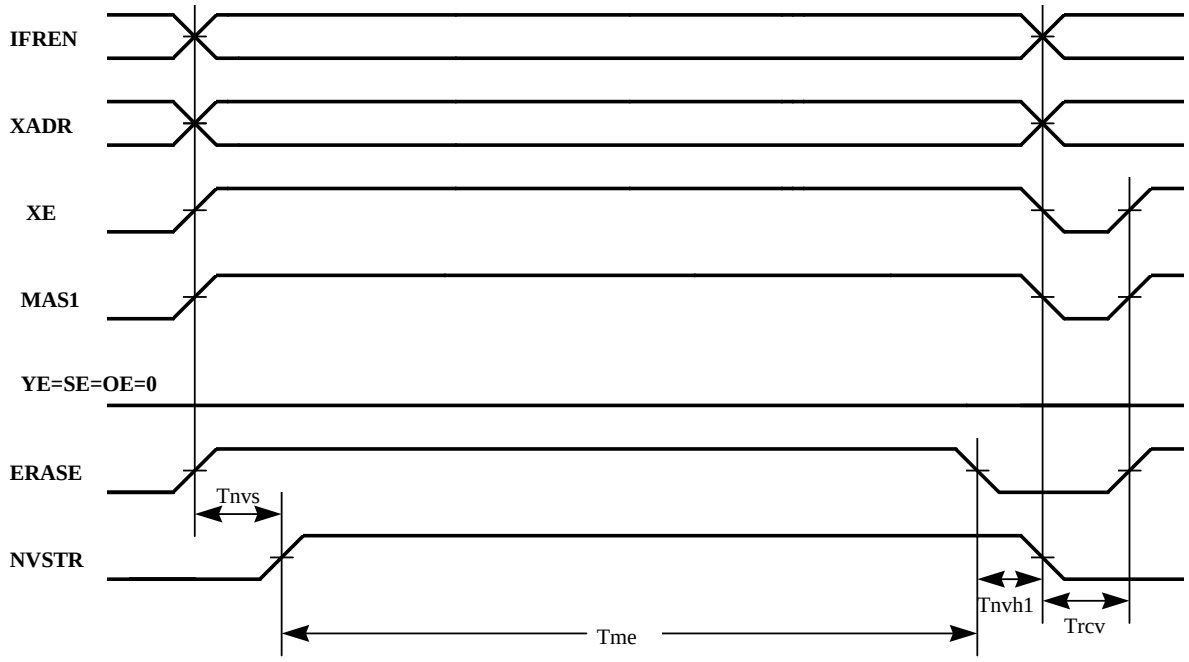


Figure 3-6 Flash Mass Erase Cycle

3.5 External Clock Operation

The 56F805 system clock can be derived from a crystal or an external system clock signal. To generate a reference frequency using the internal oscillator, a reference crystal must be connected between the EXTAL and XTAL pins.

3.5.1 Crystal Oscillator

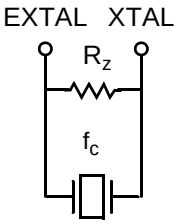
The internal oscillator is also designed to interface with a parallel-resonant crystal resonator in the frequency range specified for the external crystal in **Table 3-9**. In **Figure 3-7** a recommended crystal oscillator circuit is shown. Follow the crystal supplier's recommendations when selecting a crystal, because crystal parameters determine the component values required to provide maximum stability and reliable start-up. The crystal and associated components should be mounted as close as possible to the EXTAL and XTAL pins to minimize output distortion and start-up stabilization time. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-8**, no external load capacitors should be used.

The 56F80x components internally are modeled as a parallel resonant oscillator circuit to provide a capacitive load on each of the oscillator pins (XTAL and EXTAL) of 10pF to 13pF over temperature and process variations. Using a typical value of internal capacitance on these pins of 12pF and a value of 3pF

as a typical circuit board trace capacitance the parallel load capacitance presented to the crystal is 9pF as determined by the following equation:

$$CL = \frac{CL1 * CL2}{CL1 + CL2} + Cs = \frac{12 * 12}{12 + 12} + 3 = 6 + 3 = 9pF$$

This is the value load capacitance that should be used when selecting a crystal and determining the actual frequency of operation of the crystal oscillator circuit.

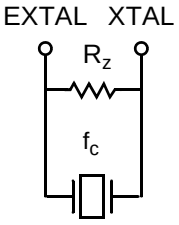


Recommended External Crystal Parameters:
R_z = 1 to 3 MΩ
f_c = 8MHz (optimized for 8MHz)

Figure 3-7 Connecting to a Crystal Oscillator

3.5.2 Ceramic Resonator

It is also possible to drive the internal oscillator with a ceramic resonator, assuming the overall system design can tolerate the reduced signal integrity. In **Figure 3-8**, a typical ceramic resonator circuit is shown. Refer to supplier's recommendations when selecting a ceramic resonator and associated components. The resonator and components should be mounted as close as possible to the EXTAL and XTAL pins. The internal 56F80x oscillator circuitry is designed to have no external load capacitors present. As shown in **Figure 3-7** no external load capacitors should be used.



Recommended Ceramic Resonator Parameters:
R_z = 1 to 3 MΩ
f_c = 8MHz (optimized for 8MHz)

Figure 3-8 Connecting a Ceramic Resonator

Note: Freescale recommends only two terminal ceramic resonators vs. three terminal resonators (which contain an internal bypass capacitor to ground).

3.5.3 External Clock Source

The recommended method of connecting an external clock is given in **Figure 3-9**. The external clock source is connected to XTAL and the EXTAL pin is grounded.

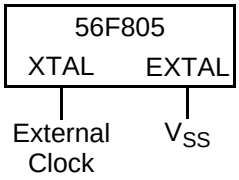


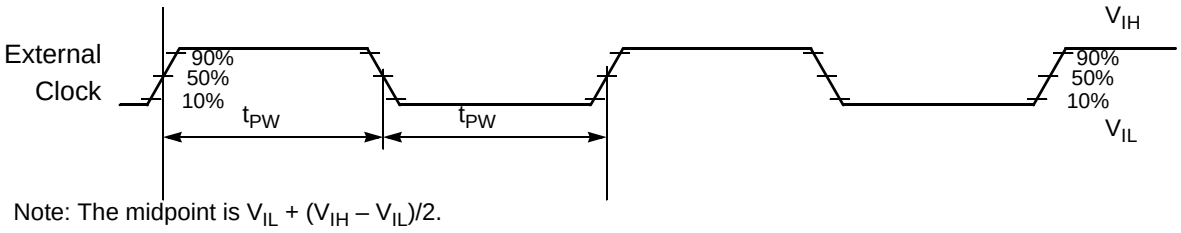
Figure 3-9 Connecting an External Clock Signal

Table 3-8 External Clock Operation Timing Requirements[3]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°$C

Characteristic	Symbol	Min	Typ	Max	Unit
Frequency of operation (external clock driver)[1]	f_{osc}	0	—	80	MHz
Clock Pulse Width[2, 5]	t_{PW}	6.25	—	—	ns

1. See **Figure 3-9** for details on using the recommended connection of an external clock driver.
2. The high or low pulse width must be no smaller than 6.25ns or the chip will not function. However, the high pulse width does not have to be any particular percent of the low pulse width.
3. Parameters listed are guaranteed by design.



Note: The midpoint is $V_{IL} + (V_{IH} – V_{IL})/2$.

Figure 3-10 External Clock Timing

3.5.4 Phase Locked Loop Timing

Table 3-9 PLL Timing

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$V, $T_A = –40°$ to $+85°C$

Characteristic	Symbol	Min	Typ	Max	Unit
External reference crystal frequency for the PLL[1]	f_{osc}	4	8	10	MHz
PLL output frequency[2]	$f_{out}/2$	40	—	110	MHz
PLL stabilization time [3] 0^o to $+85^oC$	t_{plls}	—	1	10	ms
PLL stabilization time[3] -40^o to 0^oC	t_{plls}	—	100	200	ms

1. An externally supplied reference clock should be as free as possible from any phase jitter for the PLL to work correctly. The PLL is optimized for 8MHz input crystal.

2. ZCLK may not exceed 80MHz. For additional information on ZCLK and $f_{out}/2$, please refer to the OCCS chapter in the User Manual. ZCLK = f_{op}

3. This is the minimum time required after the PLL set-up is changed to ensure reliable operation.

3.7 Reset, Stop, Wait, Mode Select, and Interrupt Timing

Table 3-11 Reset, Stop, Wait, Mode Select, and Interrupt Timing[1, 6]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF

Characteristic	Symbol	Min	Max	Unit	See Figure
$\overline{\text{RESET}}$ Assertion to Address, Data and Control Signals High Impedance	t_{RAZ}	—	21	ns	Figure 3-12
Minimum $\overline{\text{RESET}}$ Assertion Duration[2] OMR Bit 6 = 0 OMR Bit 6 = 1	t_{RA}	 275,000T 128T	 — —	 ns ns	Figure 3-12
$\overline{\text{RESET}}$ Deassertion to First External Address Output	t_{RDA}	33T	34T	ns	Figure 3-12
Edge-sensitive Interrupt Request Width	t_{IRW}	1.5T	—	ns	Figure 3-13
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to External Data Memory Access Out Valid, caused by first instruction execution in the interrupt service routine	t_{IDM}	15T	—	ns	Figure 3-14
$\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to General Purpose Output Valid, caused by first instruction execution in the interrupt service routine	t_{IG}	16T	—	ns	Figure 3-14
$\overline{\text{IRQA}}$ Low to First Valid Interrupt Vector Address Out recovery from Wait State[3]	t_{IRI}	13T	—	ns	Figure 3-15
$\overline{\text{IRQA}}$ Width Assertion to Recover from Stop State[4]	t_{IW}	2T	—	ns	Figure 3-16
Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of first instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IF}	 — —	 275,000T 12T	 ns ns	Figure 3-16
Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Cause the Fetch of First $\overline{\text{IRQA}}$ Interrupt Instruction (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{IRQ}	 — —	 275,000T 12T	 ns ns	Figure 3-17
Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to First Interrupt Vector Address Out Valid (exiting Stop) OMR Bit 6 = 0 OMR Bit 6 = 1	t_{II}	 — —	 275,000T 12T	 ns ns	Figure 3-17
$\overline{\text{RSTO}}$ pulse width[5] normal operation internal reset mode	t_{RSTO}	 63ET 2,097,151ET		 ns ns	Figure 3-18

1. In the formulas, T = clock cycle. For an operating frequency of 80MHz, T = 12.5ns.
2. Circuit stabilization delay is required during reset when using an external clock or crystal oscillator in two cases:
   • After power-on reset
   • When recovering from Stop state
3. The minimum is specified for the duration of an edge-sensitive IRQA interrupt required to recover from the Stop state. This is not the minimum required so that the IRQA interrupt is accepted.
4. The interrupt instruction fetch is visible on the pins only in Mode 3.
5. ET = External Clock period, For an external crystal frequency of 8MHz, ET=125ns.
6. Parameters listed are guaranteed by design.

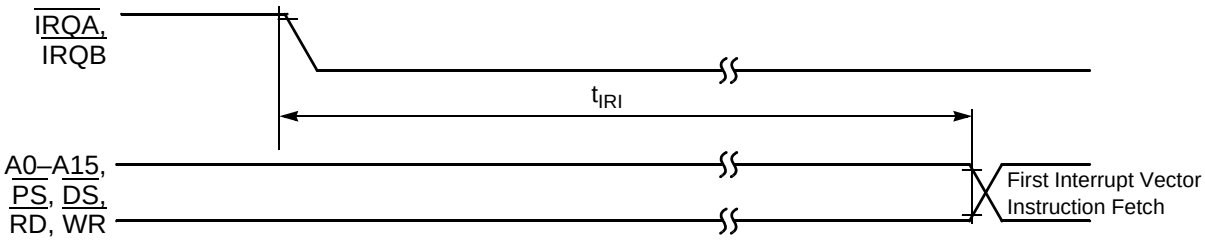


Figure 3-15 Interrupt from Wait State Timing

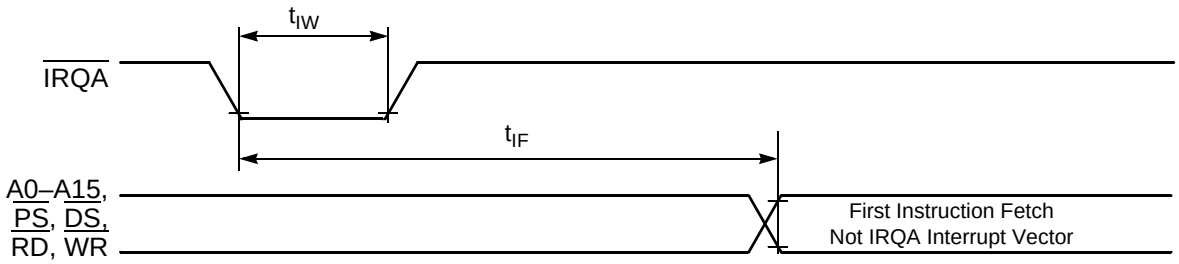


Figure 3-16 Recovery from Stop State Using Asynchronous Interrupt Timing

Figure 3-17 Recovery from Stop State Using IRQA Interrupt Service

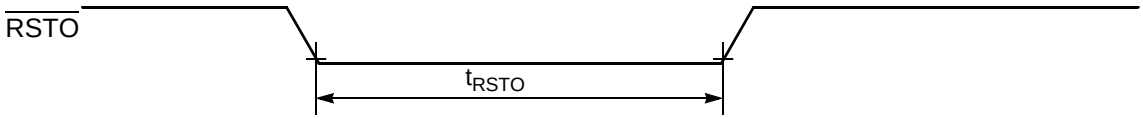


Figure 3-18 Reset Output Timing

3.8 Serial Peripheral Interface (SPI) Timing

Table 3-12 SPI Timing[1]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, $f_{OP} = 80$MHz

Characteristic	Symbol	Min	Max	Unit	See Figure
Cycle time Master Slave	t_C	 50 25	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Enable lead time Master Slave	t_{ELD}	 — 25	 — —	 ns ns	Figure **3-22**
Enable lag time Master Slave	t_{ELG}	 — 100	 — —	 ns ns	Figure **3-22**
Clock (SCLK) high time Master Slave	t_{CH}	 17.6 12.5	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Clock (SCLK) low time Master Slave	t_{CL}	 24.1 25	 — —	 ns ns	Figure **3-22**
Data set-up time required for inputs Master Slave	t_{DS}	 20 0	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Data hold time required for inputs Master Slave	t_{DH}	 0 2	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Access time (time to data active from high-impedance state) Slave	t_A	 4.8	 15	 ns	Figure **3-22**
Disable time (hold time to high-impedance state) Slave	t_D	 3.7	 15.2	 ns	Figure **3-22**
Data Valid for outputs Master Slave (after enable edge)	t_{DV}	 — —	 4.5 20.4	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Data invalid Master Slave	t_{DI}	 0 0	 — —	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Rise time Master Slave	t_R	 — —	 11.5 10.0	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**
Fall time Master Slave	t_F	 — —	 9.7 9.0	 ns ns	Figures **3-19**, **3-20**, **3-21**, **3-22**

1. Parameters listed are guaranteed by design.

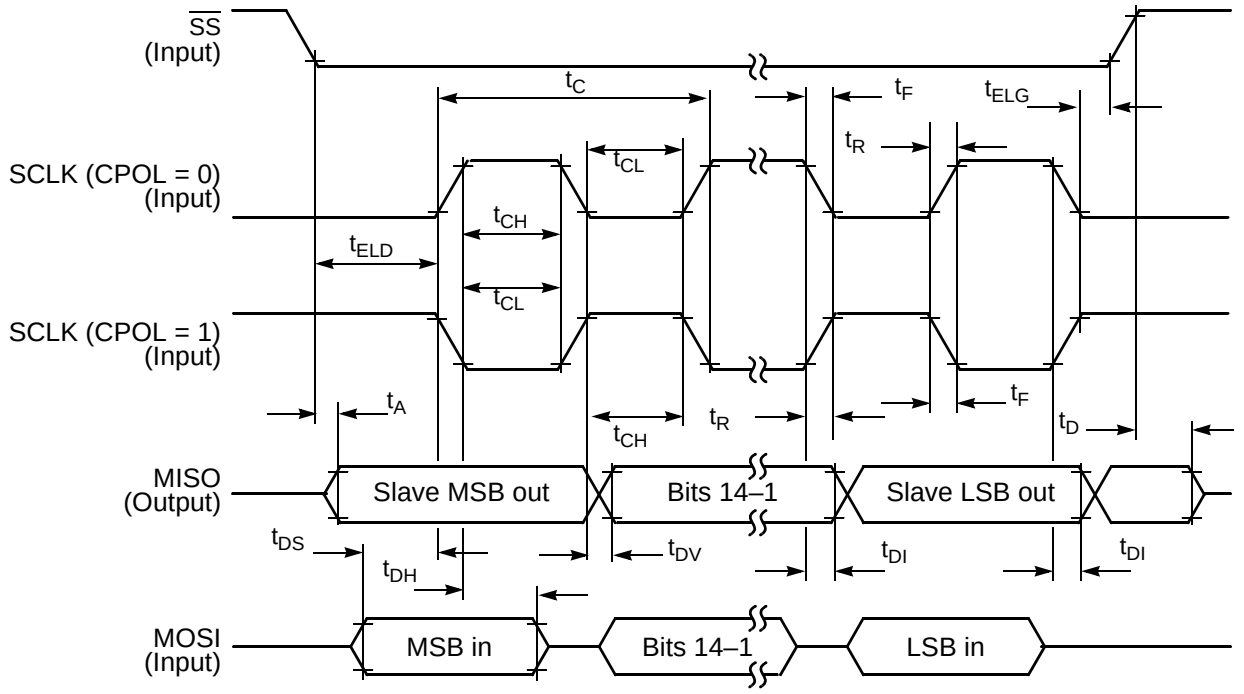


Figure 3-21 SPI Slave Timing (CPHA = 0)

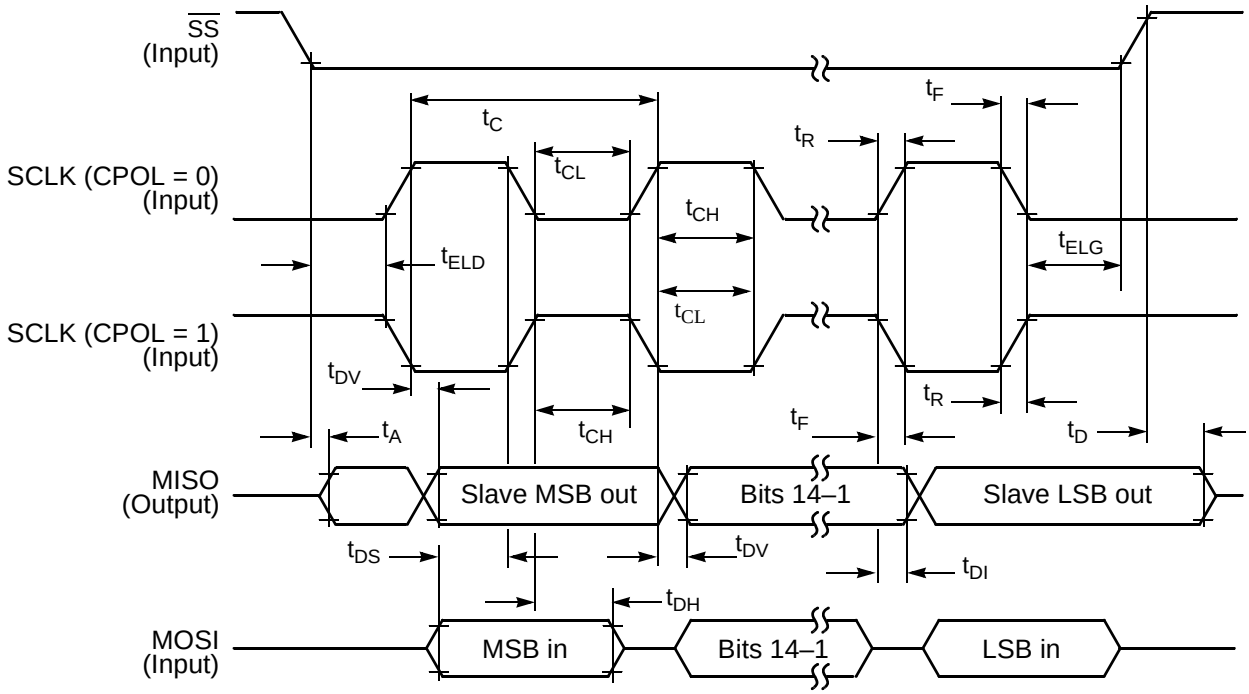
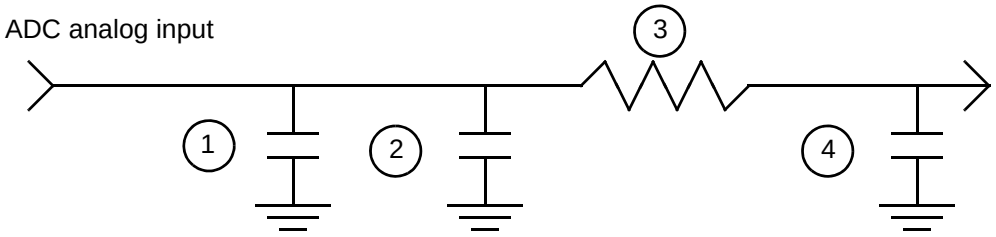


Figure 3-22 SPI Slave Timing (CPHA = 1)

Table 3-16 ADC Characteristics (Continued)

Characteristic	Symbol	Min	Typ	Max	Unit
ADC Quiescent Current (both ADCs)	I_{ADC}	—	50	—	mA
V_{REF} Quiescent Current (both ADCs)	I_{VREF}	—	12	16.5	mA

1. For optimum ADC performance, keep the minimum V_{ADCIN} value ≥ 25mV. Inputs less than 25mV may convert to a digital output code of 0.
2. V_{REF} must be equal to or less than V_{DDA} and must be greater than 2.7V. For optimal ADC performance, set V_{REF} to V_{DDA}-0.3V.
3. Measured in 10-90% range.
4. LSB = Least Significant Bit.
5. Guaranteed by characterization.
6. $t_{AIC} = 1/f_{ADIC}$



1. Parasitic capacitance due to package, pin to pin, and pin to package base coupling. (1.8pf)
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing. (2.04pf)
3. Equivalent resistance for the ESD isolation resistor and the channel select mux. (500 ohms)
4. Sampling capacitor at the sample and hold circuit. (1pf)

Figure 3-27 Equivalent Analog Input Circuit

3.13 Controller Area Network (CAN) Timing

Table 3-17 CAN Timing[2]

Operating Conditions: $V_{SS} = V_{SSA} = 0$ V, $V_{DD} = V_{DDA} = 3.0–3.6$ V, $T_A = –40°$ to $+85°C$, $C_L \leq 50$pF, MSCAN Clock = 30MHz

Characteristic	Symbol	Min	Max	Unit
Baud Rate	BR_{CAN}	—	1	Mbps
Bus Wakeup detection [1]	T_{WAKEUP}	5	—	us

1. If Wakeup glitch filter is enabled during the design initialization and also CAN is put into Sleep mode then, any bus event (on MSCAN_RX pin) whose duration is less than 5 microseconds is filtered away. However, a valid CAN bus wakeup detection takes place for a wakeup pulse equal to or greater than 5 microseconds. The number 5 microseconds originates from the fact that the CAN wakeup message consists of 5 dominant bits at the highest possible baud rate of 1Mbps.
2. Parameters listed are guaranteed by design.

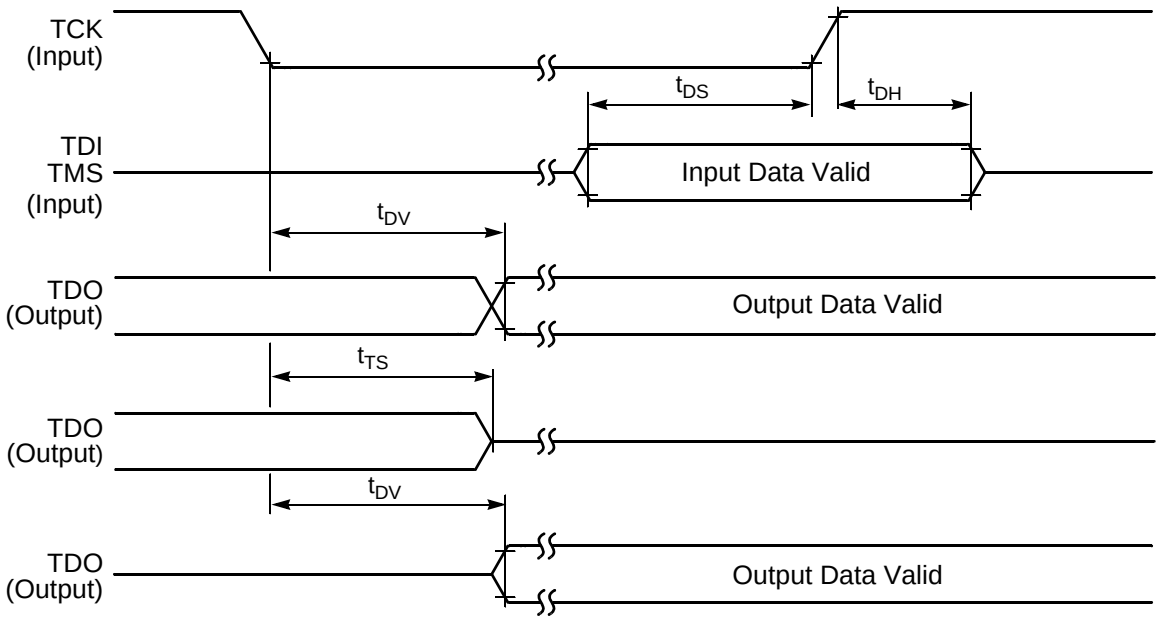


Figure 3-30 Test Access Port Timing Diagram

Figure 3-31 $\overline{\text{TRST}}$ Timing Diagram

Figure 3-32 OnCE—Debug Event

Part 4 Packaging

4.1 Package and Pin-Out Information 56F805

This section contains package and pin-out information for the 144-pin LQFP configuration of the 56F805.

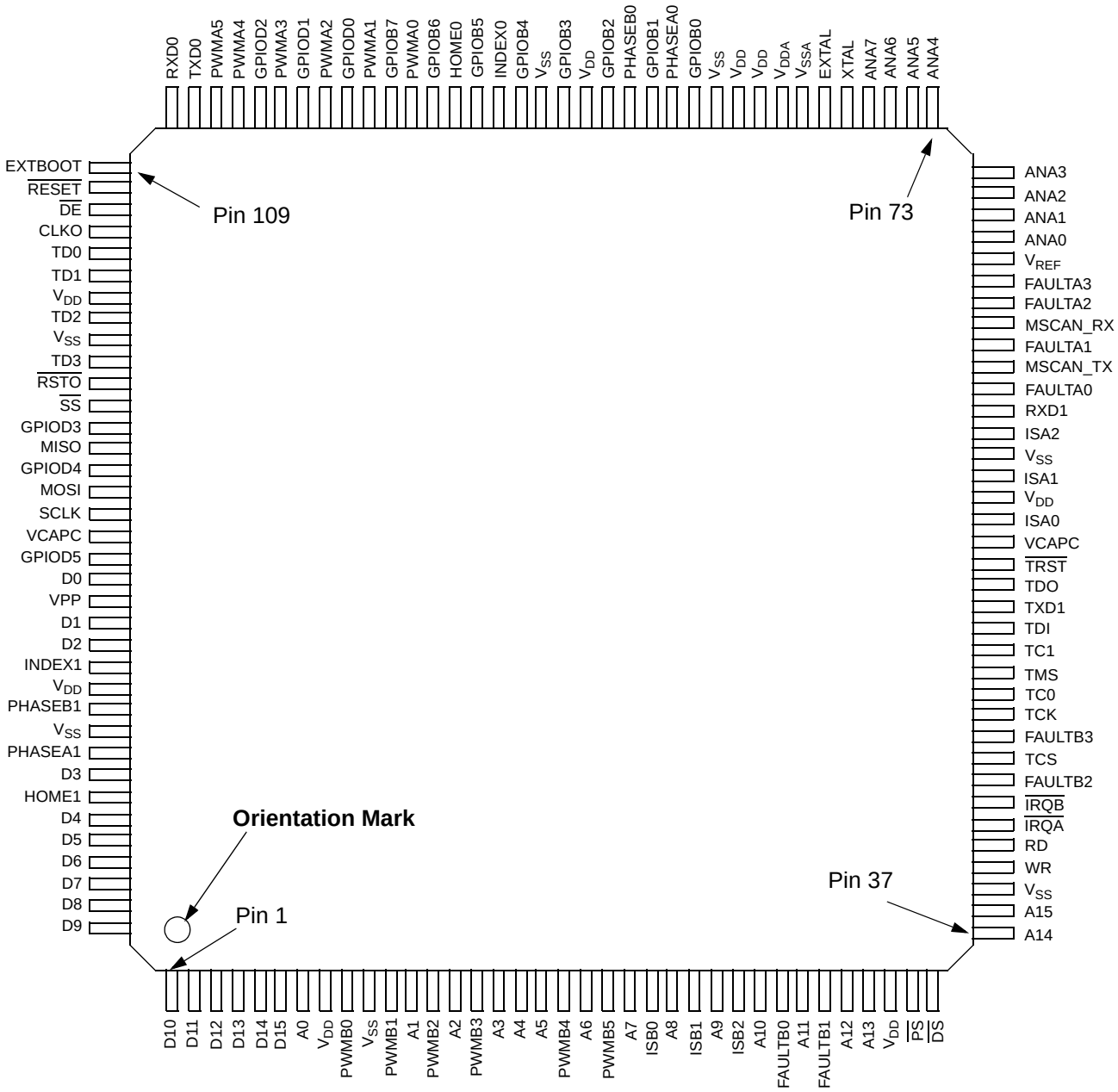
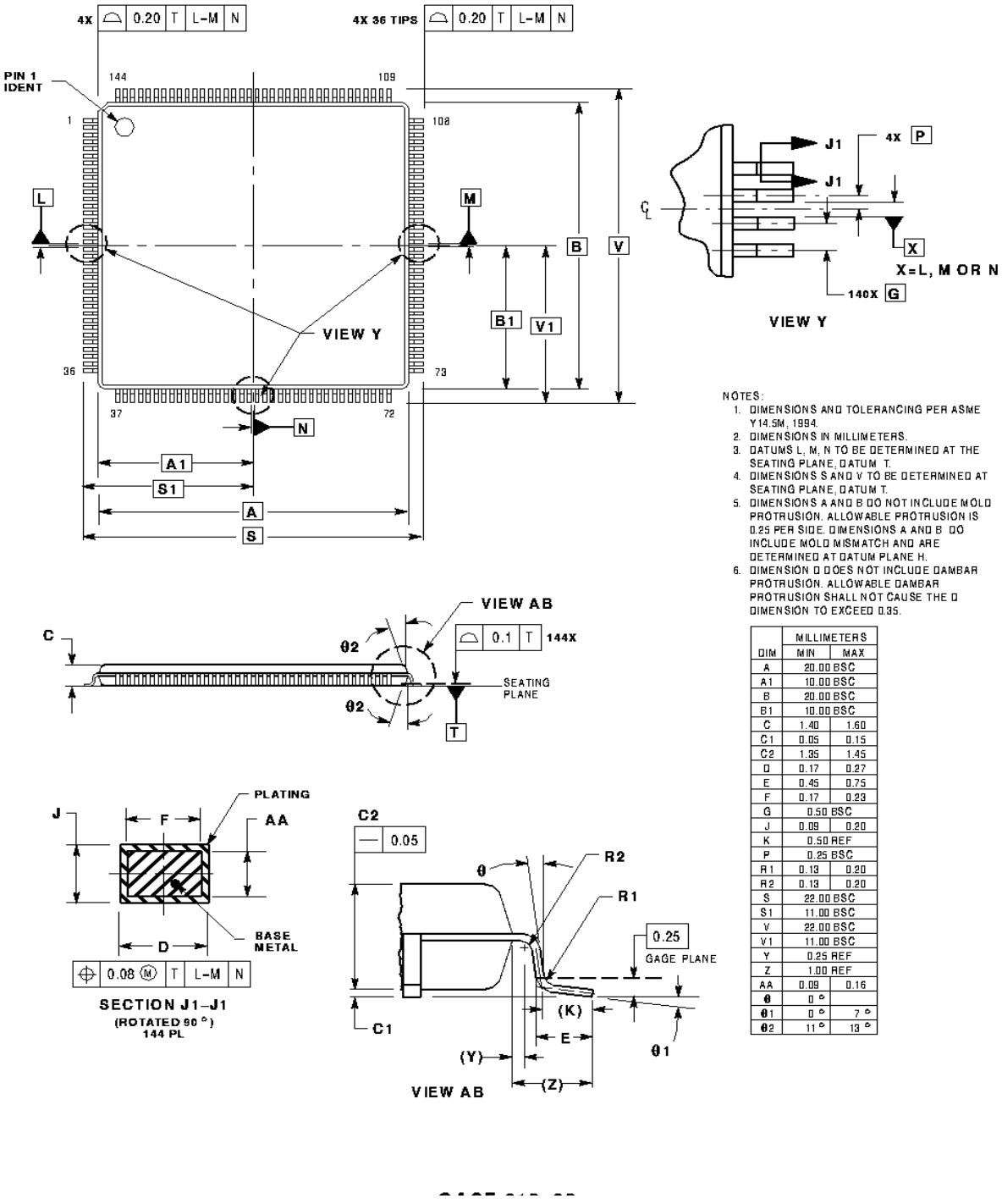


Figure 4-1 Top View, 56F805 144-pin LQFP Package

Table 4-1 56F805 Pin Identification by Pin Number

Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name	Pin No.	Signal Name
1	D10	37	A14	73	ANA4	109	EXTBOOT
2	D11	38	A15	74	ANA5	110	$\overline{\text{RESET}}$
3	D12	39	V_{SS}	75	ANA6	111	$\overline{\text{DE}}$
4	D13	40	WR	76	ANA7	112	CLKO
5	D14	41	RD	77	XTAL	113	TD0
6	D15	42	$\overline{\text{IRQA}}$	78	EXTAL	114	TD1
7	A0	43	$\overline{\text{IRQB}}$	79	V_{SSA}	115	V_{DD}
8	V_{DD}	44	FAULTB2	80	V_{DDA}	116	TD2
9	PWMB0	45	TCS	81	V_{DD}	117	V_{SS}
10	V_{SS}	46	FAULTB3	82	V_{DD}	118	TD3
11	PWMB1	47	TCK	83	V_{SS}	119	$\overline{\text{RSTO}}$
12	A1	48	TC0	84	GPIOB0	120	$\overline{\text{SS}}$
13	PWMB2	49	TMS	85	PHASEA0	121	GPIOD3
14	A2	50	TC1	86	GPIOB1	122	MISO
15	PWMB3	51	TDI	87	PHASEB0	123	GPIOD4
16	A3	52	TXD1	88	GPIOB2	124	MOSI
17	A4	53	TDO	89	V_{DD}	125	SCLK
18	A5	54	$\overline{\text{TRST}}$	90	GPIOB3	126	VCAPC
19	PWMB4	55	VCAPC	91	V_{SS}	127	GPIOD5
20	A6	56	ISA0	92	GPIOB4	128	D0
21	PWMB5	57	V_{DD}	93	INDEX0	129	VPP
22	A7	58	ISA1	94	GPIOB5	130	D1
23	ISB0	59	V_{SS}	95	HOME0	131	D2
24	A8	60	ISA2	96	GPIOB6	132	INDEX1
25	ISB1	61	RXD1	97	PWMA0	133	V_{DD}
26	A9	62	FAULTA0	98	GPIOB7	134	PHASEB1
27	ISB2	63	MSCAN_TX	99	PWMA1	135	V_{SS}
28	A10	64	FAULTA1	100	GPIOD0	136	PHASEA1
29	FAULTB0	65	MSCAN_RX	101	PWMA2	137	D3
30	A11	66	FAULTA2	102	GPIOD1	138	HOME1



DIM	MILLIMETERS MIN	MAX
A	20.00 BSC	
A1	10.00 BSC	
B	20.00 BSC	
B1	10.00 BSC	
C	1.40	1.60
C1	0.05	0.15
C2	1.35	1.45
D	0.17	0.27
E	0.45	0.75
F	0.17	0.23
G	0.50 BSC	
J	0.09	0.20
K	0.50 REF	
P	0.25 BSC	
R1	0.13	0.20
R2	0.13	0.20
S	22.00 BSC	
S1	11.00 BSC	
V	22.00 BSC	
V1	11.00 BSC	
Y	0.25 REF	
Z	1.00 REF	
AA	0.09	0.16
θ	0°	
θ1	0°	7°
θ2	11°	13°

Figure 4-2 144-pin LQFP Mechanical Information

Please see **www.freescale.com** for the most current case outline.