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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

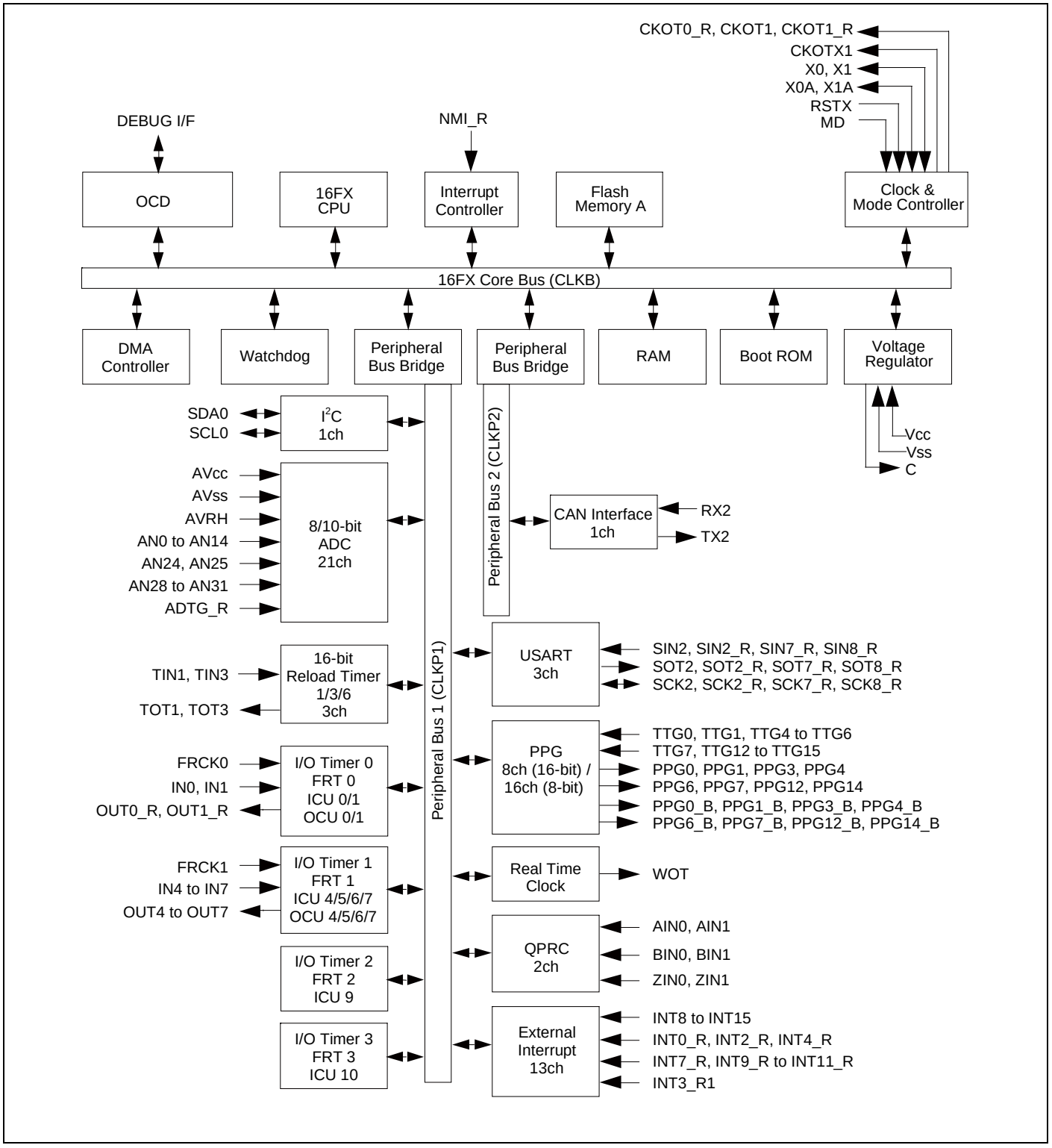
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f622abpmc-gse1

- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
- Source Clock Timers

  Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with Free-running Timer occurs
  - A pair of compare registers can be used to generate an output signal
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as 2 × 8-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
- Quadrature Position/Revolution Counter (QPRC)
  - Up/down count mode, Phase difference count mode, Count mode with direction
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers with interrupt
  - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, can not be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I^2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor
- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase or write

2. Block Diagram



4. Pin Description

Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
FRCKn	Free-Running Timer	Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
INTn_R1	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SCLn	I^2C	I^2C interface n clock I/O input/output pin
SDAn	I^2C	I^2C interface n serial data I/O input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin

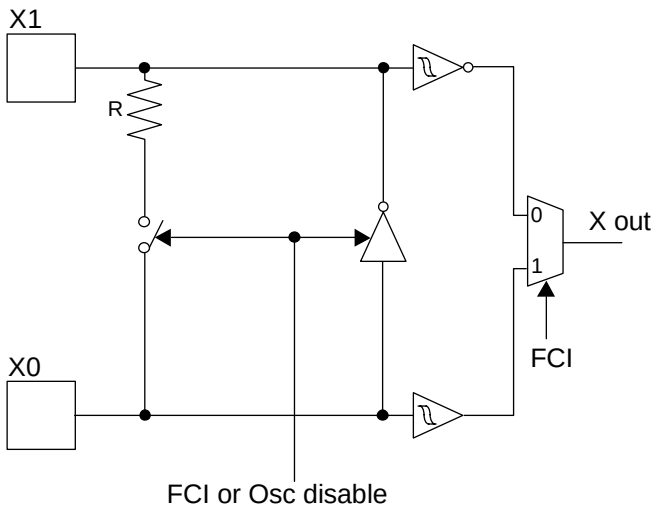
5. Pin Circuit Type

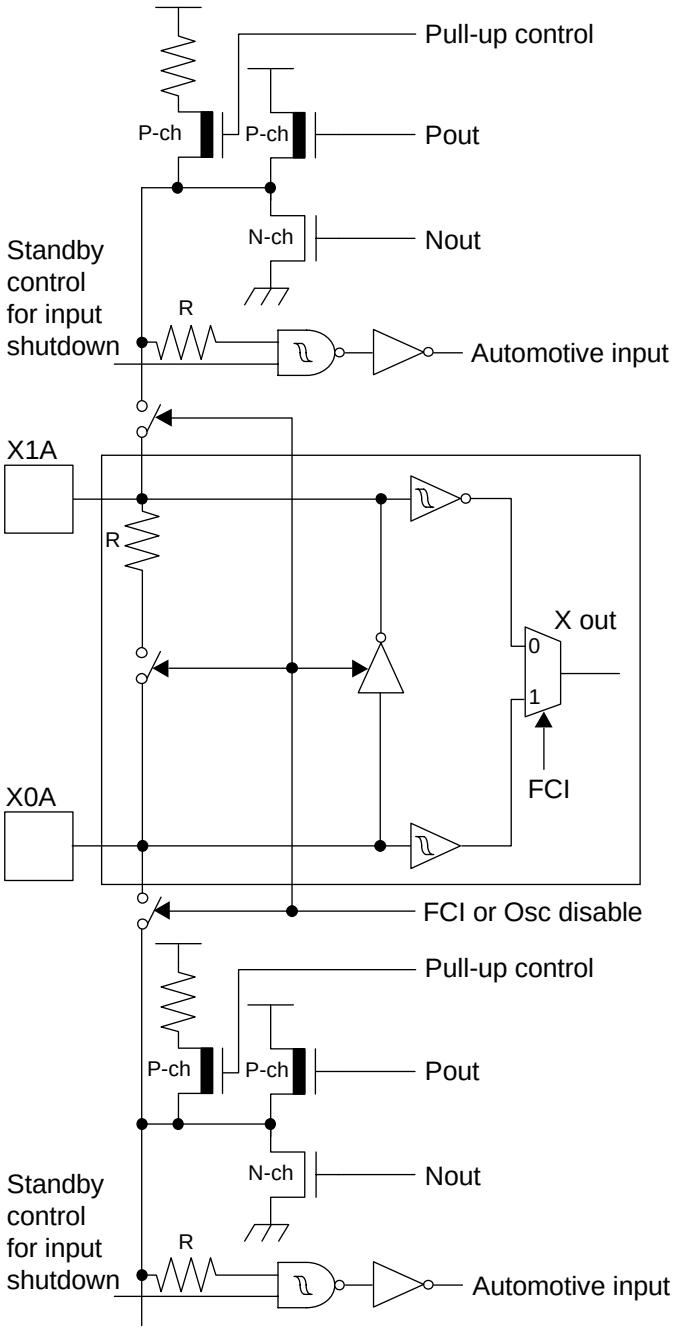
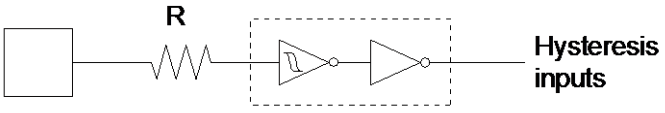
Pin no.	I/O circuit type*	Pin name
1	Supply	AVss
2	G	AVRH
3	K	P06_2 / AN2
4	K	P06_3 / AN3 / PPG3
5	K	P06_4 / AN4 / PPG4
6	K	P06_5 / AN5
7	K	P06_6 / AN6 / PPG6
8	K	P06_7 / AN7 / PPG7
9	I	P05_0 / AN8 / SIN2 / INT3_R1
10	K	P05_1 / AN9 / SOT2
11	I	P05_2 / AN10 / SCK2
12	K	P05_3 / AN11 / TIN3 / WOT
13	K	P05_4 / AN12 / TOT3 / INT2_R
14	K	P05_5 / AN13 / INT0_R / NMI_R
15	K	P05_6 / AN14 / INT4_R
16	H	P04_2 / IN6 / INT9_R / TTG6 / TTG14
17	H	P04_3 / IN7 / TTG7 / TTG15
18	Supply	Vss
19	B	P04_0 / X0A
20	B	P04_1 / X1A
21	C	MD
22	H	P17_0
23	O	DEBUG I/F
24	M	P00_0 / INT8 / SCK7_R / PPG0_B
25	H	P00_1 / INT9 / SOT7_R / PPG1_B
26	M	P00_2 / INT10 / SIN7_R
27	M	P00_3 / INT11 / SCK8_R / PPG3_B
28	H	P00_4 / INT12 / SOT8_R / PPG12_B
29	M	P00_5 / INT13 / SIN8_R / PPG14_B
30	H	P00_6 / INT14
31	H	P00_7 / INT15
32	H	P01_0 / TIN1 / CKOT1 / OUT0_R

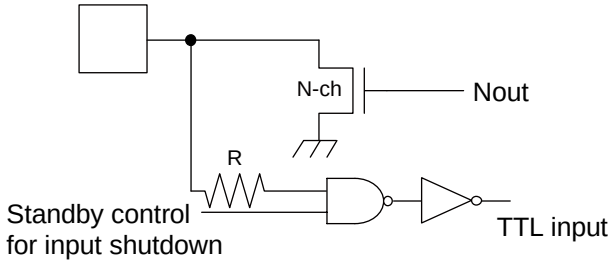
Pin no.	I/O circuit type*	Pin name
33	N	P04_5 / SCL0
34	O	DEBUG I/F
35	H	P17_0
36	C	MD
37	A	X0
38	A	X1
39	Supply	Vss
40	B	P04_0 / X0A
41	B	P04_1 / X1A
42	C	RSTX
43	J	P11_7 / SEG3 / IN0_R
44	J	P11_0 / COM0
45	J	P11_1 / COM1 / PPG0_R
46	J	P11_2 / COM2 / PPG1_R
47	J	P11_3 / COM3 / PPG2_R
48	J	P12_0 / SEG4 / IN1_R
49	J	P12_1 / SEG5 / TIN1_R / PPG0_B
50	J	P12_2 / SEG6 / TOT1_R / PPG1_B
51	J	P12_4 / SEG8
52	J	P12_5 / SEG9 / TIN2_R / PPG2_B
53	J	P12_6 / SEG10 / TOT2_R / PPG3_B
54	J	P12_7 / SEG11 / INT1_R
55	J	P01_1 / SEG21 / CKOT1
56	J	P01_3 / SEG23
57	L	P03_0 / SEG36 / V0
58	L	P03_1 / SEG37 / V1
59	L	P03_2 / SEG38 / V2
60	L	P03_3 / SEG39 / V3
61	M	P03_4 / RX0 / INT4
62	H	P03_5 / TX0
63	H	P03_6 / INT0 / NMI
64	Supply	Vcc

*: See “I/O Circuit Type” for details on the I/O circuit types.

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

Type	Circuit	Remarks
O		• Open-drain I/O • Output 25mA, Vcc = 2.7V • TTL input

■Precautions Related to Usage of Devices
Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

12.2 Precautions for Package Mounting
Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

■Lead Insertion Type
Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

■Surface Mount Type
Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

■Lead-Free Packaging
CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

■Storage of Semiconductor Devices
Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.
   When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

■Baking
Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{cc}/V^{ss})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{cc} pins and V_{ss} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC}, AVRH) exceed the digital power-supply voltage.

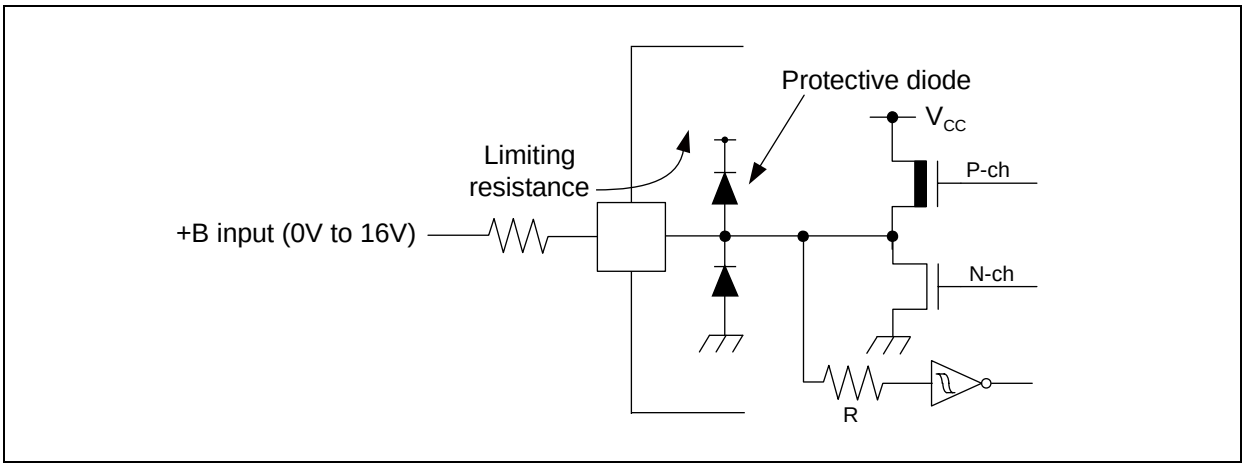
13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register PIER = 0).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than 2kΩ.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

- The DEBUG I/F pin has only a protective diode against V_{SS}. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Write/erase to a large sector in flash memory is warranted with TA ≤ + 105°C.

WARNING
Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.3 DC Characteristics

14.3.1 Current Rating

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Run modes[*1]	I_{CCPLL}	Vcc	PLL Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32MHz Flash 0 wait (CLKRC and CLKSC stopped)	-	25	-	mA	T_A = +25°C
				-	-	34	mA	T_A = +105°C
				-	-	35	mA	T_A = +125°C
	I_{CCMAIN}		Main Run mode with CLKS1/2 = CLKB = CLKP1/2 = 4MHz Flash 0 wait (CLKPLL, CLKSC and CLKRC stopped)	-	3.5	-	mA	T_A = +25°C
				-	-	7.5	mA	T_A = +105°C
				-	-	8.5	mA	T_A = +125°C
	I_{CCRCH}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	1.7	-	mA	T_A = +25°C
				-	-	5.5	mA	T_A = +105°C
				-	-	6.5	mA	T_A = +125°C
	I_{CCRCL}		RC Run mode with CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz Flash 0 wait (CLKMC, CLKPLL and CLKSC stopped)	-	0.15	-	mA	T_A = +25°C
				-	-	3.2	mA	T_A = +105°C
				-	-	4.2	mA	T_A = +125°C
	I_{CCSUB}		Sub Run mode with CLKS1/2 = CLKB = CLKP1/2 = 32kHz Flash 0 wait (CLKMC, CLKPLL and CLKRC stopped)	-	0.1	-	mA	T_A = +25°C
				-	-	3	mA	T_A = +105°C
				-	-	4	mA	T_A = +125°C

14.4.8 USART Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C, C_L=50pF)

Parameter	Symbol	Pin name	Conditions	4.5V ≤ V_{CC} < 5.5V		2.7V ≤ V_{CC} < 4.5V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1}$ – 20*	-	$N \times t_{CLKP1}$ – 30*	-	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		t_{CLKP1} + 45	-	t_{CLKP1} + 55	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1}$ + 45	-	$2t_{CLKP1}$ + 55	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2$ + 10	-	$t_{CLKP1}/2$ + 10	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		t_{CLKP1} + 10	-	t_{CLKP1} + 10	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:

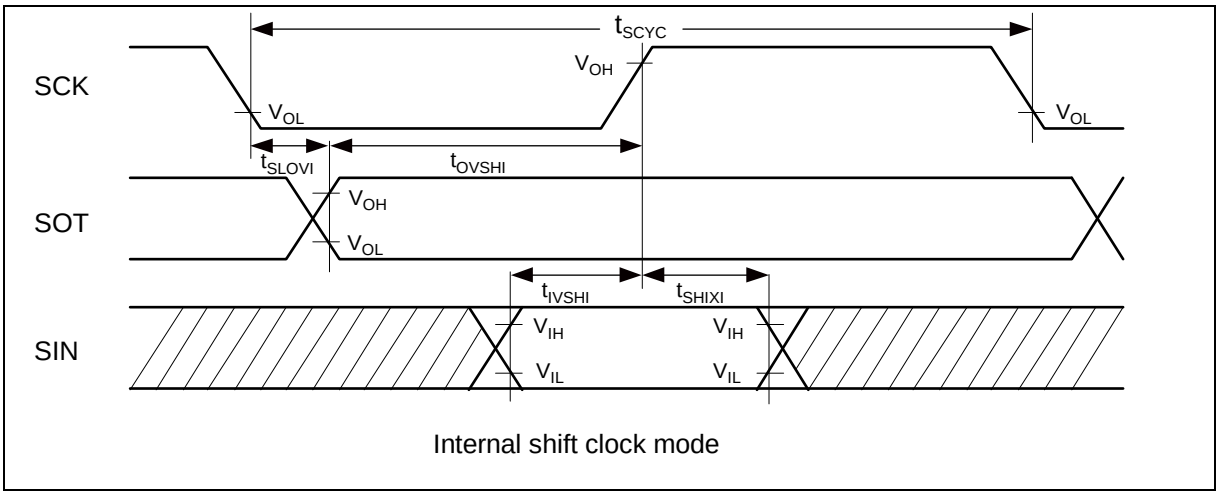
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in “MB96600 series HARDWARE MANUAL”.
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
  For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

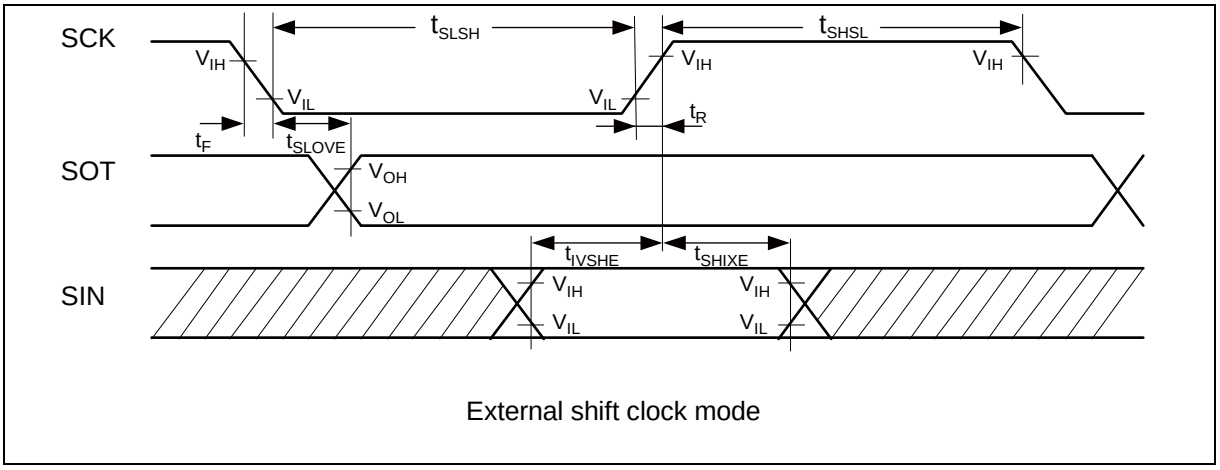
- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then N = k, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then N = k + 1, where k is an integer > 1

Examples:

t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4
…	…



Internal shift clock mode



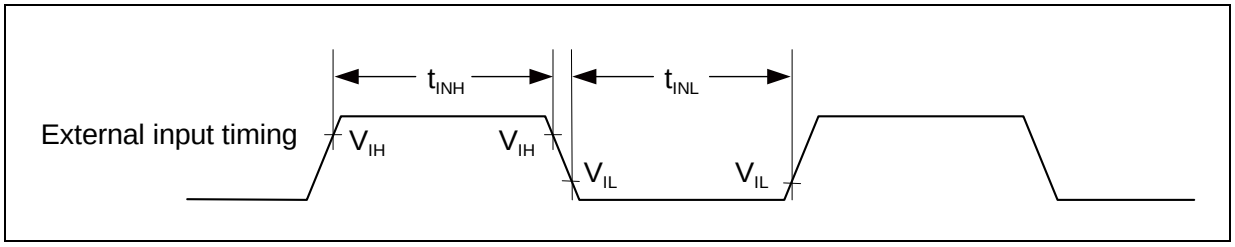
External shift clock mode

14.4.9 External Input Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

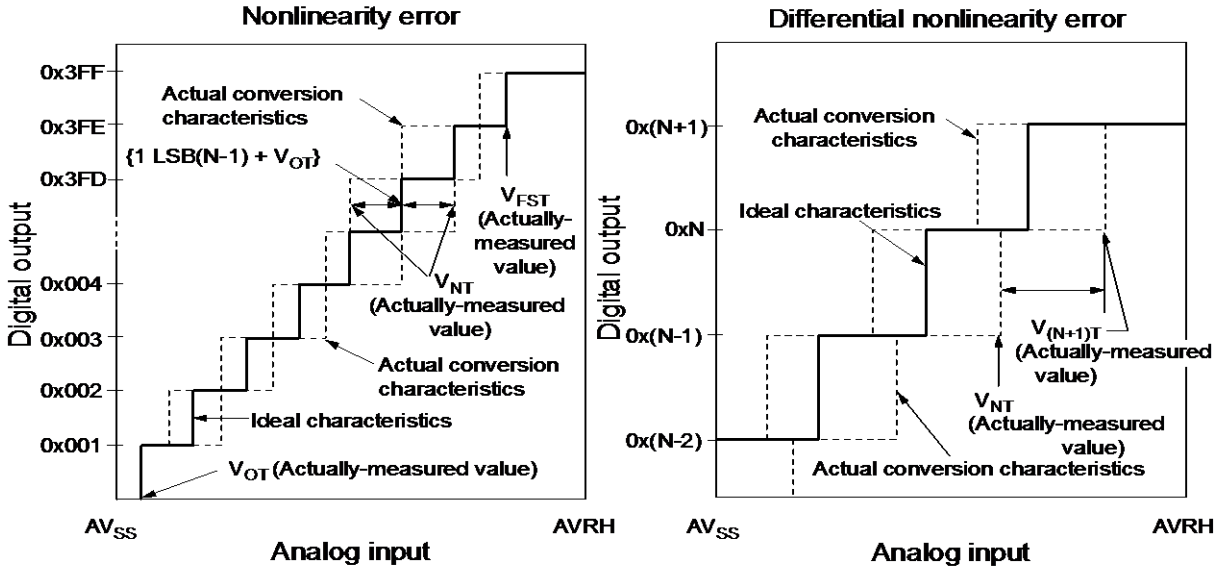
Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH}, t_{INL}	Pnn_m	$2t_{CLKP1}$ +200 (t_{CLKP1}= $1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG_R				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		FRCKn				Free-Running Timer input clock
		INn				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R, INTn_R1	200	-	ns	External Interrupt
		NMI_R				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.5.3 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage : Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.



$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.

14.6 Low Voltage Detection Function Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
Detected voltage[*1]	V_{DL0}	CILCR:LVL = 0000_B	2.70	2.90	3.10	V
	V_{DL1}	CILCR:LVL = 0001_B	2.79	3.00	3.21	V
	V_{DL2}	CILCR:LVL = 0010_B	2.98	3.20	3.42	V
	V_{DL3}	CILCR:LVL = 0011_B	3.26	3.50	3.74	V
	V_{DL4}	CILCR:LVL = 0100_B	3.45	3.70	3.95	V
	V_{DL5}	CILCR:LVL = 0111_B	3.73	4.00	4.27	V
	V_{DL6}	CILCR:LVL = 1001_B	3.91	4.20	4.49	V
Power supply voltage change rate[*2]	dV/dt	-	- 0.004	-	+ 0.004	V/µs
Hysteresis width	V_{HYS}	CILCR:LVHYS=0	-	-	50	mV
		CILCR:LVHYS=1	80	100	120	mV
Stabilization time	$T_{LVDSTAB}$	-	-	-	75	µs
Detection delay time	t_d	-	-	-	30	µs

[*1]: If the power supply voltage fluctuates within the time less than the detection delay time (t_d), there is a possibility that the low voltage detection will occur or stop after the power supply voltage passes the detection range.

[*2]: In order to perform the low voltage detection at the detection voltage (V_{DLX}), be sure to suppress fluctuation of the power supply voltage within the limits of the change ration of power supply voltage.

14.7 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	T_A ≤ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	T_A ≤ + 105°C	-	25	400	µs	Not including system-level overhead time.
	Small Sector	-	-	25	400	µs	
Chip erase time		T_A ≤ + 105°C	-	5.11	25.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 [*2]
10,000	10 [*2]
100,000	5 [*2]

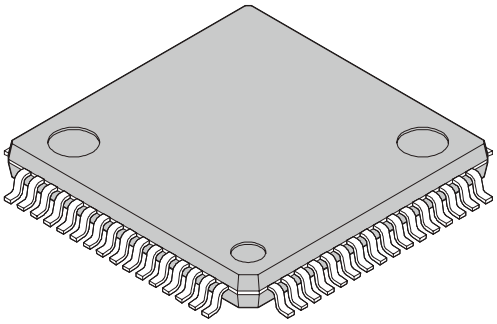
[*1]: See "Low Voltage Detection Function Characteristics".

[*2]: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

■Used setting

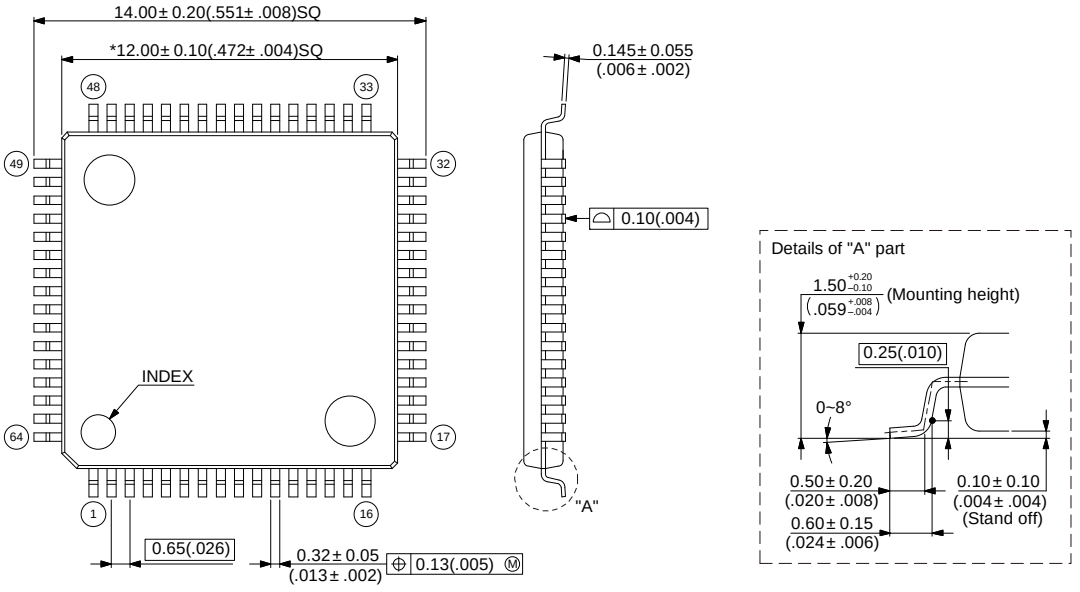
Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode

17. Package Dimension

64-pin plastic LQFP		
	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
(FPT-64P-M23)	Code (Reference)	P-LQFP64-12 × 12-0.65

64-pin plastic LQFP
(FPT-64P-M23)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values