Infineon Technologies - MB96F622RBPMC1-GSE1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f622rbpmc1-gse1

- A/D converter
  - SAR-type
  - 8/10-bit resolution
  - Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
  - Range Comparator Function
- Source Clock Timers

  Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)
- Hardware Watchdog Timer
  - Hardware watchdog timer is active after reset
  - Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval
- Reload Timers
  - 16-bit wide
  - Prescaler with $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$ of peripheral clock frequency
  - Event count function
- Free-Running Timers
  - Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
  - Prescaler with 1, $1/2^1$, $1/2^2$, $1/2^3$, $1/2^4$, $1/2^5$, $1/2^6$, $1/2^7$, $1/2^8$ of peripheral clock frequency
- Input Capture Units
  - 16-bit wide
  - Signals an interrupt upon external event
  - Rising edge, Falling edge or Both (rising & falling) edges sensitive
- Output Compare Units
  - 16-bit wide
  - Signals an interrupt when a match with Free-running Timer occurs
  - A pair of compare registers can be used to generate an output signal
- Programmable Pulse Generator
  - 16-bit down counter, cycle and duty setting registers
  - Can be used as 2 × 8-bit PPG
  - Interrupt at trigger, counter borrow and/or duty match
  - PWM operation and one-shot operation
  - Internal prescaler allows 1, 1/4, 1/16, 1/64 of peripheral clock as counter clock or of selected Reload timer underflow as clock input
  - Can be triggered by software or reload timer
  - Can trigger ADC conversion
  - Timing point capture
- Quadrature Position/Revolution Counter (QPRC)
  - Up/down count mode, Phase difference count mode, Count mode with direction
  - 16-bit position counter
  - 16-bit revolution counter
  - Two 16-bit compare registers with interrupt
  - Detection edge of the three external event input pins AIN, BIN and ZIN is configurable
- Real Time Clock
  - Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
  - Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
  - Read/write accessible second/minute/hour registers
  - Can signal interrupts every half second/second/minute/hour/day
  - Internal clock divider and prescaler provide exact 1s clock
- External Interrupts
  - Edge or Level sensitive
  - Interrupt mask bit per channel
  - Each available CAN channel RX has an external interrupt for wake-up
  - Selected USART channels SIN have an external interrupt for wake-up
- Non Maskable Interrupt
  - Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
  - Once enabled, can not be disabled other than by reset
  - High or Low level sensitive
  - Pin shared with external interrupt 0
- I/O Ports
  - Most of the external pins can be used as general purpose I/O
  - All push-pull outputs (except when used as I^2C SDA/SCL line)
  - Bit-wise programmable as input/output or peripheral signal
  - Bit-wise programmable input enable
  - One input level per GPIO-pin (either Automotive or CMOS hysteresis)
  - Bit-wise programmable pull-up resistor
- Built-in On Chip Debugger (OCD)
  - One-wire debug tool interface
  - Break function:
    - Hardware break: 6 points (shared with code event)
    - Software break: 4096 points
  - Event function
    - Code event: 6 points (shared with hardware break)
    - Data event: 6 points
    - Event sequencer: 2 levels + reset
  - Execution time measurement function
  - Trace function: 42 branches
  - Security function
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erase or write

1. Product Lineup

Features			MB96620	Remark
Product Type			Flash Memory Product	
Subclock			Subclock can be set by software	
Dual Operation Flash Memory		RAM	-	
32.5KB + 32KB		4KB	MB96F622R, MB96F622A	Product Options R: MCU with CAN A: MCU without CAN
64.5KB + 32KB		10KB	MB96F623R, MB96F623A	
128.5KB + 32KB		10KB	MB96F625R, MB96F625A	
Package			LQFP-64 FPT-64P-M23/M24	
DMA			2ch	
USART			3ch	LIN-USART 2/7/8
	with automatic LIN-Header transmission/reception		Yes (only 1ch)	LIN-USART 2
	with 16 byte RX- and TX-FIFO		No	
I^2C			1ch	I^2C 0
8/10-bit A/D Converter			21ch	AN 0 to 14/24/25/28 to 31
	with Data Buffer		No	
	with Range Comparator		Yes	
	with Scan Disable		No	
	with ADC Pulse Detection		No	
16-bit Reload Timer (RLT)			3ch	RLT 1/3/6
16-bit Free-Running Timer (FRT)			4ch	FRT 0 to 3 FRT 2/3 does not have external clock input pin
16-bit Input Capture Unit (ICU)			8ch (2 channels for LIN-USART)	ICU 0/1/4 to 7/9/10 (ICU 9/10 for LIN-USART)
16-bit Output Compare Unit (OCU)			6ch	OCU 0/1/4 to 7
8/16-bit Programmable Pulse Generator (PPG)			8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
	with Timing point capture		Yes	
	with Start delay		No	
	with Ramp		No	
Quadrature Position/Revolution Counter (QPRC)			2ch	QPRC 0/1
CAN Interface			1ch	CAN 2 32 Message Buffers
External Interrupts (INT)			13ch	INT 0/2/3/4/7 to 15
Non-Maskable Interrupt (NMI)			1ch	
Real Time Clock (RTC)			1ch	
I/O Ports			50 (Dual clock mode) 52 (Single clock mode)	
Clock Calibration Unit (CAL)			1ch	
Clock Output Function			2ch	
Low Voltage Detection Function			Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer			Yes	
On-chip RC-oscillator			Yes	
On-chip Debugger			Yes	

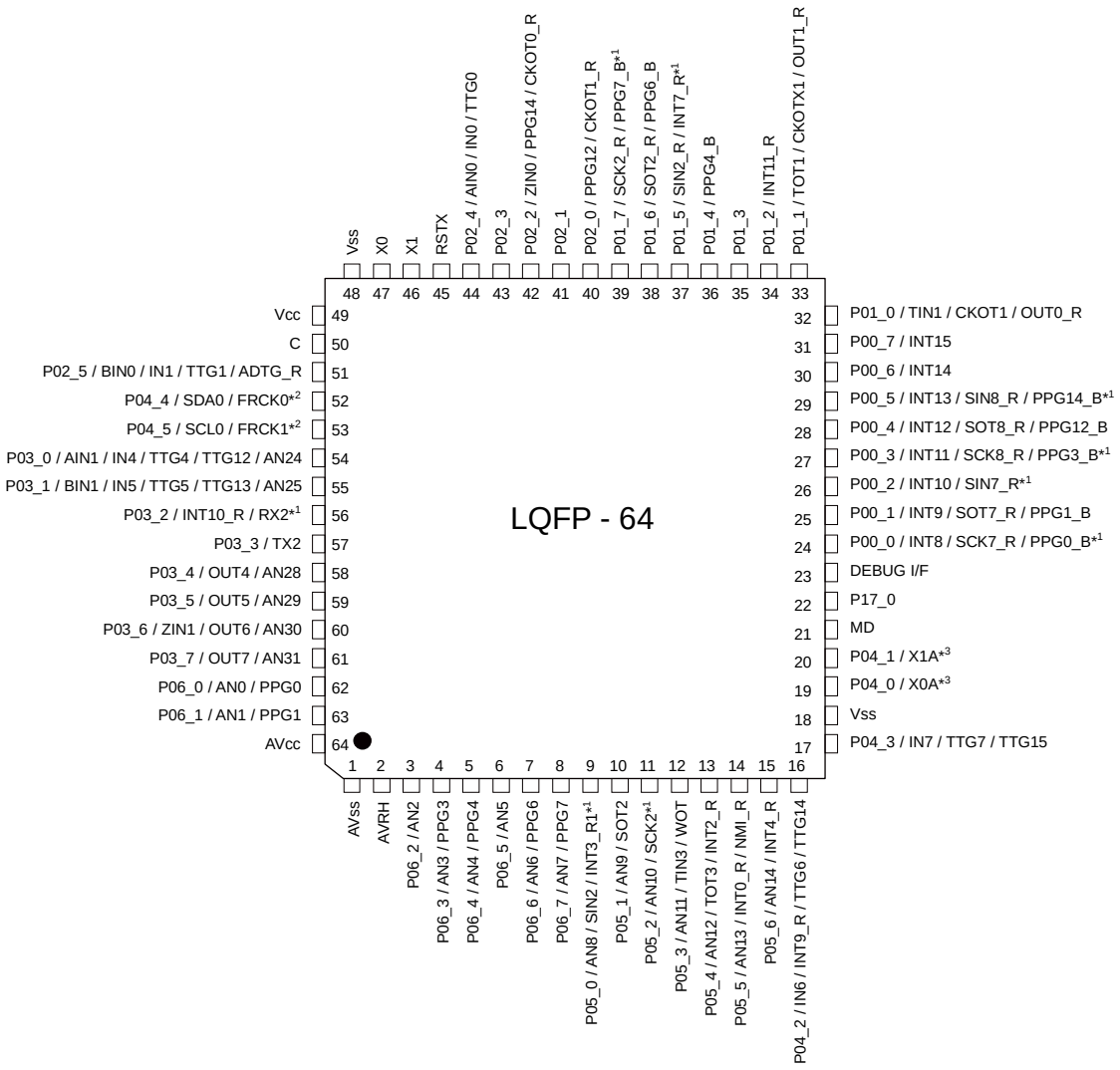
Note:

All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.

It is necessary to use the port relocate function of the general I/O port according to your function use.

3. Pin Assignment

(Top view)



(FPT-64P-M23/M24)

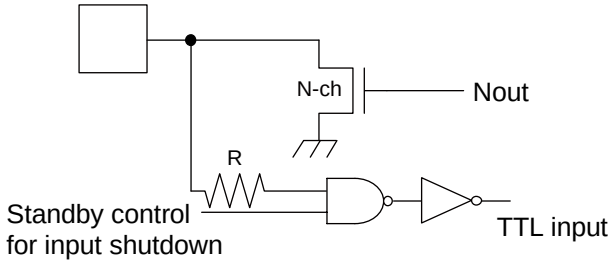
*1: CMOS input level only

*2: CMOS input level only for I^2C

*3: Please set ROM Configuration Block (RCB) to use the subclock.

Other than those above, general-purpose pins have only Automotive input level.

Pin name	Feature	Description
WOT	RTC	Real Time clock output pin
X0	Clock	Oscillator input pin
X0A	Clock	Subclock Oscillator input pin
X1	Clock	Oscillator output pin
X1A	Clock	Subclock Oscillator output pin
ZINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin

Type	Circuit	Remarks
O		• Open-drain I/O • Output 25mA, Vcc = 2.7V • TTL input

8. RAMSTART Addresses

Devices	Bank 0 RAM size	RAMSTART0
MB96F622	4KB	$00:7200_H$
MB96F623 MB96F625	10KB	$00:5A00_H$

9. User ROM Memory Map For Flash Devices

CPU mode address	Flash memory mode address	MB96F622 Flash size 32.5KB + 32KB	MB96F623 Flash size 64.5KB + 32KB	MB96F625 Flash size 128.5KB + 32KB	
$FF:FFFF_H$ $FF:8000_H$	$3F:FFFF_H$ $3F:8000_H$	SA39 - 32KB	SA39 - 64KB	SA39 - 64KB	Bank A of Flash A
$FF:7FFF_H$ $FF:0000_H$	$3F:7FFF_H$ $3F:0000_H$	Reserved			
$FE:FFFF_H$ $FE:0000_H$	$3E:FFFF_H$ $3E:0000_H$		Reserved	SA38 - 64KB	
$FD:FFFF_H$ $DF:A000_H$				Reserved	
$DF:9FFF_H$ $DF:8000_H$	$1F:9FFF_H$ $1F:8000_H$	SA4 - 8KB	SA4 - 8KB	SA4 - 8KB	Bank B of Flash A
$DF:7FFF_H$ $DF:6000_H$	$1F:7FFF_H$ $1F:6000_H$	SA3 - 8KB	SA3 - 8KB	SA3 - 8KB	
$DF:5FFF_H$ $DF:4000_H$	$1F:5FFF_H$ $1F:4000_H$	SA2 - 8KB	SA2 - 8KB	SA2 - 8KB	
$DF:3FFF_H$ $DF:2000_H$	$1F:3FFF_H$ $1F:2000_H$	SA1 - 8KB	SA1 - 8KB	SA1 - 8KB	
$DF:1FFF_H$ $DF:0000_H$	$1F:1FFF_H$ $1F:0000_H$	SAS - 512B*	SAS - 512B*	SAS - 512B*	Bank A of Flash A
$DE:FFFF_H$ $DE:0000_H$		Reserved	Reserved	Reserved	

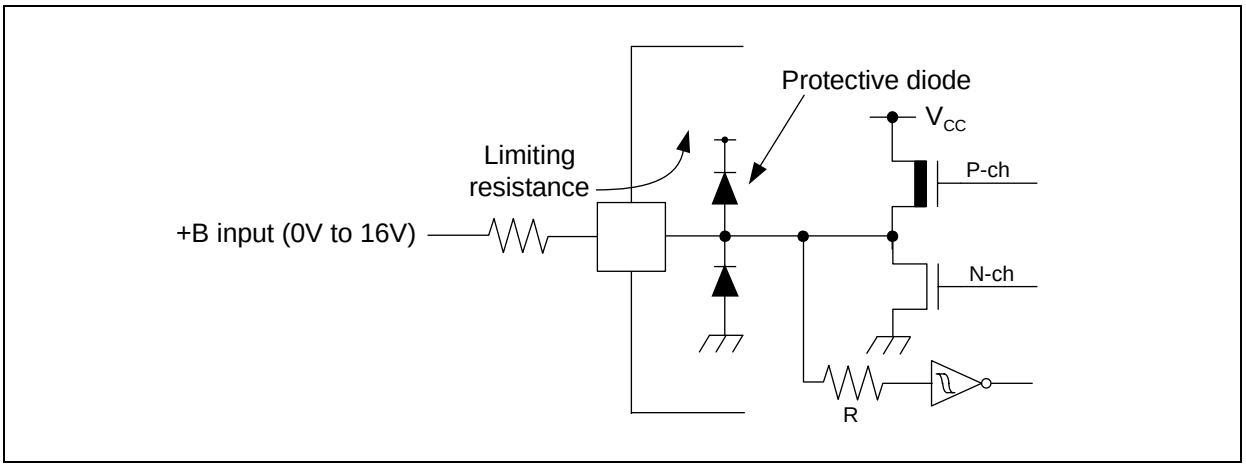
*: Physical address area of SAS-512B is from $DF:0000_H$ to $DF:01FF_H$.
Others (from $DF:0200_H$ to $DF:1FFF_H$) is mirror area of SAS-512B.
Sector SAS contains the ROM configuration block RCBA at CPU address $DF:0000_H$ -$DF:01FF_H$.
SAS can not be used for E^2PROM emulation.

11. Interrupt Vector Table

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
0	$3FC_H$	CALLV0	No	-	CALLV instruction
1	$3F8_H$	CALLV1	No	-	CALLV instruction
2	$3F4_H$	CALLV2	No	-	CALLV instruction
3	$3F0_H$	CALLV3	No	-	CALLV instruction
4	$3EC_H$	CALLV4	No	-	CALLV instruction
5	$3E8_H$	CALLV5	No	-	CALLV instruction
6	$3E4_H$	CALLV6	No	-	CALLV instruction
7	$3E0_H$	CALLV7	No	-	CALLV instruction
8	$3DC_H$	RESET	No	-	Reset vector
9	$3D8_H$	INT9	No	-	INT9 instruction
10	$3D4_H$	EXCEPTION	No	-	Undefined instruction execution
11	$3D0_H$	NMI	No	-	Non-Maskable Interrupt
12	$3CC_H$	DLY	No	12	Delayed Interrupt
13	$3C8_H$	RC_TIMER	No	13	RC Clock Timer
14	$3C4_H$	MC_TIMER	No	14	Main Clock Timer
15	$3C0_H$	SC_TIMER	No	15	Sub Clock Timer
16	$3BC_H$	LVDI	No	16	Low Voltage Detector
17	$3B8_H$	EXTINT0	Yes	17	External Interrupt 0
18	$3B4_H$	-	-	18	Reserved
19	$3B0_H$	EXTINT2	Yes	19	External Interrupt 2
20	$3AC_H$	EXTINT3	Yes	20	External Interrupt 3
21	$3A8_H$	EXTINT4	Yes	21	External Interrupt 4
22	$3A4_H$	-	-	22	Reserved
23	$3A0_H$	-	-	23	Reserved
24	$39C_H$	EXTINT7	Yes	24	External Interrupt 7
25	398_H	EXTINT8	Yes	25	External Interrupt 8
26	394_H	EXTINT9	Yes	26	External Interrupt 9
27	390_H	EXTINT10	Yes	27	External Interrupt 10
28	$38C_H$	EXTINT11	Yes	28	External Interrupt 11
29	388_H	EXTINT12	Yes	29	External Interrupt 12
30	384_H	EXTINT13	Yes	30	External Interrupt 13
31	380_H	EXTINT14	Yes	31	External Interrupt 14
32	$37C_H$	EXTINT15	Yes	32	External Interrupt 15
33	378_H	-	-	33	Reserved
34	374_H	-	-	34	Reserved
35	370_H	CAN2	No	35	CAN Controller 2
36	$36C_H$	-	-	36	Reserved
37	368_H	-	-	37	Reserved
38	364_H	PPG0	Yes	38	Programmable Pulse Generator 0
39	360_H	PPG1	Yes	39	Programmable Pulse Generator 1

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
81	$2B8_H$	OCU4	Yes	81	Output Compare Unit 4
82	$2B4_H$	OCU5	Yes	82	Output Compare Unit 5
83	$2B0_H$	OCU6	Yes	83	Output Compare Unit 6
84	$2AC_H$	OCU7	Yes	84	Output Compare Unit 7
85	$2A8_H$	-	-	85	Reserved
86	$2A4_H$	-	-	86	Reserved
87	$2A0_H$	-	-	87	Reserved
88	$29C_H$	-	-	88	Reserved
89	298_H	FRT0	Yes	89	Free-Running Timer 0
90	294_H	FRT1	Yes	90	Free-Running Timer 1
91	290_H	FRT2	Yes	91	Free-Running Timer 2
92	$28C_H$	FRT3	Yes	92	Free-Running Timer 3
93	288_H	RTC0	No	93	Real Time Clock
94	284_H	CAL0	No	94	Clock Calibration Unit
95	280_H	-	-	95	Reserved
96	$27C_H$	IIC0	Yes	96	I^2C interface 0
97	278_H	-	-	97	Reserved
98	274_H	ADC0	Yes	98	A/D Converter 0
99	270_H	-	-	99	Reserved
100	$26C_H$	-	-	100	Reserved
101	268_H	-	-	101	Reserved
102	264_H	-	-	102	Reserved
103	260_H	-	-	103	Reserved
104	$25C_H$	-	-	104	Reserved
105	258_H	LINR2	Yes	105	LIN USART 2 RX
106	254_H	LINT2	Yes	106	LIN USART 2 TX
107	250_H	-	-	107	Reserved
108	$24C_H$	-	-	108	Reserved
109	248_H	-	-	109	Reserved
110	244_H	-	-	110	Reserved
111	240_H	-	-	111	Reserved
112	$23C_H$	-	-	112	Reserved
113	238_H	-	-	113	Reserved
114	234_H	-	-	114	Reserved
115	230_H	LINR7	Yes	115	LIN USART 7 RX
116	$22C_H$	LINT7	Yes	116	LIN USART 7 TX
117	228_H	LINR8	Yes	117	LIN USART 8 RX
118	224_H	LINT8	Yes	118	LIN USART 8 TX
119	220_H	-	-	119	Reserved
120	$21C_H$	-	-	120	Reserved
121	218_H	-	-	121	Reserved
122	214_H	-	-	122	Reserved

- The DEBUG I/F pin has only a protective diode against V_{SS}. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.
- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Write/erase to a large sector in flash memory is warranted with TA ≤ + 105°C.

WARNING
Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

14.2 Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	V_{CC}, AV_{CC}	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	C_S	0.5	1.0 to 3.9	4.7	µF	1.0µF (Allowance within ± 50%) 3.9µF (Allowance within ± 20%) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at V_{CC} must use the one of a capacity value that is larger than C_S.

WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes[*2]	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2245	µA	T_A = +25°C
				-	-	3165	µA	T_A = +105°C
				-	-	3975	µA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	µA	T_A = +25°C
				-	-	1085	µA	T_A = +105°C
				-	-	1930	µA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	µA	T_A = +25°C
				-	-	1025	µA	T_A = +105°C
				-	-	1840	µA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	µA	T_A = +25°C
				-	-	855	µA	T_A = +105°C
				-	-	1640	µA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	µA	T_A = +25°C
				-	-	830	µA	T_A = +105°C
				-	-	1620	µA	T_A = +125°C

14.3.2 Pin Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level input voltage	V_{IH}	Port inputs Pnn_m	-	V_{CC} × 0.7	-	V_{CC} + 0.3	V	CMOS Hysteresis input
			-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	AUTOMOTIVE Hysteresis input
	V_{IHX0S}	X0	External clock in "Fast Clock Input mode"	VD × 0.8	-	VD	V	VD=1.8V±0.15V
	V_{IHX0AS}	X0A	External clock in "Oscillation mode"	V_{CC} × 0.8	-	V_{CC} + 0.3	V	
	V_{IHR}	RSTX	-	V_{CC} × 0.8	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHM}	MD	-	V_{CC} - 0.3	-	V_{CC} + 0.3	V	CMOS Hysteresis input
	V_{IHD}	DEBUG I/F	-	2.0	-	V_{CC} + 0.3	V	TTL Input
"L" level input voltage	V_{IL}	Port inputs Pnn_m	-	V_{SS} - 0.3	-	V_{CC} × 0.3	V	CMOS Hysteresis input
			-	V_{SS} - 0.3	-	V_{CC} × 0.5	V	AUTOMOTIVE Hysteresis input
	V_{ILX0S}	X0	External clock in "Fast Clock Input mode"	V_{SS}	-	VD × 0.2	V	VD=1.8V±0.15V
	V_{ILX0AS}	X0A	External clock in "Oscillation mode"	V_{SS} - 0.3	-	V_{CC} × 0.2	V	
	V_{ILR}	RSTX	-	V_{SS} - 0.3	-	V_{CC} × 0.2	V	CMOS Hysteresis input
	V_{ILM}	MD	-	V_{SS} - 0.3	-	V_{SS} + 0.3	V	CMOS Hysteresis input
	V_{ILD}	DEBUG I/F	-	V_{SS} - 0.3	-	0.8	V	TTL Input

14.4.3 Built-in RC Oscillation Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	µs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	µs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing

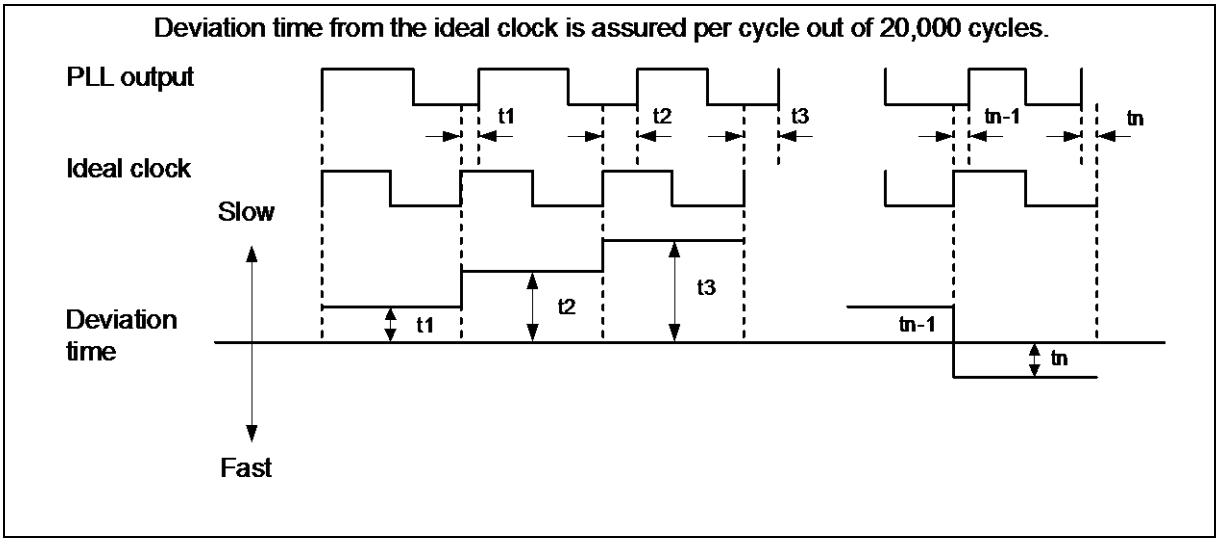
(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.5 Operating Conditions of PLL

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

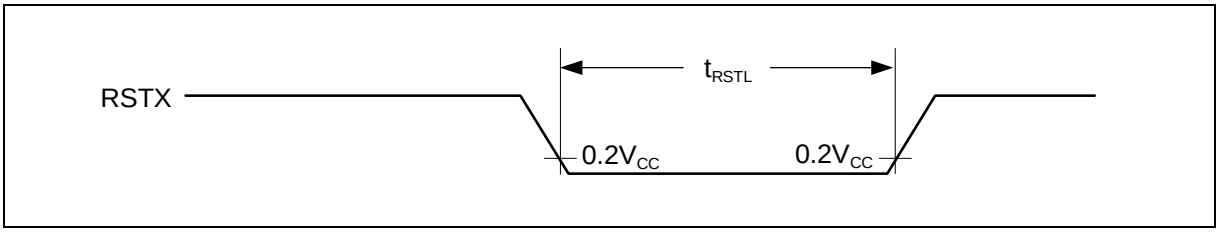
Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
PLL oscillation stabilization wait time	t_{LOCK}	1	-	4	ms	For CLKMC = 4MHz
PLL input clock frequency	f_{PLLI}	4	-	8	MHz	
PLL oscillation clock frequency	f_{CLKVCO}	56	-	108	MHz	Permitted VCO output frequency of PLL (CLKVCO)
PLL phase jitter	t_{PSKEW}	-5	-	+5	ns	For CLKMC (PLL input clock) ≥ 4MHz



14.4.6 Reset Input

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

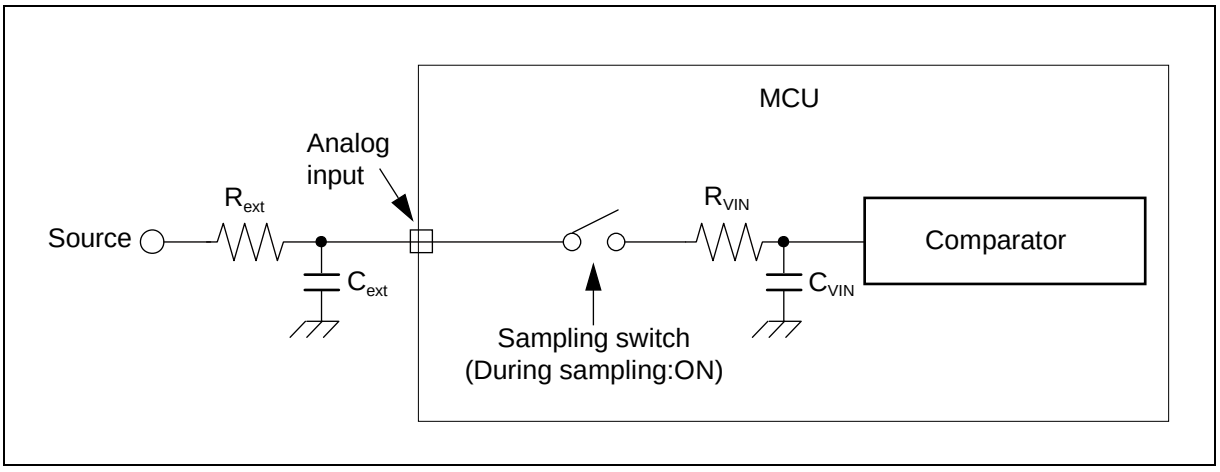
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
Reset input time	t_{RSTL}	RSTX	10	-	µs
Rejection of reset input time			1	-	µs



14.5.2 Accuracy and Setting of the A/D Converter Sampling Time

If the external impedance is too high or the sampling time too short, the analog voltage charged to the internal sample and hold capacitor is insufficient, adversely affecting the A/D conversion precision.

To satisfy the A/D conversion precision, a sufficient sampling time must be selected. The required sampling time (Tsamp) depends on the external driving impedance R_{ext}, the board capacitance of the A/D converter input pin C_{ext} and the AV_{CC} voltage level. The following replacement model can be used for the calculation:



R_{ext}: External driving impedance

C_{ext}: Capacitance of PCB at A/D converter input

C_{VIN}: Analog input capacity (I/O, analog switch and ADC are contained)

R_{VIN}: Analog input impedance (I/O, analog switch and ADC are contained)

The following approximation formula for the replacement model above can be used:

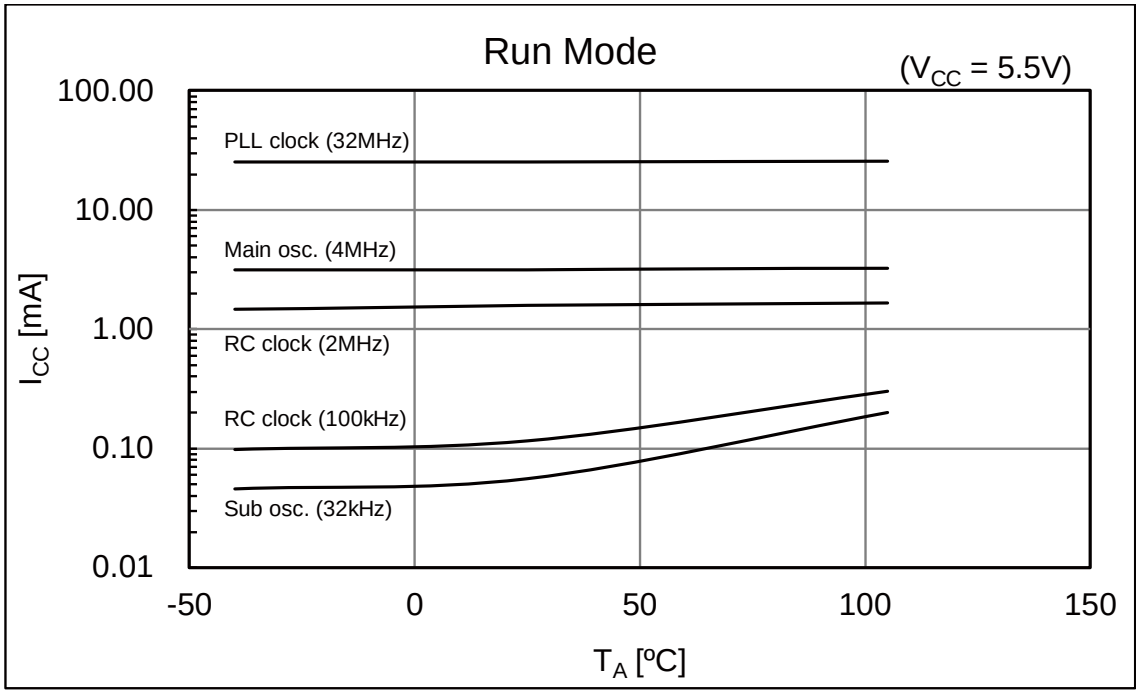
$Tsamp = 7.62 \times (Rext \times Cext + (Rext + R_{VIN}) \times C_{VIN})$

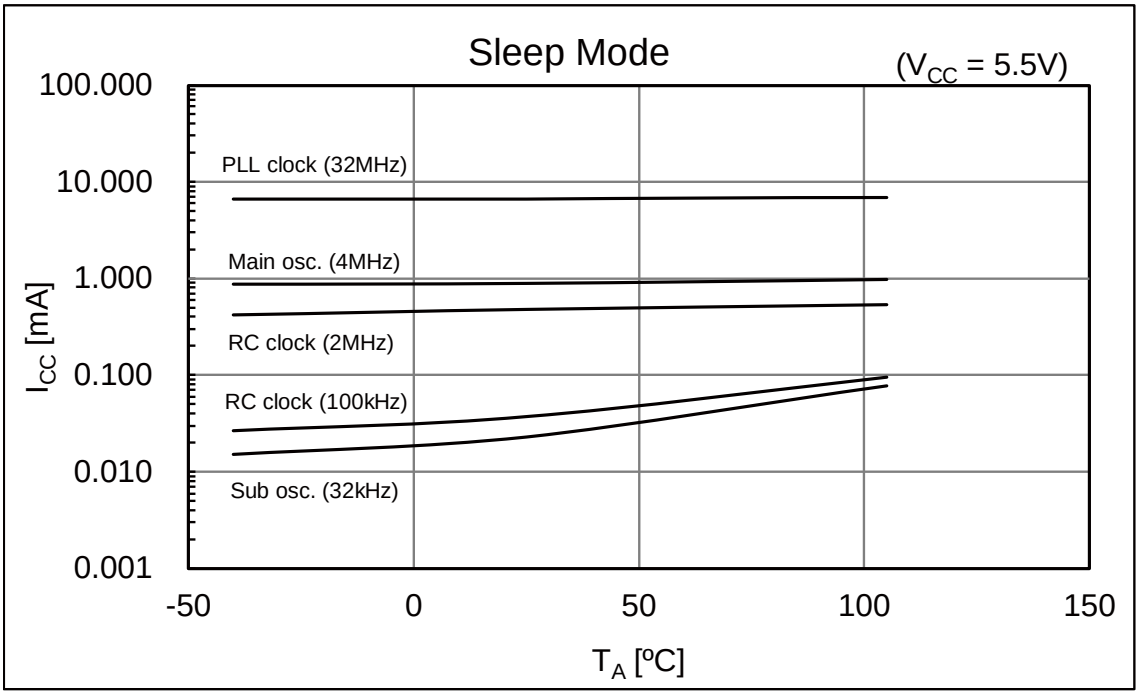
- Do not select a sampling time below the absolute minimum permitted value.
  ($0.5\mu s$ for $4.5V \le AV_{CC} \le 5.5V$, $1.2\mu s$ for $2.7V \le AV_{CC} < 4.5V$)
- If the sampling time cannot be sufficient, connect a capacitor of about $0.1\mu F$ to the analog input pin.
- A big external driving impedance also adversely affects the A/D conversion precision due to the pin input leakage current IIL (static current before the sampling switch) or the analog input leakage current IAIN (total leakage current of pin input and comparator during sampling). The effect of the pin input leakage current IIL cannot be compensated by an external capacitor.
- The accuracy gets worse as $|AVRH - AV_{SS}|$ becomes smaller.

15. Example Characteristics

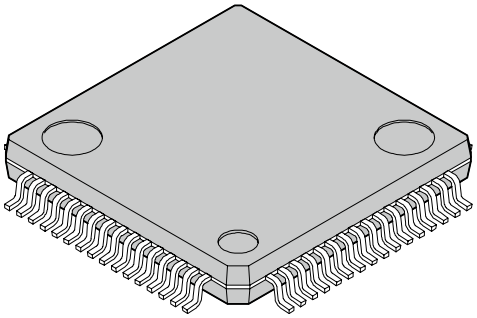
This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■MB96F625





64-pin plastic LQFP

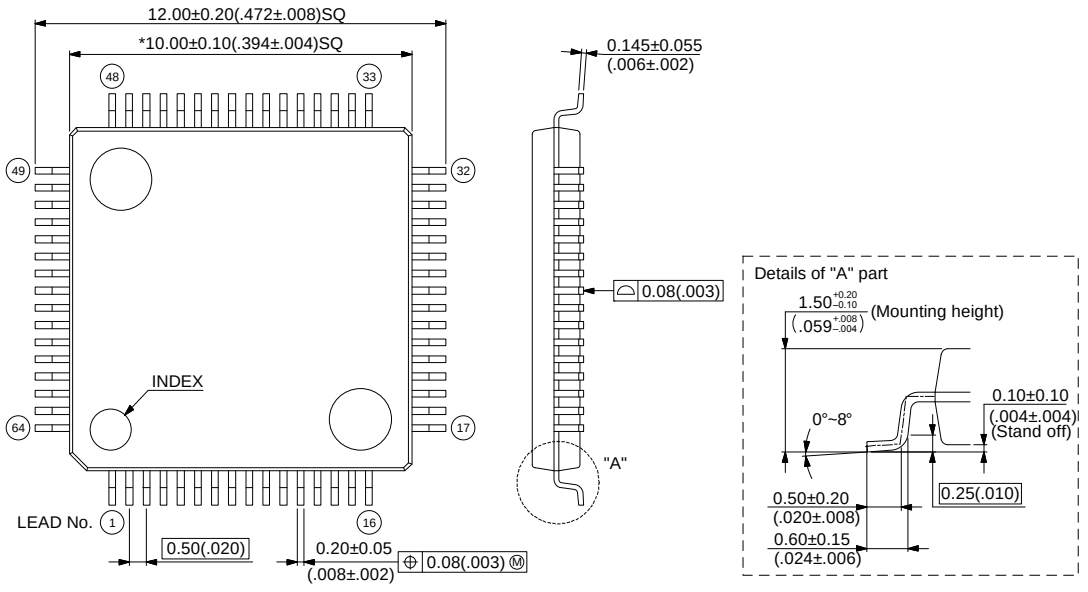


(FPT-64P-M24)

Lead pitch	0.50 mm
Package width × package length	10.0 × 10.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Weight	0.32 g
Code (Reference)	P-LFQFP64-10×10-0.50

64-pin plastic LQFP
(FPT-64P-M24)

Note 1) * : These dimensions do not include resin protrusion.
Note 2) Pins width and pins thickness include plating thickness.
Note 3) Pins width do not include tie bar cutting remainder.



Dimensions in mm (inches).
Note: The values in parentheses are reference values

18. Major Changes

Spansion Publication Number: MB96620_DS704-00008

Page	Section	Change Results
Revision 2.0		
4	Features	Changed the description of “External Interrupts” Interrupt mask and pending bit per channel → Interrupt mask bit per channel
25 to 28	Handling Precautions	Added a section
36	Electrical Characteristics 3. Dc Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz, → CLKS1/2 = CLKP1/2 = CLKRC = 2MHz,
		Changed the Conditions for I_{CCSRCL} CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz → CLKS1/2 = CLKP1/2 = CLKRC = 100kHz
37		Changed the Conditions for I_{CCTPLL} PLL Timer mode with CLKP1 = 32MHz → PLL Timer mode with CLKPLL = 32MHz
		Changed the Value of “Power supply current in Timer modes” I_{CCTPLL} Typ: 2480µA → 1800µA (T_A = +25°C) Max: 2710µA → 2245µA (T_A = +25°C) Max: 3985µA → 3165µA (T_A = +105°C) Max: 4830µA → 3975µA (T_A = +125°C)
		Changed the Conditions for I_{CCTRCL} RC Timer mode with CLKRC = 100kHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped) → RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)
38		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. → The current for "On Chip Debugger" part is not included.
49	4. Ac Characteristics (10) I^2c Timing	Added parameter, “Noise filter” and an annotation *5 for it
		Added t_{SP} to the figure
51	5. A/D Converter (2) Accuracy And Setting Of The A/D Converter Sampling Time	Deleted the unit “[Min]” from approximation formula of Sampling time
56	7. Flash Memory Write/Erase Characteristics	Changed the condition (V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C) → (V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)