

Welcome to [E-XFL.COM](https://www.e-xfl.com)

### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

#### Details

Product Status	Obsolete
Core Processor	F <sup>2</sup> MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/infineon-technologies/mb96f623abpmc1-gse1">https://www.e-xfl.com/product-detail/infineon-technologies/mb96f623abpmc1-gse1</a>

**■ A/D converter**

- SAR-type
- 8/10-bit resolution
- Signals interrupt on conversion end, single conversion mode, continuous conversion mode, stop conversion mode, activation by software, external trigger, reload timers and PPGs
- Range Comparator Function

**■ Source Clock Timers**

Three independent clock timers (23-bit RC clock timer, 23-bit Main clock timer, 17-bit Sub clock timer)

**■ Hardware Watchdog Timer**

- Hardware watchdog timer is active after reset
- Window function of Watchdog Timer is used to select the lower window limit of the watchdog interval

**■ Reload Timers**

- 16-bit wide
- Prescaler with  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$  of peripheral clock frequency
- Event count function

**■ Free-Running Timers**

- Signals an interrupt on overflow, supports timer clear upon match with Output Compare (0, 4)
- Prescaler with  $1$ ,  $1/2^1$ ,  $1/2^2$ ,  $1/2^3$ ,  $1/2^4$ ,  $1/2^5$ ,  $1/2^6$ ,  $1/2^7$ ,  $1/2^8$  of peripheral clock frequency

**■ Input Capture Units**

- 16-bit wide
- Signals an interrupt upon external event
- Rising edge, Falling edge or Both (rising & falling) edges sensitive

**■ Output Compare Units**

- 16-bit wide
- Signals an interrupt when a match with Free-running Timer occurs
- A pair of compare registers can be used to generate an output signal

**■ Programmable Pulse Generator**

- 16-bit down counter, cycle and duty setting registers
- Can be used as  $2 \times 8$ -bit PPG
- Interrupt at trigger, counter borrow and/or duty match
- PWM operation and one-shot operation
- Internal prescaler allows  $1$ ,  $1/4$ ,  $1/16$ ,  $1/64$  of peripheral clock as counter clock or of selected Reload timer underflow as clock input
- Can be triggered by software or reload timer
- Can trigger ADC conversion
- Timing point capture

**■ Quadrature Position/Revolution Counter (QPRC)**

- Up/down count mode, Phase difference count mode, Count mode with direction
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers with interrupt
- Detection edge of the three external event input pins AIN, BIN and ZIN is configurable

**■ Real Time Clock**

- Operational on main oscillation (4MHz), sub oscillation (32kHz) or RC oscillation (100kHz/2MHz)
- Capable to correct oscillation deviation of Sub clock or RC oscillator clock (clock calibration)
- Read/write accessible second/minute/hour registers
- Can signal interrupts every half second/second/minute/hour/day
- Internal clock divider and prescaler provide exact 1s clock

**■ External Interrupts**

- Edge or Level sensitive
- Interrupt mask bit per channel
- Each available CAN channel RX has an external interrupt for wake-up
- Selected USART channels SIN have an external interrupt for wake-up

**■ Non Maskable Interrupt**

- Disabled after reset, can be enabled by Boot-ROM depending on ROM configuration block
- Once enabled, can not be disabled other than by reset
- High or Low level sensitive
- Pin shared with external interrupt 0

**■ I/O Ports**

- Most of the external pins can be used as general purpose I/O
- All push-pull outputs (except when used as I<sup>2</sup>C SDA/SCL line)
- Bit-wise programmable as input/output or peripheral signal
- Bit-wise programmable input enable
- One input level per GPIO-pin (either Automotive or CMOS hysteresis)
- Bit-wise programmable pull-up resistor

**■ Built-in On Chip Debugger (OCD)**

- One-wire debug tool interface
- Break function:
  - Hardware break: 6 points (shared with code event)
  - Software break: 4096 points
- Event function
  - Code event: 6 points (shared with hardware break)
  - Data event: 6 points
  - Event sequencer: 2 levels + reset
- Execution time measurement function
- Trace function: 42 branches
- Security function

**■ Flash Memory**

- Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
- Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
- Supports automatic programming, Embedded Algorithm
- Write/Erase/Erase-Suspend/Resume commands
- A flag indicating completion of the automatic algorithm
- Erase can be performed on each sector individually
- Sector protection
- Flash Security feature to protect the content of the Flash
- Low voltage detection during Flash erase or write

## 1. Product Lineup

Features		MB96620	Remark
Product Type		Flash Memory Product	
Subclock		Subclock can be set by software	
Dual Operation Flash Memory	RAM	-	
32.5KB + 32KB	4KB	MB96F622R, MB96F622A	Product Options R: MCU with CAN A: MCU without CAN
64.5KB + 32KB	10KB	MB96F623R, MB96F623A	
128.5KB + 32KB	10KB	MB96F625R, MB96F625A	
Package		LQFP-64 FPT-64P-M23/M24	
DMA		2ch	
USART		3ch	LIN-USART 2/7/8
	with automatic LIN-Header transmission/reception	Yes (only 1ch)	LIN-USART 2
	with 16 byte RX- and TX-FIFO	No	
I <sup>2</sup> C		1ch	I <sup>2</sup> C 0
8/10-bit A/D Converter		21ch	AN 0 to 14/24/25/28 to 31
	with Data Buffer	No	
	with Range Comparator	Yes	
	with Scan Disable	No	
	with ADC Pulse Detection	No	
16-bit Reload Timer (RLT)		3ch	RLT 1/3/6
16-bit Free-Running Timer (FRT)		4ch	FRT 0 to 3 FRT 2/3 does not have external clock input pin
16-bit Input Capture Unit (ICU)		8ch (2 channels for LIN-USART)	ICU 0/1/4 to 7/9/10 (ICU 9/10 for LIN-USART)
16-bit Output Compare Unit (OCU)		6ch	OCU 0/1/4 to 7
8/16-bit Programmable Pulse Generator (PPG)		8ch (16-bit) / 16ch (8-bit)	PPG 0/1/3/4/6/7/12/14
	with Timing point capture	Yes	
	with Start delay	No	
	with Ramp	No	
Quadrature Position/Revolution Counter (QPRC)		2ch	QPRC 0/1
CAN Interface		1ch	CAN 2 32 Message Buffers
External Interrupts (INT)		13ch	INT 0/2/3/4/7 to 15
Non-Maskable Interrupt (NMI)		1ch	
Real Time Clock (RTC)		1ch	
I/O Ports		50 (Dual clock mode) 52 (Single clock mode)	
Clock Calibration Unit (CAL)		1ch	
Clock Output Function		2ch	
Low Voltage Detection Function		Yes	Low voltage detection function can be disabled by software
Hardware Watchdog Timer		Yes	
On-chip RC-oscillator		Yes	
On-chip Debugger		Yes	

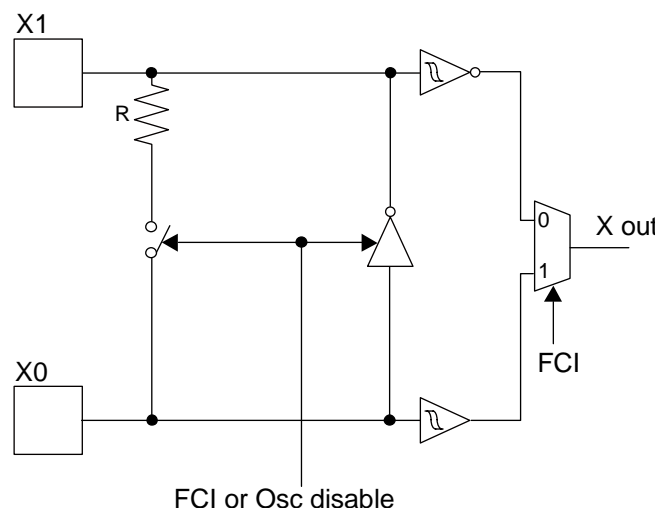
### Note:

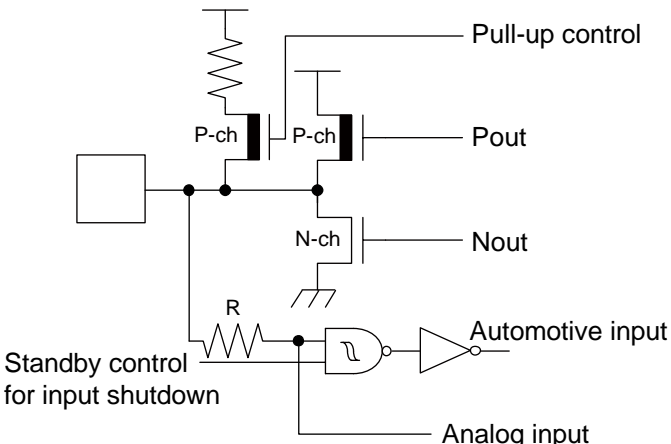
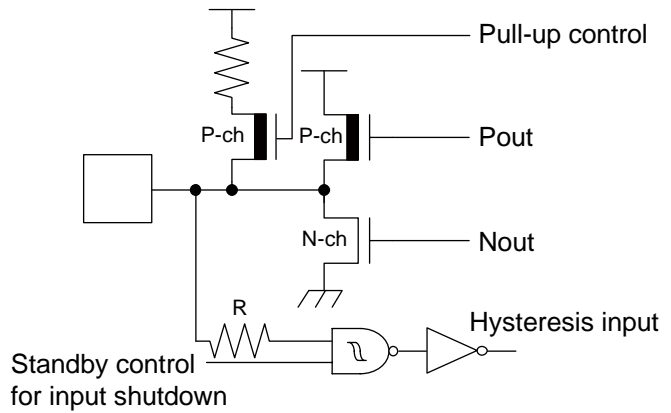
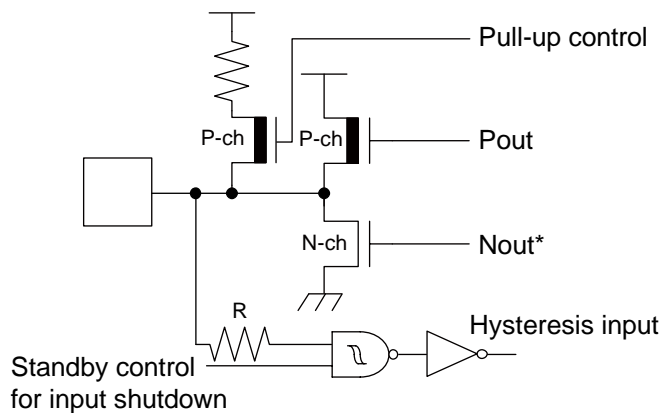
All signals of the peripheral function in each product cannot be allocated by limiting the pins of package.  
It is necessary to use the port relocate function of the general I/O port according to your function use.

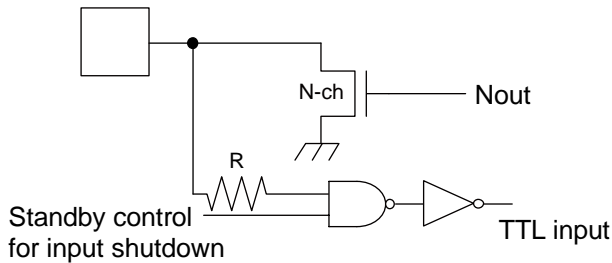
## 4. Pin Description

Pin name	Feature	Description
ADTG_R	ADC	Relocated A/D converter trigger input pin
AINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
ANn	ADC	A/D converter channel n input pin
AVcc	Supply	Analog circuits power supply pin
AVRH	ADC	A/D converter high reference voltage input pin
AVss	Supply	Analog circuits power supply pin
BINn	QPRC	Quadrature Position/Revolution Counter Unit n input pin
C	Voltage regulator	Internally regulated power supply stabilization capacitor pin
CKOTn	Clock Output function	Clock Output function n output pin
CKOTn_R	Clock Output function	Relocated Clock Output function n output pin
CKOTXn	Clock Output function	Clock Output function n inverted output pin
DEBUG I/F	OCD	On Chip Debugger input/output pin
FRCKn	Free-Running Timer	Free-Running Timer n input pin
INn	ICU	Input Capture Unit n input pin
INTn	External Interrupt	External Interrupt n input pin
INTn_R	External Interrupt	Relocated External Interrupt n input pin
INTn_R1	External Interrupt	Relocated External Interrupt n input pin
MD	Core	Input pin for specifying the operating mode
NMI_R	External Interrupt	Relocated Non-Maskable Interrupt input pin
OUTn	OCU	Output Compare Unit n waveform output pin
OUTn_R	OCU	Relocated Output Compare Unit n waveform output pin
Pnn_m	GPIO	General purpose I/O pin
PPGn	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
PPGn_B	PPG	Programmable Pulse Generator n output pin (16bit/8bit)
RSTX	Core	Reset input pin
RXn	CAN	CAN interface n RX input pin
SCKn	USART	USART n serial clock input/output pin
SCKn_R	USART	Relocated USART n serial clock input/output pin
SCLn	I <sup>2</sup> C	I <sup>2</sup> C interface n clock I/O input/output pin
SDAn	I <sup>2</sup> C	I <sup>2</sup> C interface n serial data I/O input/output pin
SINn	USART	USART n serial data input pin
SINn_R	USART	Relocated USART n serial data input pin
SOTn	USART	USART n serial data output pin
SOTn_R	USART	Relocated USART n serial data output pin
TINn	Reload Timer	Reload Timer n event input pin
TOTn	Reload Timer	Reload Timer n output pin
TTGn	PPG	Programmable Pulse Generator n trigger input pin
TXn	CAN	CAN interface n TX output pin
Vcc	Supply	Power supply pin
Vss	Supply	Power supply pin

## 6. I/O Circuit Type

Type	Circuit	Remarks
A	 <p>FCI or Osc disable</p>	<p>High-speed oscillation circuit:</p> <ul style="list-style-type: none"> <li>• Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin)</li> <li>• Feedback resistor = approx. <math>1.0\text{M}\Omega</math></li> <li>• The amplitude: <math>1.8\text{V}\pm 0.15\text{V}</math> to operate by the internal supply voltage</li> </ul>

Type	Circuit	Remarks
K	 <p>Pull-up control</p> <p>P-ch</p> <p>Pout</p> <p>N-ch</p> <p>Nout</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Automotive input</p> <p>Analog input</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• Automotive input with input shutdown function</li> <li>• Programmable pull-up resistor</li> <li>• Analog input</li> </ul>
M	 <p>Pull-up control</p> <p>P-ch</p> <p>Pout</p> <p>N-ch</p> <p>Nout</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 4\text{mA}</math>, <math>I_{OH} = -4\text{mA}</math>)</li> <li>• CMOS hysteresis input with input shutdown function</li> <li>• Programmable pull-up resistor</li> </ul>
N	 <p>Pull-up control</p> <p>P-ch</p> <p>Pout</p> <p>N-ch</p> <p>Nout*</p> <p>R</p> <p>Standby control for input shutdown</p> <p>Hysteresis input</p>	<ul style="list-style-type: none"> <li>• CMOS level output (<math>I_{OL} = 3\text{mA}</math>, <math>I_{OH} = -3\text{mA}</math>)</li> <li>• CMOS hysteresis input with input shutdown function</li> <li>• Programmable pull-up resistor</li> </ul> <p>*: N-channel transistor has slew rate control according to I<sup>2</sup>C spec, irrespective of usage.</p>

Type	Circuit	Remarks
O	 <p>Standby control for input shutdown</p> <p>TTL input</p> <p>N-ch</p> <p>Nout</p> <p>R</p>	<ul style="list-style-type: none"> <li>• Open-drain I/O</li> <li>• Output 25mA, <math>V_{CC} = 2.7V</math></li> <li>• TTL input</li> </ul>

**8. RAMSTART Addresses**

Devices	Bank 0 RAM size	RAMSTART0
MB96F622	4KB	00:7200 <sub>H</sub>
MB96F623 MB96F625	10KB	00:5A00 <sub>H</sub>



## 10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96620		
Pin Number	USART Number	Normal Function
9	USART2	SIN2
10		SOT2
11		SCK2
26	USART7	SIN7_R
25		SOT7_R
24		SCK7_R
29	USART8	SIN8_R
28		SOT8_R
27		SCK8_R

#### ■ Precautions Related to Usage of Devices

Cypress semiconductor devices are intended for use in standard applications (computers, office automation and other office equipment, industrial, communications, and measurement equipment, personal or household devices, etc.).

CAUTION: Customers considering the use of our products in special applications where failure or abnormal operation may directly affect human lives or cause physical injury or property damage, or where extremely high levels of reliability are demanded (such as aerospace systems, atomic energy controls, sea floor repeaters, vehicle operating controls, medical devices for life support, etc.) are requested to consult with sales representatives before such use. The company will not be responsible for damages arising from such use without prior approval.

### 12.2 Precautions for Package Mounting

Package mounting may be either lead insertion type or surface mount type. In either case, for heat resistance during soldering, you should only mount under Cypress's recommended conditions. For detailed information about mount conditions, contact your sales representative.

#### ■ Lead Insertion Type

Mounting of lead insertion type packages onto printed circuit boards may be done by two methods: direct soldering on the board, or mounting by using a socket.

Direct mounting onto boards normally involves processes for inserting leads into through-holes on the board and using the flow soldering (wave soldering) method of applying liquid solder. In this case, the soldering process usually causes leads to be subjected to thermal stress in excess of the absolute ratings for storage temperature. Mounting processes should conform to Cypress recommended mounting conditions.

If socket mounting is used, differences in surface treatment of the socket contacts and IC lead surfaces can lead to contact deterioration after long periods. For this reason it is recommended that the surface treatment of socket contacts and IC leads be verified before mounting.

#### ■ Surface Mount Type

Surface mount packaging has longer and thinner leads than lead-insertion packaging, and therefore leads are more easily deformed or bent. The use of packages with higher pin counts and narrower pin pitch results in increased susceptibility to open connections caused by deformed pins, or shorting due to solder bridges.

You must use appropriate mounting techniques. Cypress recommends the solder reflow method, and has established a ranking of mounting conditions for each product. Users are advised to mount packages in accordance with Cypress ranking of recommended conditions.

#### ■ Lead-Free Packaging

CAUTION: When ball grid array (BGA) packages with Sn-Ag-Cu balls are mounted using Sn-Pb eutectic soldering, junction strength may be reduced under some conditions of use.

#### ■ Storage of Semiconductor Devices

Because plastic chip packages are formed from plastic resins, exposure to natural environmental conditions will cause absorption of moisture. During mounting, the application of heat to a package that has absorbed moisture can cause surfaces to peel, reducing moisture resistance and causing packages to crack. To prevent, do the following:

1. Avoid exposure to rapid temperature changes, which cause moisture to condense inside the product. Store products in locations where temperature changes are slight.
2. Use dry boxes for product storage. Products should be stored below 70% relative humidity, and at temperatures between 5°C and 30°C.  
When you open Dry Package that recommends humidity 40% to 70% relative humidity.
3. When necessary, Cypress packages semiconductor devices in highly moisture-resistant aluminum laminate bags, with a silica gel desiccant. Devices should be sealed in their aluminum laminate bags for storage.
4. Avoid storing packages where they are exposed to corrosive gases or high levels of dust.

#### ■ Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the Cypress recommended conditions for baking.

Condition: 125°C/24 h

## 13. Handling Devices

**Special care is required for the following when handling the device:**

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins ( $V_{CC}/V_{SS}$ )
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)

### 13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than  $V_{CC}$  or lower than  $V_{SS}$  is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between  $V_{CC}$  pins and  $V_{SS}$  pins.
- The  $AV_{CC}$  power supply is applied before the  $V_{CC}$  voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage ( $AV_{CC}$ ,  $AVRH$ ) exceed the digital power-supply voltage.

### 13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register  $PIER = 0$ ).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than  $2k\Omega$ .

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

### 13.6 Crystal oscillator and ceramic resonator circuit

Noise at X0, X1 pins or X0A, X1A pins might cause abnormal operation. It is required to provide bypass capacitors with shortest possible distance to X0, X1 pins and X0A, X1A pins, crystal oscillator (or ceramic resonator) and ground lines, and, to the utmost effort, that the lines of oscillation circuit do not cross the lines of other circuits.

It is highly recommended to provide a printed circuit board artwork surrounding X0, X1 pins and X0A, X1A pins with a ground area for stabilizing the operation.

It is highly recommended to evaluate the quartz/MCU or resonator/MCU system at the quartz or resonator manufacturer, especially when using low-Q resonators at higher frequencies.

### 13.7 Turn on sequence of power supply to A/D converter and analog inputs

It is required to turn the A/D converter power supply ( $AV_{CC}$ ,  $AVRH$ ) and analog inputs ( $ANn$ ) on after turning the digital power supply ( $V_{CC}$ ) on.

It is also required to turn the digital power off after turning the A/D converter supply and analog inputs off. In this case,  $AVRH$  must not exceed  $AV_{CC}$ . Input voltage for ports shared with analog input ports also must not exceed  $AV_{CC}$  (turning the analog and digital power supplies simultaneously on or off is acceptable).

### 13.8 Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as  $AV_{CC} = V_{CC}$ ,  $AV_{SS} = AVRH = V_{SS}$ .

### 13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50 $\mu$ s from 0.2V to 2.7V.

### 13.10 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the  $V_{CC}$  power supply voltage, a malfunction may occur. The  $V_{CC}$  power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that  $V_{CC}$  ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard  $V_{CC}$  power supply voltage and the transient fluctuation rate becomes 0.1V/ $\mu$ s or less in instantaneous fluctuation for power supply switching.

### 13.11 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

### 13.12 Mode Pin (MD)

Connect the mode pin directly to  $V_{CC}$  or  $V_{SS}$  pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to  $V_{CC}$  or  $V_{SS}$  pin and provide a low-impedance connection.

## 14.2 Recommended Operating Conditions

( $V_{SS} = AV_{SS} = 0V$ )

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{CC}, AV_{CC}$	2.7	-	5.5	V	
		2.0	-	5.5	V	Maintains RAM data in stop mode
Smoothing capacitor at C pin	$C_S$	0.5	1.0 to 3.9	4.7	$\mu F$	1.0 $\mu F$ (Allowance within $\pm 50\%$ ) 3.9 $\mu F$ (Allowance within $\pm 20\%$ ) Please use the ceramic capacitor or the capacitor of the frequency response of this level. The smoothing capacitor at $V_{CC}$ must use the one of a capacity value that is larger than $C_S$ .

### WARNING

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure. No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes <sup>*2</sup>	I <sub>CCTPLL</sub>	V <sub>CC</sub>	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2245	μA	T <sub>A</sub> = +25°C
				-	-	3165	μA	T <sub>A</sub> = +105°C
				-	-	3975	μA	T <sub>A</sub> = +125°C
	I <sub>CCTMAIN</sub>		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	325	μA	T <sub>A</sub> = +25°C
				-	-	1085	μA	T <sub>A</sub> = +105°C
				-	-	1930	μA	T <sub>A</sub> = +125°C
	I <sub>CCTRCH</sub>		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	210	μA	T <sub>A</sub> = +25°C
				-	-	1025	μA	T <sub>A</sub> = +105°C
				-	-	1840	μA	T <sub>A</sub> = +125°C
	I <sub>CCTRCL</sub>		RC Timer mode with CLKRC = 100kHz (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	μA	T <sub>A</sub> = +25°C
				-	-	855	μA	T <sub>A</sub> = +105°C
				-	-	1640	μA	T <sub>A</sub> = +125°C
	I <sub>CCTSUB</sub>		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	μA	T <sub>A</sub> = +25°C
				-	-	830	μA	T <sub>A</sub> = +105°C
				-	-	1620	μA	T <sub>A</sub> = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V <sub>OH4</sub>	4mA type	4.5V ≤ V <sub>CC</sub> ≤ 5.5V I <sub>OH</sub> = -4mA	V <sub>CC</sub> - 0.5	-	V <sub>CC</sub>	V	
			2.7V ≤ V <sub>CC</sub> < 4.5V I <sub>OH</sub> = -1.5mA					
	V <sub>OH3</sub>	3mA type	4.5V ≤ V <sub>CC</sub> ≤ 5.5V I <sub>OH</sub> = -3mA	V <sub>CC</sub> - 0.5	-	V <sub>CC</sub>	V	
			2.7V ≤ V <sub>CC</sub> < 4.5V I <sub>OH</sub> = -1.5mA					
"L" level output voltage	V <sub>OL4</sub>	4mA type	4.5V ≤ V <sub>CC</sub> ≤ 5.5V I <sub>OL</sub> = +4mA	-	-	0.4	V	
			2.7V ≤ V <sub>CC</sub> < 4.5V I <sub>OL</sub> = +1.7mA					
	V <sub>OL3</sub>	3mA type	2.7V ≤ V <sub>CC</sub> < 5.5V I <sub>OL</sub> = +3mA	-	-	0.4	V	
	V <sub>OLD</sub>	DEBUG I/F	V <sub>CC</sub> = 2.7V I <sub>OL</sub> = +25mA	0	-	0.25	V	
Input leak current	I <sub>IL</sub>	Pnn_m	V <sub>SS</sub> < V <sub>I</sub> < V <sub>CC</sub> AV <sub>SS</sub> < V <sub>I</sub> < AV <sub>CC</sub> , AVR <sub>H</sub>	- 1	-	+ 1	μA	
Pull-up resistance value	R <sub>PU</sub>	Pnn_m	V <sub>CC</sub> = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C <sub>IN</sub>	Other than C, V <sub>CC</sub> , V <sub>SS</sub> , AV <sub>CC</sub> , AV <sub>SS</sub> , AVR <sub>H</sub>	-	-	5	15	pF	

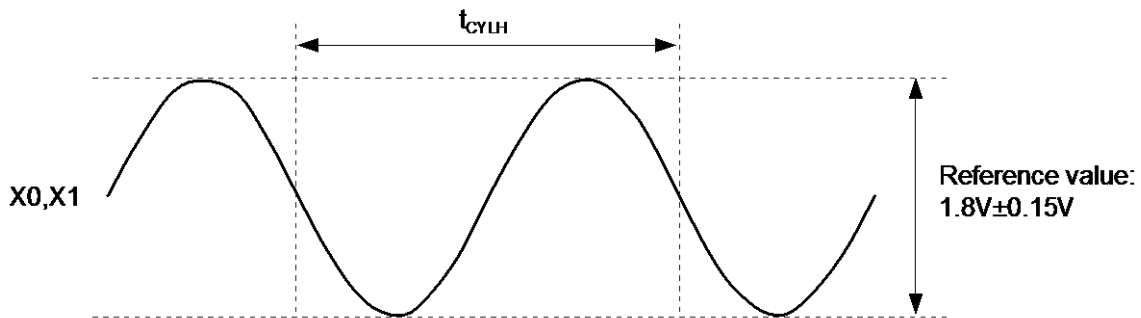
## 14.4 AC Characteristics

### 14.4.1 Main Clock Input Characteristics

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_D = 1.8V \pm 0.15V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^\circ C$  to  $+125^\circ C$ )

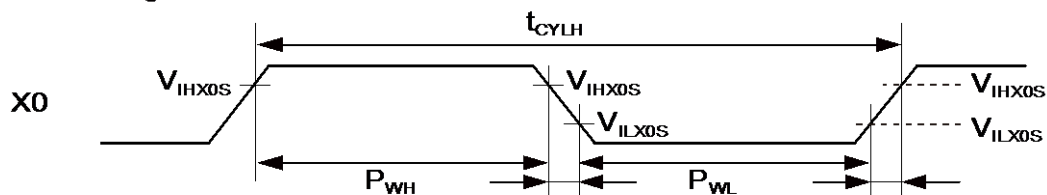
Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	$f_c$	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	$f_{FCI}$	X0	-	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL off
			4	-	8	MHz	When using a single phase external clock in "Fast Clock Input mode", PLL on
Input clock cycle	$t_{CYLH}$	-	125	-	-	ns	
Input clock pulse width	$P_{WH}, P_{WL}$	-	55	-	-	ns	

#### When using the crystal oscillator



The amplitude changes by resistance, capacity which added outside or the difference of the device.

#### When using the external clock

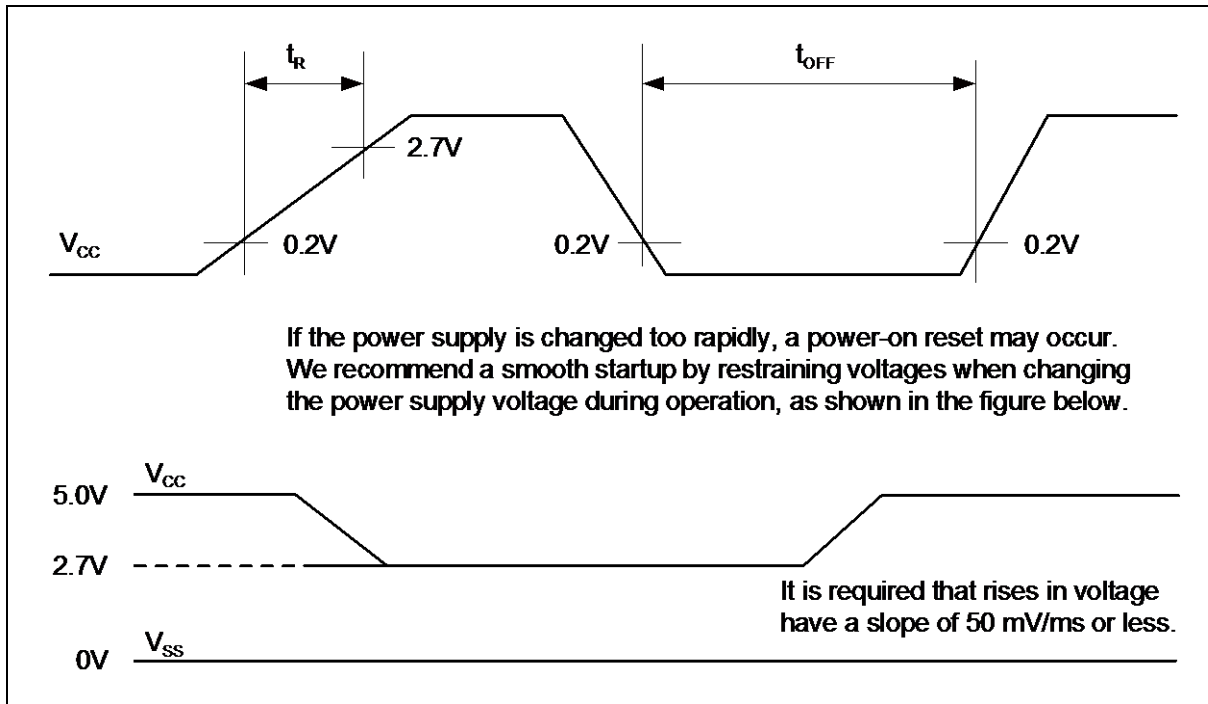




#### 14.4.7 Power-on Reset Timing

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ )

Parameter	Symbol	Pin name	Value			Unit
			Min	Typ	Max	
Power on rise time	$t_R$	$V_{CC}$	0.05	-	30	ms
Power off time	$t_{OFF}$	$V_{CC}$	1	-	-	ms



#### 14.4.8 USART Timing

( $V_{CC} = AV_{CC} = 2.7V$  to  $5.5V$ ,  $V_{SS} = AV_{SS} = 0V$ ,  $T_A = -40^{\circ}C$  to  $+125^{\circ}C$ ,  $C_L = 50pF$ )

Parameter	Symbol	Pin name	Conditions	$4.5V \leq V_{CC} < 5.5V$		$2.7V \leq V_{CC} < 4.5V$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	$t_{SCYC}$	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVI}$	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT $\rightarrow$ SCK $\uparrow$ delay time	$t_{OVSHI}$	SCKn, SOTn		$N \times t_{CLKP1} - 20$	-	$N \times t_{CLKP1} - 30$	-	ns
SIN $\rightarrow$ SCK $\uparrow$ setup time	$t_{IVSHI}$	SCKn, SINn		$t_{CLKP1} + 45$	-	$t_{CLKP1} + 55$	-	ns
SCK $\uparrow \rightarrow$ SIN hold time	$t_{SHIXI}$	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	$t_{SLSH}$	SCKn	External shift clock mode	$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
Serial clock "H" pulse width	$t_{SHSL}$	SCKn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK $\downarrow \rightarrow$ SOT delay time	$t_{SLOVE}$	SCKn, SOTn		-	$2t_{CLKP1} + 45$	-	$2t_{CLKP1} + 55$	ns
SIN $\rightarrow$ SCK $\uparrow$ setup time	$t_{IVSHE}$	SCKn, SINn		$t_{CLKP1}/2 + 10$	-	$t_{CLKP1}/2 + 10$	-	ns
SCK $\uparrow \rightarrow$ SIN hold time	$t_{SHIXE}$	SCKn, SINn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK fall time	$t_F$	SCKn		-	20	-	20	ns
SCK rise time	$t_R$	SCKn		-	20	-	20	ns

#### Notes:

- AC characteristic in CLK synchronized mode.
- $C_L$  is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96600 series HARDWARE MANUAL".
- $t_{CLKP1}$  indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.  
For example, the combination of SCKn and SOTn\_R is not guaranteed.

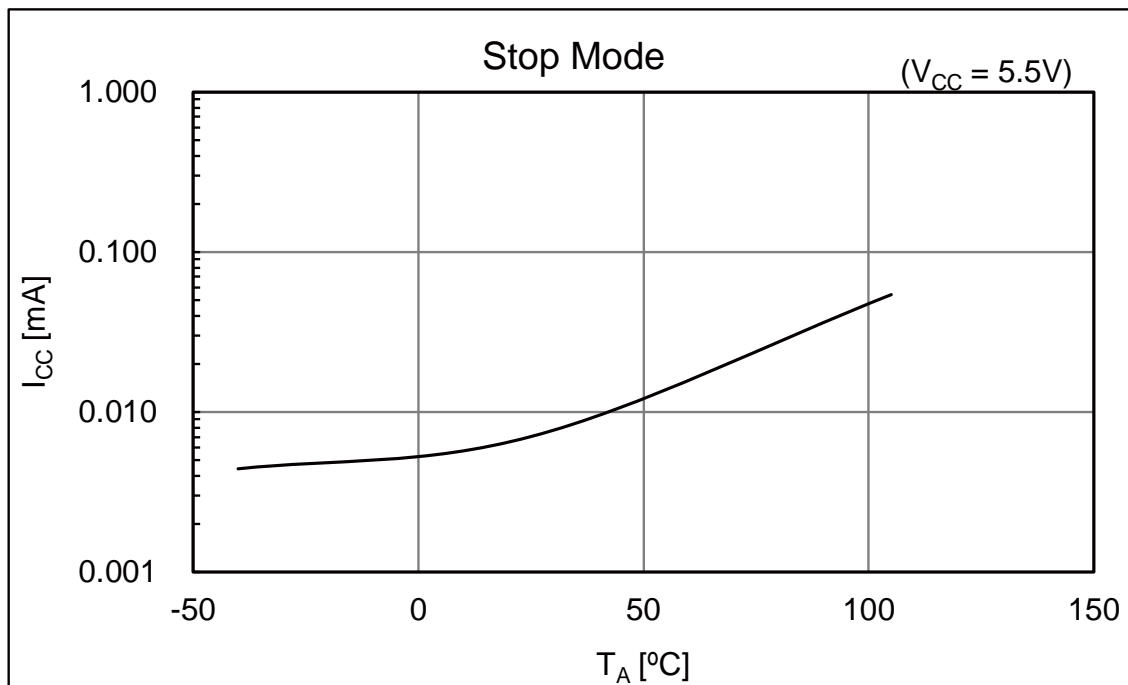
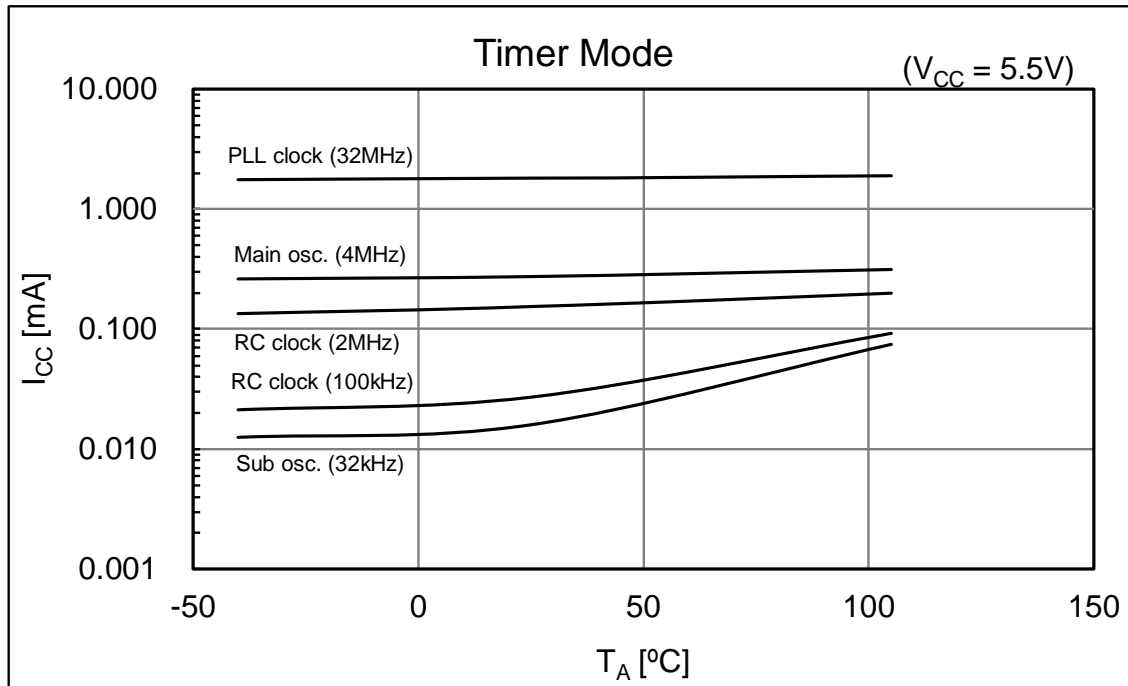
\*: Parameter N depends on  $t_{SCYC}$  and can be calculated as follows:

- If  $t_{SCYC} = 2 \times k \times t_{CLKP1}$ , then  $N = k$ , where k is an integer  $> 2$
- If  $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$ , then  $N = k + 1$ , where k is an integer  $> 1$

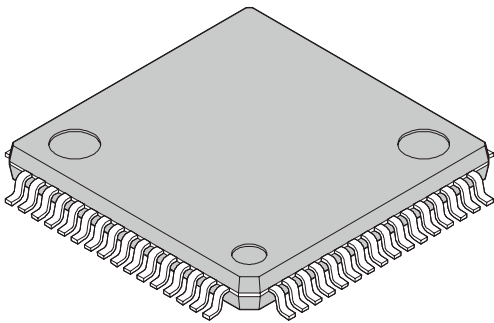
Examples:

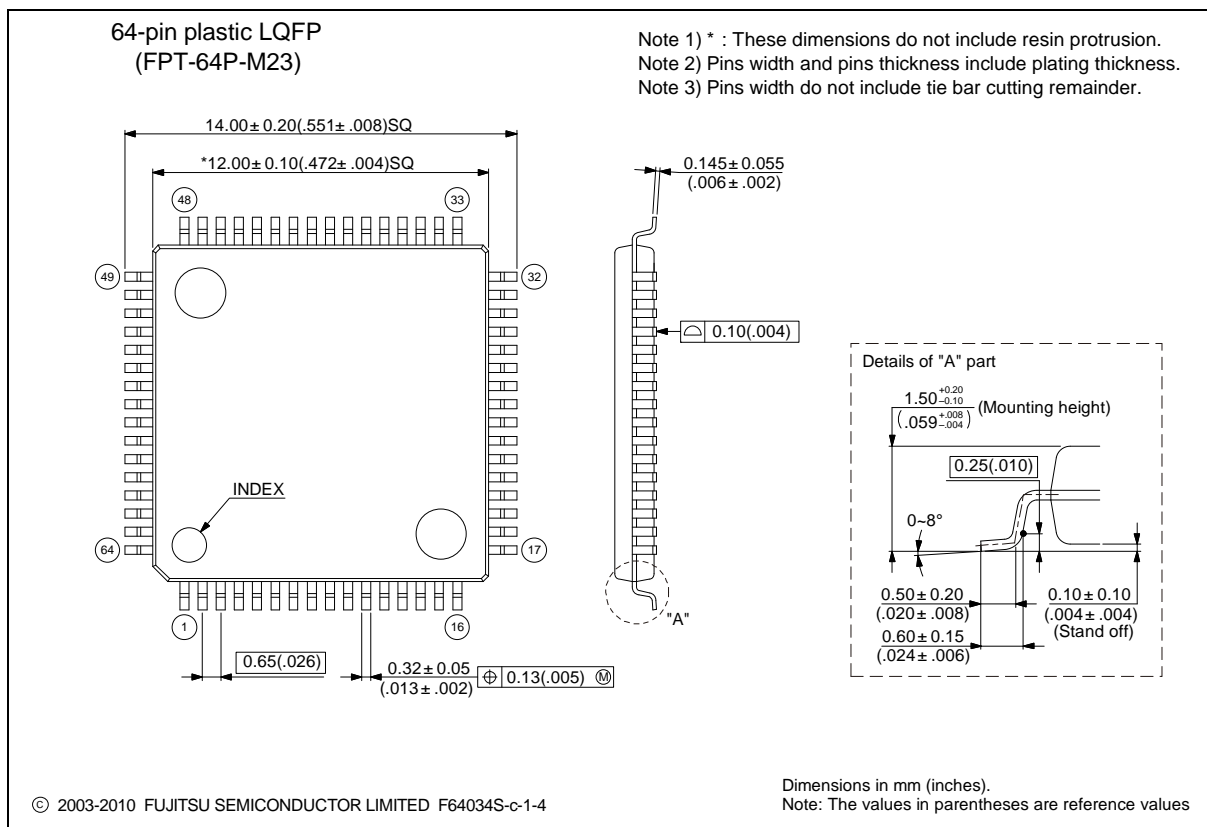
$t_{scyc}$	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}, 6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}, 8 \times t_{CLKP1}$	4
...	...

■ MB96F625



## 17. Package Dimension

 <p>64-pin plastic LQFP</p> <p>(FPT-64P-M23)</p>	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
	Code (Reference)	P-LQFP64-12 × 12-0.65



## 18. Major Changes

Spanion Publication Number: MB96620\_DS704-00008

Page	Section	Change Results
Revision 2.0		
4	Features	Changed the description of "External Interrupts" Interrupt mask and pending bit per channel → Interrupt mask bit per channel
25 to 28	Handling Precautions	Added a section
36	Electrical Characteristics 3. Dc Characteristics (1) Current Rating	Changed the Conditions for $I_{CCSRCH}$ $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz$ , → $CLKS1/2 = CLKP1/2 = CLKRC = 2MHz$ ,
		Changed the Conditions for $I_{CCSRCL}$ $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz$ → $CLKS1/2 = CLKP1/2 = CLKRC = 100kHz$
37		Changed the Conditions for $I_{CCTPLL}$ PLL Timer mode with $CLKP1 = 32MHz$ → PLL Timer mode with $CLKPLL = 32MHz$
		Changed the Value of "Power supply current in Timer modes" $I_{CCTPLL}$ Typ: $2480\mu A \rightarrow 1800\mu A$ ( $T_A = +25^\circ C$ ) Max: $2710\mu A \rightarrow 2245\mu A$ ( $T_A = +25^\circ C$ ) Max: $3985\mu A \rightarrow 3165\mu A$ ( $T_A = +105^\circ C$ ) Max: $4830\mu A \rightarrow 3975\mu A$ ( $T_A = +125^\circ C$ )
		Changed the Conditions for $I_{CCTRCL}$ RC Timer mode with $CLKRC = 100kHz$ , SMCR:LPMSS = 0 ( $CLKPLL$ , $CLKMC$ and $CLKSC$ stopped) → RC Timer mode with $CLKRC = 100kHz$ ( $CLKPLL$ , $CLKMC$ and $CLKSC$ stopped)
38		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. → The current for "On Chip Debugger" part is not included.
49	4. Ac Characteristics (10) $I^2C$ Timing	Added parameter, "Noise filter" and an annotation *5 for it Added $t_{SP}$ to the figure
51	5. A/D Converter (2) Accuracy And Setting Of The A/D Converter Sampling Time	Deleted the unit "[Min]" from approximation formula of Sampling time
56	7. Flash Memory Write/Erase Characteristics	Changed the condition ( $V_{CC} = AV_{CC} = 2.7V$ to $5.5V$ , $V_D = 1.8V \pm 0.15V$ , $V_{SS} = AV_{SS} = 0V$ , $T_A = -40^\circ C$ to $+125^\circ C$ ) → ( $V_{CC} = AV_{CC} = 2.7V$ to $5.5V$ , $V_{SS} = AV_{SS} = 0V$ , $T_A = -40^\circ C$ to $+125^\circ C$ )