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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Obsolete
Core Processor	F ² MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I ² C, LINbus, SCI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	52
Program Memory Size	160KB (160K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 21x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f625rbpmc-gse1

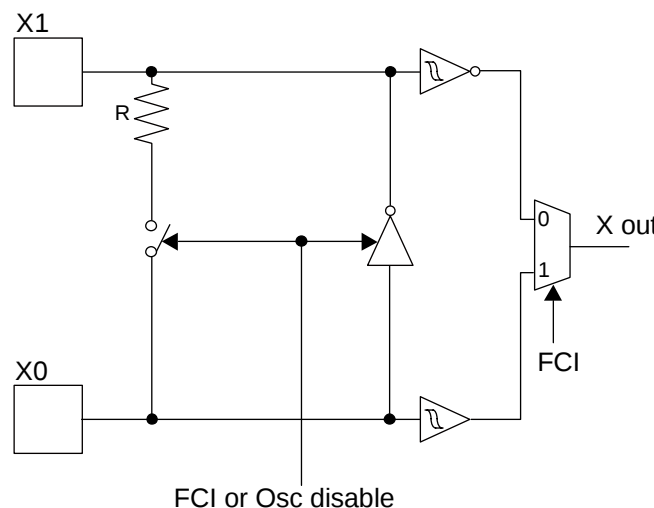
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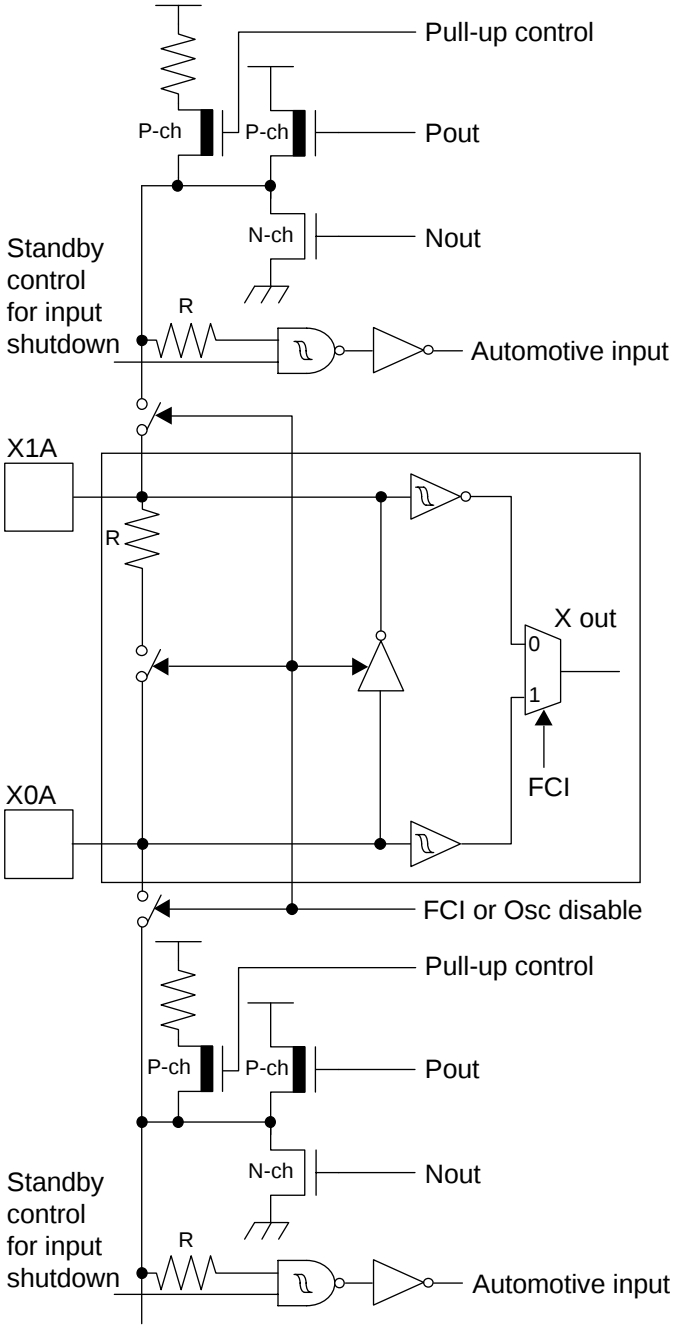
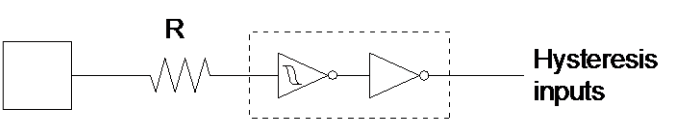
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5. Pin Circuit Type

Pin no.	I/O circuit type*	Pin name
1	Supply	AVss
2	G	AVRH
3	K	P06_2 / AN2
4	K	P06_3 / AN3 / PPG3
5	K	P06_4 / AN4 / PPG4
6	K	P06_5 / AN5
7	K	P06_6 / AN6 / PPG6
8	K	P06_7 / AN7 / PPG7
9	I	P05_0 / AN8 / SIN2 / INT3_R1
10	K	P05_1 / AN9 / SOT2
11	I	P05_2 / AN10 / SCK2
12	K	P05_3 / AN11 / TIN3 / WOT
13	K	P05_4 / AN12 / TOT3 / INT2_R
14	K	P05_5 / AN13 / INT0_R / NMI_R
15	K	P05_6 / AN14 / INT4_R
16	H	P04_2 / IN6 / INT9_R / TTG6 / TTG14
17	H	P04_3 / IN7 / TTG7 / TTG15
18	Supply	Vss
19	B	P04_0 / X0A
20	B	P04_1 / X1A
21	C	MD
22	H	P17_0
23	O	DEBUG I/F
24	M	P00_0 / INT8 / SCK7_R / PPG0_B
25	H	P00_1 / INT9 / SOT7_R / PPG1_B
26	M	P00_2 / INT10 / SIN7_R
27	M	P00_3 / INT11 / SCK8_R / PPG3_B
28	H	P00_4 / INT12 / SOT8_R / PPG12_B
29	M	P00_5 / INT13 / SIN8_R / PPG14_B
30	H	P00_6 / INT14
31	H	P00_7 / INT15
32	H	P01_0 / TIN1 / CKOT1 / OUT0_R

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. $1.0\text{M}\Omega$ • The amplitude: $1.8\text{V}\pm 0.15\text{V}$ to operate by the internal supply voltage

Type	Circuit	Remarks
B	 Pull-up control P-ch P-out N-ch N-out Standby control for input shutdown R Automotive input X1A R X0A X out FCI FCI or Osc disable Pull-up control P-ch P-out N-ch N-out Standby control for input shutdown R Automotive input	Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output ($I_{OL} = 4\text{mA}$, $I_{OH} = -4\text{mA}$), Automotive input with input shutdown function and programmable pull-up resistor)
C	 R Hysteresis inputs	CMOS hysteresis input pin

10. Serial Programming Communication Interface

USART pins for Flash serial programming (MD = 0, DEBUG I/F = 0, Serial Communication mode)

MB96620		
Pin Number	USART Number	Normal Function
9	USART2	SIN2
10		SOT2
11		SCK2
26	USART7	SIN7_R
25		SOT7_R
24		SCK7_R
29	USART8	SIN8_R
28		SOT8_R
27		SCK8_R

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■ Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■ Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■ Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.

2. Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device. Therefore, avoid this type of connection.

3. Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■ Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNP junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■ Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■ Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

13. Handling Devices

Special care is required for the following when handling the device:

- Latch-up prevention
- Unused pins handling
- External clock usage
- Notes on PLL clock mode operation
- Power supply pins (V_{CC}/V_{SS})
- Crystal oscillator and ceramic resonator circuit
- Turn on sequence of power supply to A/D converter and analog inputs
- Pin handling when not using the A/D converter
- Notes on Power-on
- Stabilization of power supply voltage
- Serial communication
- Mode Pin (MD)

13.1 Latch-up prevention

CMOS IC chips may suffer latch-up under the following conditions:

- A voltage higher than V_{CC} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between V_{CC} pins and V_{SS} pins.
- The AV_{CC} power supply is applied before the V_{CC} voltage.

Latch-up may increase the power supply current dramatically, causing thermal damages to the device.

For the same reason, extra care is required to not let the analog power-supply voltage (AV_{CC} , $AVRH$) exceed the digital power-supply voltage.

13.2 Unused pins handling

Unused input pins can be left open when the input is disabled (corresponding bit of Port Input Enable register $PIER = 0$).

Leaving unused input pins open when the input is enabled may result in misbehavior and possible permanent damage of the device. To prevent latch-up, they must therefore be pulled up or pulled down through resistors which should be more than $2k\Omega$.

Unused bidirectional pins can be set either to the output state and be then left open, or to the input state with either input disabled or external pull-up/pull-down resistor as described above.

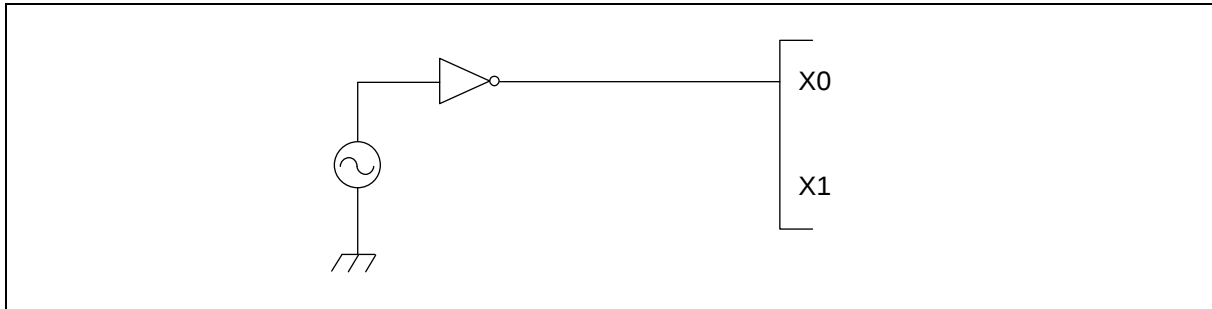
13.3 External clock usage

The permitted frequency range of an external clock depends on the oscillator type and configuration.

See AC Characteristics for detailed modes and frequency limits. Single and opposite phase external clocks must be connected as follows:

13.3.1 Single phase external clock for Main oscillator

When using a single phase external clock for the Main oscillator, X0 pin must be driven and X1 pin left open. And supply 1.8V power to the external clock.

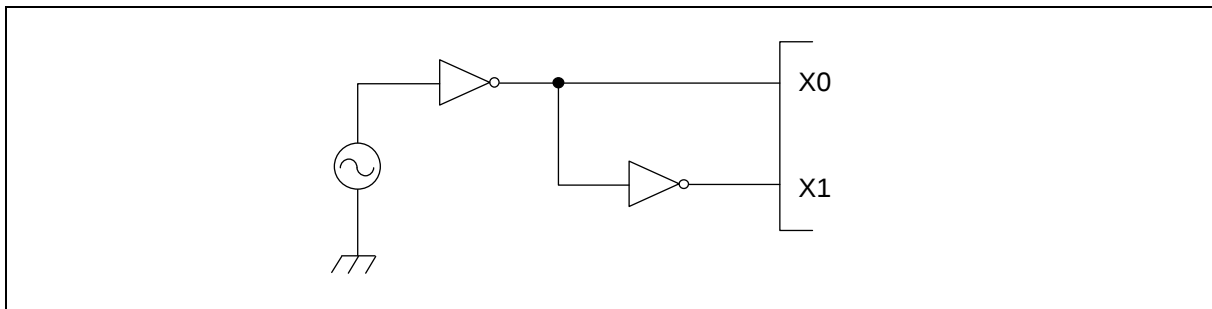


13.3.2 Single phase external clock for Sub oscillator

When using a single phase external clock for the Sub oscillator, "External clock mode" must be selected and X0A/P04_0 pin must be driven. X1A/P04_1 pin can be configured as GPIO.

13.3.3 Opposite phase external clock

When using an opposite phase external clock, X1 (X1A) pins must be supplied with a clock signal which has the opposite phase to the X0 (X0A) pins. Supply level on X0 and X1 pins must be 1.8V.



13.4 Notes on PLL clock mode operation

If the microcontroller is operated with PLL clock mode and no external oscillator is operating or no external clock is supplied, the microcontroller attempts to work with the free oscillating PLL. Performance of this operation, however, cannot be guaranteed.

13.5 Power supply pins (V_{CC}/V_{SS})

It is required that all V_{CC} -level as well as all V_{SS} -level power supply pins are at the same potential. If there is more than one V_{CC} or V_{SS} level, the device may operate incorrectly or be damaged even within the guaranteed operating range.

V_{CC} and V_{SS} pins must be connected to the device from the power supply with lowest possible impedance.

The smoothing capacitor at V_{CC} pin must use the one of a capacity value that is larger than C_s .

Besides this, as a measure against power supply noise, it is required to connect a bypass capacitor of about $0.1\mu F$ between V_{CC} and V_{SS} pins as close as possible to V_{CC} and V_{SS} pins.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
"H" level output voltage	V _{OH4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -4mA	V _{CC} - 0.5	-	V _{CC}	V	
			2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA					
	V _{OH3}	3mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OH} = -3mA	V _{CC} - 0.5	-	V _{CC}	V	
			2.7V ≤ V _{CC} < 4.5V I _{OH} = -1.5mA					
"L" level output voltage	V _{OL4}	4mA type	4.5V ≤ V _{CC} ≤ 5.5V I _{OL} = +4mA	-	-	0.4	V	
			2.7V ≤ V _{CC} < 4.5V I _{OL} = +1.7mA					
	V _{OL3}	3mA type	2.7V ≤ V _{CC} < 5.5V I _{OL} = +3mA	-	-	0.4	V	
	V _{OLD}	DEBUG I/F	V _{CC} = 2.7V I _{OL} = +25mA	0	-	0.25	V	
Input leak current	I _{IL}	Pnn_m	V _{SS} < V _I < V _{CC} AV _{SS} < V _I < AV _{CC} , AVR _H	- 1	-	+ 1	μA	
Pull-up resistance value	R _{PU}	Pnn_m	V _{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C _{IN}	Other than C, V _{CC} , V _{SS} , AV _{CC} , AV _{SS} , AVR _H	-	-	5	15	pF	

14.4.3 Built-in RC Oscillation Characteristics
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C)$

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Clock frequency	f_{RC}	50	100	200	kHz	When using slow frequency of RC oscillator
		1	2	4	MHz	When using fast frequency of RC oscillator
RC clock stabilization time	t_{RCSTAB}	80	160	320	μs	When using slow frequency of RC oscillator (16 RC clock cycles)
		64	128	256	μs	When using fast frequency of RC oscillator (256 RC clock cycles)

14.4.4 Internal Clock Timing
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C)$

Parameter	Symbol	Value		Unit
		Min	Max	
Internal System clock frequency (CLKS1 and CLKS2)	f_{CLKS1}, f_{CLKS2}	-	54	MHz
Internal CPU clock frequency (CLKB), Internal peripheral clock frequency (CLKP1)	f_{CLKB}, f_{CLKP1}	-	32	MHz
Internal peripheral clock frequency (CLKP2)	f_{CLKP2}	-	32	MHz

14.4.8 USART Timing
 $(V_{CC} = AV_{CC} = 2.7V \text{ to } 5.5V, V_{SS} = AV_{SS} = 0V, T_A = -40^{\circ}C \text{ to } +125^{\circ}C, C_L=50pF)$

Parameter	Symbol	Pin name	Conditions	$4.5V \leq V_{CC} < 5.5V$		$2.7V \leq V_{CC} < 4.5V$		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYC}	SCKn	Internal shift clock mode	$4t_{CLKP1}$	-	$4t_{CLKP1}$	-	ns
SCK ↓ → SOT delay time	t_{SLOVI}	SCKn, SOTn		- 20	+ 20	- 30	+ 30	ns
SOT → SCK ↑ delay time	t_{OVSHI}	SCKn, SOTn		$N \times t_{CLKP1} - 20^*$	-	$N \times t_{CLKP1} - 30^*$	-	ns
SIN → SCK ↑ setup time	t_{IVSHI}	SCKn, SINn		$t_{CLKP1} + 45$	-	$t_{CLKP1} + 55$	-	ns
SCK ↑ → SIN hold time	t_{SHIXI}	SCKn, SINn		0	-	0	-	ns
Serial clock "L" pulse width	t_{SLSH}	SCKn	External shift clock mode	$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
Serial clock "H" pulse width	t_{SHSL}	SCKn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK ↓ → SOT delay time	t_{SLOVE}	SCKn, SOTn		-	$2t_{CLKP1} + 45$	-	$2t_{CLKP1} + 55$	ns
SIN → SCK ↑ setup time	t_{IVSHE}	SCKn, SINn		$t_{CLKP1}/2 + 10$	-	$t_{CLKP1}/2 + 10$	-	ns
SCK ↑ → SIN hold time	t_{SHIXE}	SCKn, SINn		$t_{CLKP1} + 10$	-	$t_{CLKP1} + 10$	-	ns
SCK fall time	t_F	SCKn		-	20	-	20	ns
SCK rise time	t_R	SCKn		-	20	-	20	ns

Notes:

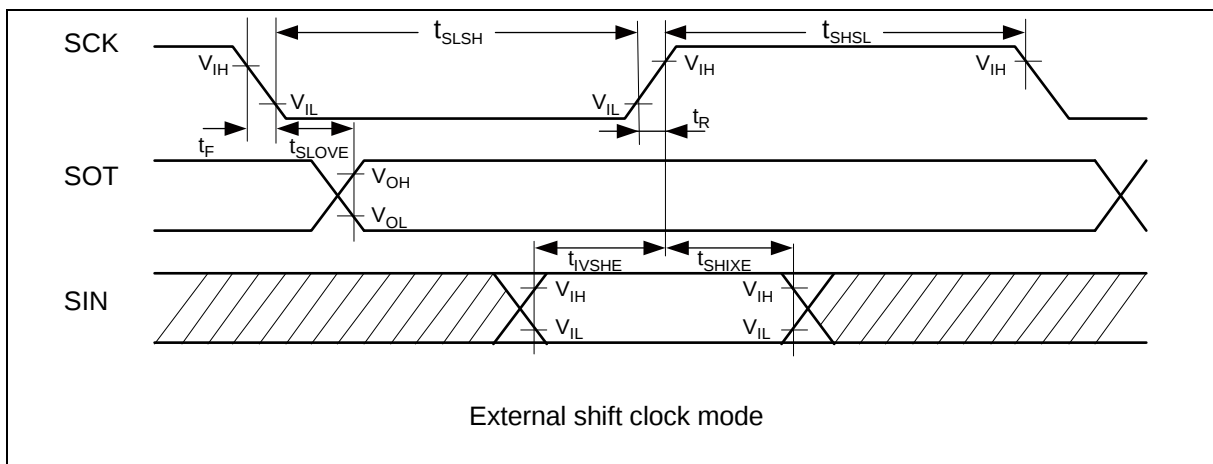
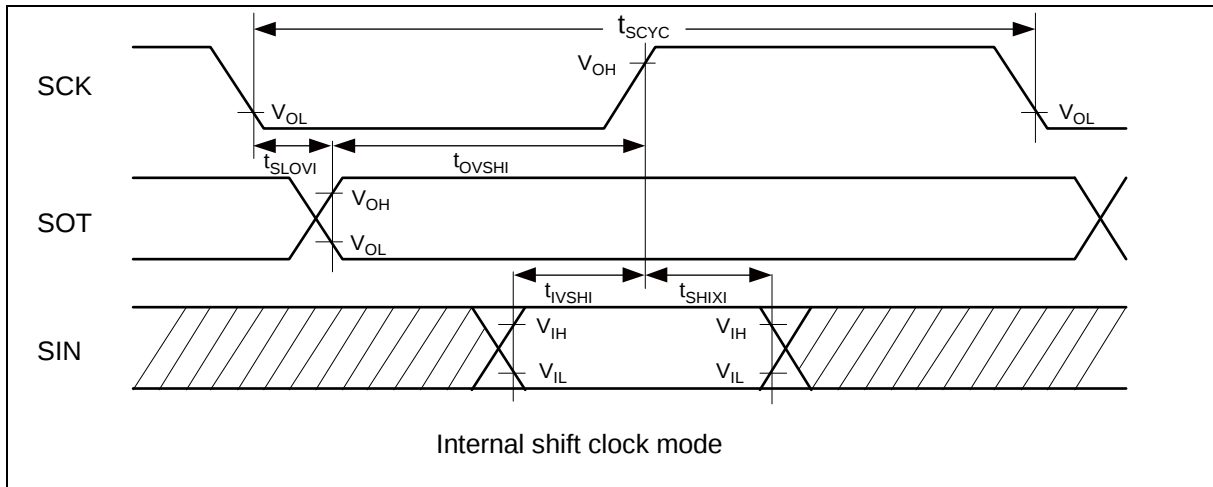
- AC characteristic in CLK synchronized mode.
- C_L is the load capacity value of pins when testing.
- Depending on the used machine clock frequency, the maximum possible baud rate can be limited by some parameters. These parameters are shown in "MB96600 series HARDWARE MANUAL".
- t_{CLKP1} indicates the peripheral clock 1 (CLKP1), Unit: ns
- These characteristics only guarantee the same relocate port number.
For example, the combination of SCKn and SOTn_R is not guaranteed.

*: Parameter N depends on t_{SCYC} and can be calculated as follows:

- If $t_{SCYC} = 2 \times k \times t_{CLKP1}$, then $N = k$, where k is an integer > 2
- If $t_{SCYC} = (2 \times k + 1) \times t_{CLKP1}$, then $N = k + 1$, where k is an integer > 1

Examples:

t_{scyc}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}, 6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}, 8 \times t_{CLKP1}$	4
...	...

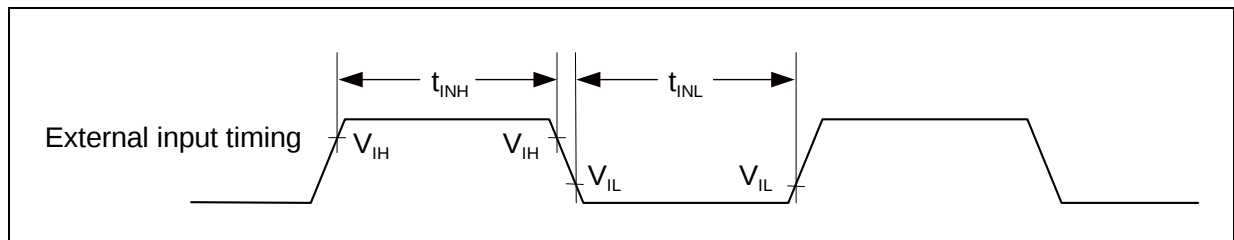


14.4.9 External Input Timing

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Value		Unit	Remarks
			Min	Max		
Input pulse width	t_{INH} , t_{INL}	Pnn_m	$2t_{CLKP1} + 200$ ($t_{CLKP1} = 1/f_{CLKP1}$)*	-	ns	General Purpose I/O
		ADTG_R				A/D Converter trigger input
		TINn				Reload Timer
		TTGn				PPG trigger input
		FRCKn				Free-Running Timer input clock
		INn				Input Capture
		AINn, BINn, ZINn				Quadrature Position/Revolution Counter
		INTn, INTn_R, INTn_R1	200	-	ns	External Interrupt
		NMI_R				Non-Maskable Interrupt

*: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time except stop when in stop mode.



14.5 A/D Converter

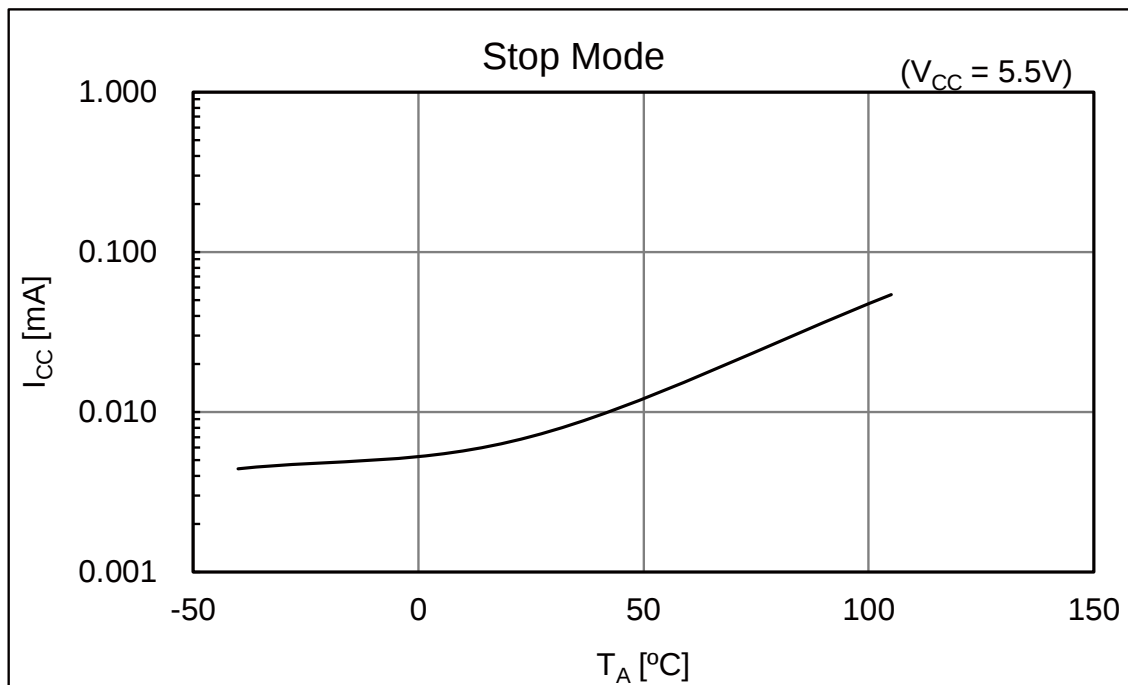
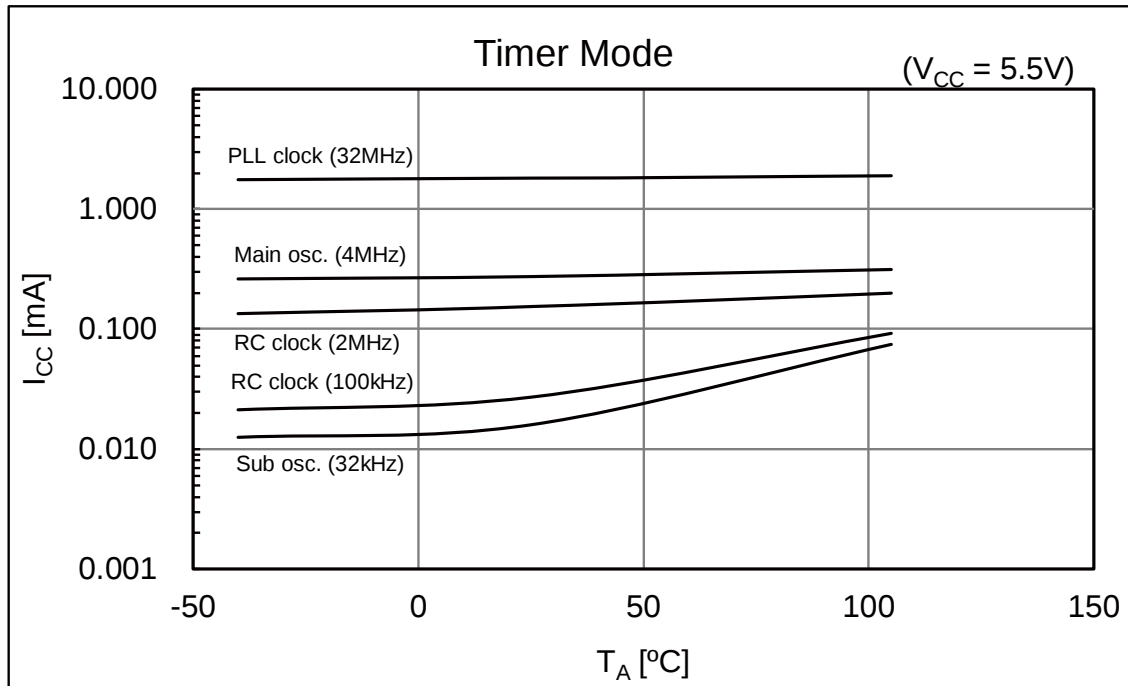
14.5.1 Electrical Characteristics for the A/D Converter

($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution	-	-	-	-	10	bit	
Total error	-	-	- 3.0	-	+ 3.0	LSB	
Nonlinearity error	-	-	- 2.5	-	+ 2.5	LSB	
Differential Nonlinearity error	-	-	- 1.9	-	+ 1.9	LSB	
Zero transition voltage	V_{OT}	ANn	Typ - 20	$AV_{SS} + 0.5LSB$	Typ + 20	mV	
Full scale transition voltage	V_{FST}	ANn	Typ - 20	$AVRH - 1.5LSB$	Typ + 20	mV	
Compare time*	-	-	1.0	-	5.0	μs	$4.5V \leq AV_{CC} \leq 5.5V$
			2.2	-	8.0	μs	$2.7V \leq AV_{CC} < 4.5V$
Sampling time*	-	-	0.5	-	-	μs	$4.5V \leq AV_{CC} \leq 5.5V$
			1.2	-	-	μs	$2.7V \leq AV_{CC} < 4.5V$
Power supply current	I_A	AV_{CC}	-	2.0	3.1	mA	A/D Converter active
	I_{AH}		-	-	3.3	μA	A/D Converter not operated
Reference power supply current (between AVRH and AV_{SS})	I_R	AVRH	-	520	810	μA	A/D Converter active
	I_{RH}		-	-	1.0	μA	A/D Converter not operated
Analog input capacity	C_{VIN}	AN8, 9, 12, 13	-	-	15.5	pF	Normal outputs
		AN16 to 23	-	-	17.4	pF	High current outputs
Analog impedance	R_{VIN}	ANn	-	-	1450	Ω	$4.5V \leq AV_{CC} \leq 5.5V$
			-	-	2700	Ω	$2.7V \leq AV_{CC} < 4.5V$
Analog port input current (during conversion)	I_{AIN}	AN8, 9, 12, 13	- 1.0	-	+ 1.0	μA	$AV_{SS} < V_{AIN} < AV_{CC}, AVRH$
		AN16 to 23	- 3.0	-	+ 3.0	μA	
Analog input voltage	V_{AIN}	ANn	AV_{SS}	-	AVRH	V	
Reference voltage range	-	AVRH	$AV_{CC} - 0.1$	-	AV_{CC}	V	
Variation between channels	-	ANn	-	-	4.0	LSB	

*: Time for each channel.

■ MB96F625



16. Ordering Information

MCU with CAN controller

Part number	Flash memory	Package*
MB96F622RBPMC-GSE1	Flash A (64.5KB)	64-pin plastic LQFP (FPT-64P-M23)
MB96F622RBPMC-GSE2		
MB96F622RBPMC-GTE1		64-pin plastic LQFP (FPT-64P-M24)
MB96F622RBPMC1-GSE1		
MB96F622RBPMC1-GSE2		
MB96F622RBPMC1-GTE1		
MB96F623RBPMC-GSE1	Flash A (96.5KB)	64-pin plastic LQFP (FPT-64P-M23)
MB96F623RBPMC-GSE2		
MB96F623RBPMC-GTE1		64-pin plastic LQFP (FPT-64P-M24)
MB96F623RBPMC1-GSE1		
MB96F623RBPMC1-GSE2		
MB96F623RBPMC1-GTE1		
MB96F625RBPMC-GSE1	Flash A (160.5KB)	64-pin plastic LQFP (FPT-64P-M23)
MB96F625RBPMC-GSE2		
MB96F625RBPMC-GTE1		64-pin plastic LQFP (FPT-64P-M24)
MB96F625RBPMC1-GSE1		
MB96F625RBPMC1-GSE2		
MB96F625RBPMC1-GTE1		

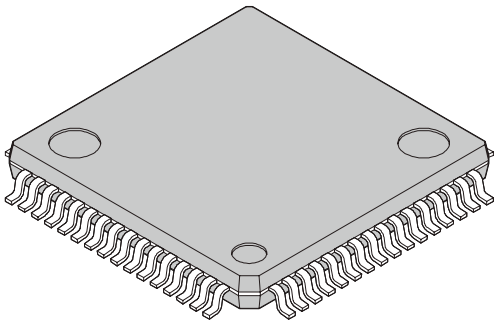
*: For details about package, see "PACKAGE DIMENSION".

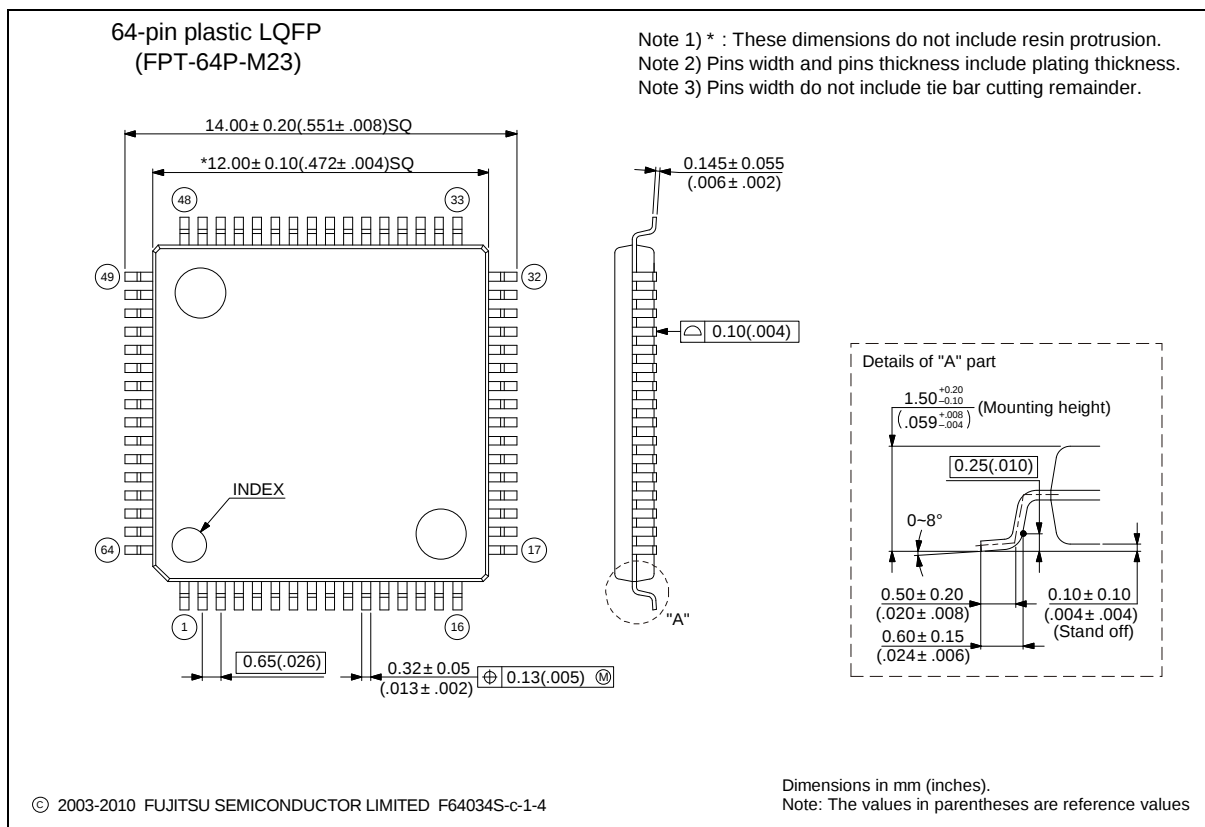
MCU without CAN controller

Part number	Flash memory	Package*
MB96F622ABPMC-GSE1	Flash A (64.5KB)	64-pin plastic LQFP (FPT-64P-M23)
MB96F622ABPMC-GSE2		
MB96F622ABPMC-GTE1		64-pin plastic LQFP (FPT-64P-M24)
MB96F622ABPMC1-GSE1		
MB96F622ABPMC1-GSE2		
MB96F622ABPMC1-GTE1		
MB96F623ABPMC-GSE1	Flash A (96.5KB)	64-pin plastic LQFP (FPT-64P-M23)
MB96F623ABPMC-GSE2		
MB96F623ABPMC-GTE1		64-pin plastic LQFP (FPT-64P-M24)
MB96F623ABPMC1-GSE1		
MB96F623ABPMC1-GSE2		
MB96F623ABPMC1-GTE1		
MB96F625ABPMC-GSE1	Flash A (160.5KB)	64-pin plastic LQFP (FPT-64P-M23)
MB96F625ABPMC-GSE2		
MB96F625ABPMC-GTE1		64-pin plastic LQFP (FPT-64P-M24)
MB96F625ABPMC1-GSE1		
MB96F625ABPMC1-GSE2		
MB96F625ABPMC1-GTE1		

*: For details about package, see "PACKAGE DIMENSION".

17. Package Dimension

64-pin plastic LQFP  (FPT-64P-M23)	Lead pitch	0.65 mm
	Package width × package length	12.0 × 12.0 mm
	Lead shape	Gullwing
	Sealing method	Plastic mold
	Mounting height	1.70 mm MAX
	Weight	0.47 g
	Code (Reference)	P-LQFP64-12 × 12-0.65



18. Major Changes

Spanion Publication Number: MB96620_DS704-00008

Page	Section	Change Results
Revision 2.0		
4	Features	Changed the description of "External Interrupts" Interrupt mask and pending bit per channel → Interrupt mask bit per channel
25 to 28	Handling Precautions	Added a section
36	Electrical Characteristics 3. Dc Characteristics (1) Current Rating	Changed the Conditions for I_{CCSRCH} $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 2MHz$, → $CLKS1/2 = CLKP1/2 = CLKRC = 2MHz$,
		Changed the Conditions for I_{CCSRCL} $CLKS1/2 = CLKB = CLKP1/2 = CLKRC = 100kHz$ → $CLKS1/2 = CLKP1/2 = CLKRC = 100kHz$
37		Changed the Conditions for I_{CCTPLL} PLL Timer mode with $CLKP1 = 32MHz$ → PLL Timer mode with $CLKPLL = 32MHz$
		Changed the Value of "Power supply current in Timer modes" I_{CCTPLL} Typ: $2480\mu A \rightarrow 1800\mu A$ ($T_A = +25^\circ C$) Max: $2710\mu A \rightarrow 2245\mu A$ ($T_A = +25^\circ C$) Max: $3985\mu A \rightarrow 3165\mu A$ ($T_A = +105^\circ C$) Max: $4830\mu A \rightarrow 3975\mu A$ ($T_A = +125^\circ C$)
38		Changed the Conditions for I_{CCTRCL} RC Timer mode with $CLKRC = 100kHz$, SMCR:LPMSS = 0 ($CLKPLL$, $CLKMC$ and $CLKSC$ stopped) → RC Timer mode with $CLKRC = 100kHz$ ($CLKPLL$, $CLKMC$ and $CLKSC$ stopped)
		Changed the annotation *2 Power supply for "On Chip Debugger" part is not included. Power supply current in Run mode does not include Flash Write / Erase current. → The current for "On Chip Debugger" part is not included.
49	4. Ac Characteristics (10) I^2C Timing	Added parameter, "Noise filter" and an annotation *5 for it Added t_{SP} to the figure
51	5. A/D Converter (2) Accuracy And Setting Of The A/D Converter Sampling Time	Deleted the unit "[Min]" from approximation formula of Sampling time
56	7. Flash Memory Write/Erase Characteristics	Changed the condition ($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_D = 1.8V \pm 0.15V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$) → ($V_{CC} = AV_{CC} = 2.7V$ to $5.5V$, $V_{SS} = AV_{SS} = 0V$, $T_A = -40^\circ C$ to $+125^\circ C$)

Document History

Document Title: MB96620 Series F²MC-16FX 16-Bit Microcontroller

Document Number: 002-04712

Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	-	KSUN	01/31/2014	Migrated to Cypress and assigned document number 002-04712. No change to document contents or format.
*A	5137624	KSUN	02/17/2016	Updated to Cypress format.

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