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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Not For New Designs |
| Core Processor | Coldfire V2 |
| Core Size | 32-Bit Single-Core |
| Speed | 66MHz |
| Connectivity | CANbus, I²C, SPI, UART/USART |
| Peripherals | DMA, LVD, POR, PWM, WDT |
| Number of I/O | 55 |
| Program Memory Size | 256KB (256K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | - |
| RAM Size | 32K x 8 |
| Voltage - Supply (Vcc/Vdd) | 3V ~ 3.6V |
| Data Converters | A/D 8x12b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 100-LQFP |
| Supplier Device Package | 100-LQFP (14x14) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5213caf66 |

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  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines for two UARTs
  - Transmit and receive FIFO buffers
- $I^2C$ module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard $I^2C$ bus
  - Master and slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued serial peripheral interface (QSPI)
  - Full-duplex, three-wire synchronous transfers
  - Up to four chip selects available
  - Master mode operation only
  - Programmable bit rates up to half the CPU clock frequency
  - Up to 16 pre-programmed transfers
- Fast analog-to-digital converter (ADC)
  - Eight analog input channels
  - 12-bit resolution
  - Minimum 1.125 µs conversion time
  - Simultaneous sampling of two channels for motor control applications
  - Single-scan or continuous operation
  - Optional interrupts on conversion complete, zero crossing (sign change), or under/over low/high limit
  - Unused analog channels can be used as digital I/O
- Four 32-bit timers with DMA support
  - 12.5 ns resolution at 80 MHz
  - Programmable sources for clock input, including an external clock option
  - Programmable prescaler
  - Input capture capability with programmable trigger edge on input pin
  - Output compare with programmable mode for the output pin
  - Free run and restart modes
  - Maskable interrupts on input capture or output compare
  - DMA trigger capability on input capture or output compare
- Four-channel general purpose timer
  - 16-bit architecture
  - Programmable prescaler
  - Output pulse-widths variable from microseconds to seconds
  - Single 16-bit input pulse accumulator
  - Toggle-on-overflow feature for pulse-width modulator (PWM) generation
  - One dual-mode pulse accumulation channel
- Pulse-width modulation timer
  - Operates as eight channels with 8-bit resolution or four channels with 16-bit resolution
  - Programmable period and duty cycle
  - Programmable enable/disable for each channel
  - Software selectable polarity for each channel
  - Period and duty cycle are double buffered. Change takes effect when the end of the current period is reached (PWM counter reaches zero) or when the channel is disabled.

  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low-power mode support
- Clock generation features
  - One to 48 MHz crystal, 8 MHz on-chip relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator
  - Two to 10 MHz reference frequency for normal PLL mode with a pre-divider programmable from 1 to 8
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - $2^n$ ($n \leq 0 \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)

Figure 2 shows the pinout configuration for the 100 LQFP.

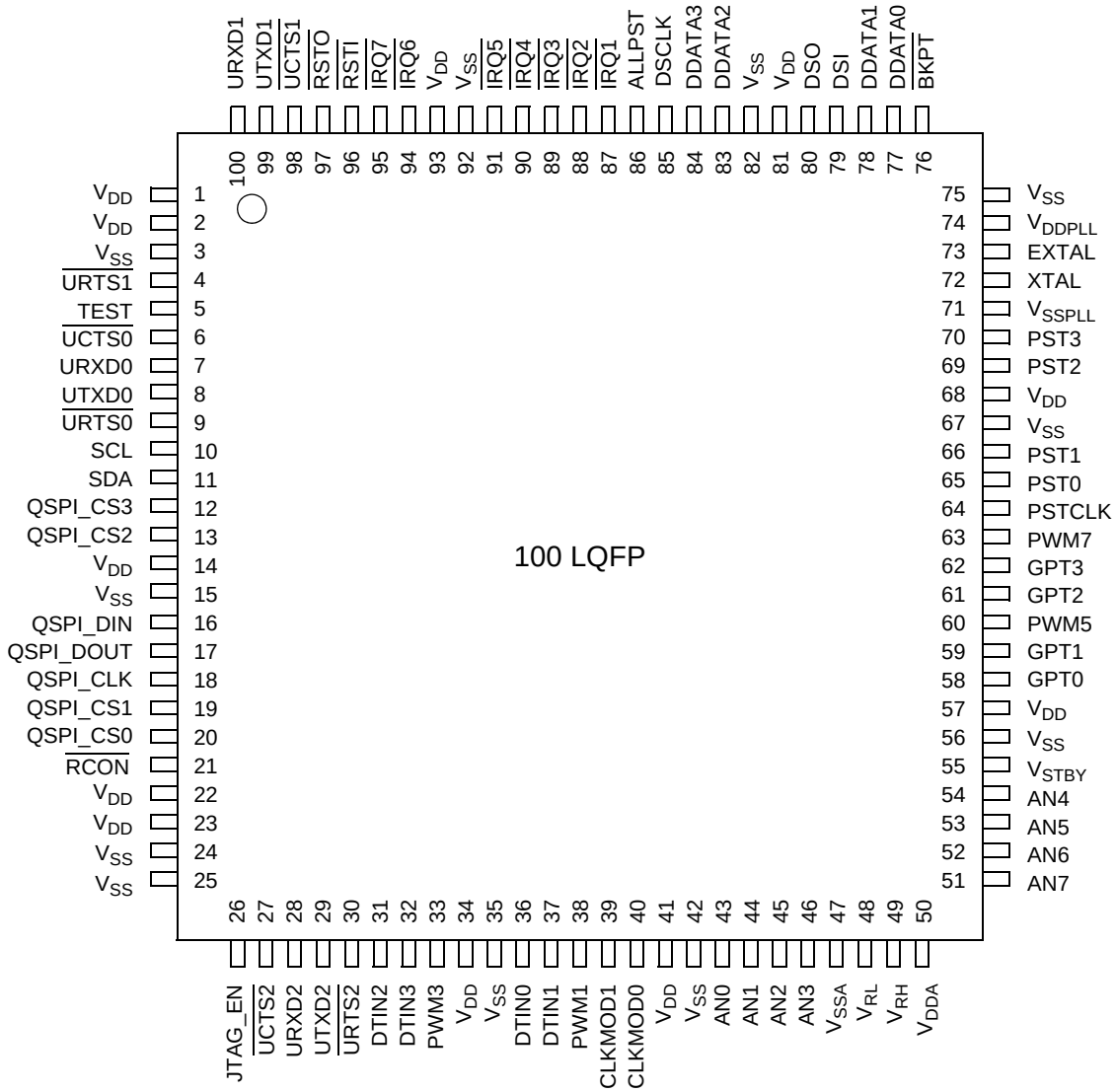


**Figure 2. 100 LQFP Pin Assignments**

Figure 3 shows the pinout configuration for the 81 MAPBGA.

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 |
|---|---|---|---|---|---|---|---|---|---|
| A | $V_{SS}$ | UTXD1 | $\overline{RSTI}$ | $\overline{IRQ5}$ | $\overline{IRQ3}$ | ALLPST | TDO | TMS | $V_{SS}$ |
| B | $\overline{URTS1}$ | URXD1 | $\overline{RSTO}$ | $\overline{IRQ6}$ | $\overline{IRQ2}$ | $\overline{TRST}$ | TDI | $V_{DD}$PLL | EXTAL |
| C | $\overline{UCTS0}$ | TEST | $\overline{UCTS1}$ | $\overline{IRQ7}$ | $\overline{IRQ4}$ | $\overline{IRQ1}$ | TCLK | $V_{SS}$PLL | XTAL |
| D | URXD0 | UTXD0 | $\overline{URTS0}$ | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | PWM7 | GPT3 | GPT2 |
| E | SCL | SDA | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | $V_{DD}$ | PWM5 | GPT1 |
| F | QSPI_CS3 | QSPI_CS2 | QSPI_DIN | $V_{SS}$ | $V_{DD}$ | $V_{SS}$ | GPT0 | $V_{STBY}$ | AN4 |
| G | QSPI_DOUT | QSPI_CLK | $\overline{RCON}$ | DTIN1 | CLKMOD0 | AN2 | AN3 | AN5 | AN6 |
| H | QSPI_CS0 | QSPI_CS1 | DTIN3 | DTIN0 | CLKMOD1 | AN1 | $V_{SSA}$ | $V_{DDA}$ | AN7 |
| J | $V_{SS}$ | JTAG_EN | DTIN2 | PWM3 | PWM1 | AN0 | $V_{RL}$ | $V_{RH}$ | $V_{SSA}$ |

**Figure 3. 81 MAPBGA Pin Assignments**

Figure 4 shows the pinout configuration for the 64 LQFP and 64 QFN.

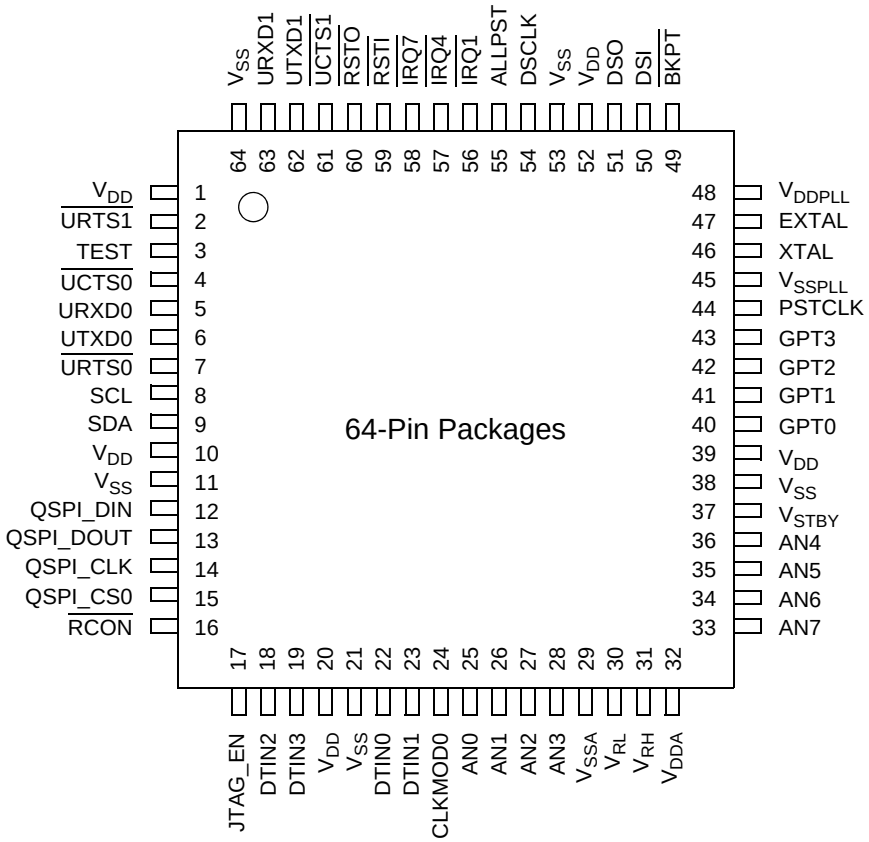


**Figure 4. 64 LQFP and 64 QFN Pin Assignments**

Table 3 shows the pin functions by primary and alternate purpose, and illustrates which packages contain each pin.

## 1.2 Reset Signals

Table 4 describes signals used to reset the chip or as a reset indication.

**Table 4. Reset Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Reset In | $\overline{\text{RSTI}}$ | Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals. | I |
| Reset Out | $\overline{\text{RSTO}}$ | Driven low for 1024 CPU clocks after the reset source has deasserted. | O |

## 1.3 PLL and Clock Signals

Table 5 describes signals used to support the on-chip clock generation circuitry.

**Table 5. PLL and Clock Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| External Clock In | EXTAL | Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used. | I |
| Crystal | XTAL | Crystal oscillator output except when CLKMOD1=1, then sampled as part of the clock mode selection mechanism. | O |
| Clock Out | CLKOUT | This output signal reflects the internal system clock. | O |

## 1.4 Mode Selection

Table 6 describes signals used in mode selection; Table 7 describes the particular clocking modes.

**Table 6. Mode Selection Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Clock Mode Selection | CLKMOD[1:0] | Selects the clock boot mode. | I |
| Reset Configuration | RCON | The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device. | |
| Test | TEST | Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions. | I |

**Table 7. Clocking Modes**

| CLKMOD[1:0] | XTAL | Configure the clock mode. |
|---|---|---|
| 00 | 0 | PLL disabled, clock driven by external oscillator |
| 00 | 1 | PLL disabled, clock driven by on-chip oscillator |
| 01 | N/A | PLL disabled, clock driven by crystal |
| 10 | 0 | PLL in normal mode, clock driven by external oscillator |
| 10 | 1 | PLL in normal mode, clock driven by on-chip oscillator |
| 11 | N/A | PLL in normal mode, clock driven by crystal |

## 1.8 UART Module Signals

Table 11 describes the UART module signals.

**Table 11. UART Module Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Transmit Serial Data Output | UTXD*n* | Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source. | O |
| Receive Serial Data Input | URXD*n* | Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts the clock. | I |
| Clear-to-Send | $\overline{\text{UCTS}}n$ | Indication to the UART modules that they can begin data transmission. | I |
| Request-to-Send | $\overline{\text{URTS}}n$ | Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level. | O |

## 1.9 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

**Table 12. DMA Timer Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| DMA Timer Input | DTIN | Event input to the DMA timer modules. | I |
| DMA Timer Output | DTOUT | Programmable output from the DMA timer modules. | O |

## 1.10 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

**Table 13. ADC Signals**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Analog Inputs | AN[7:0] | Inputs to the analog-to-digital converter. | I |
| Analog Reference | $V_{RH}$ | Reference voltage high and low inputs. | I |
| | $V_{RL}$ | | I |
| Analog Supply | $V_{DDA}$ | Isolate the ADC circuitry from power supply noise. | — |
| | $V_{SSA}$ | | — |
| ADC Sync Inputs | SYNCA / SYNCB | These signals can initiate an analog-to-digital conversion process. | I |

**Table 16. Debug Support Signals (continued)**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| Development Serial Input | DSI | Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1). | I |
| Development Serial Output | DSO | Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high. | O |
| Debug Data | DDATA[3:0] | Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0]. | O |
| Processor Status Clock | PSTCLK | Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values.<br>If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs.<br>PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing. | O |
| Processor Status Outputs | PST[3:0] | Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0]. | O |
| All Processor Status Outputs | ALLPST | Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST. | O |

## 1.14 EzPort Signal Descriptions

Table contains a list of EzPort external signals.

**Table 17. EzPort Signal Descriptions**

| Signal Name | Abbreviation | Function | I/O |
|---|---|---|---|
| EzPort Clock | EZPCK | Shift clock for EzPort transfers. | I |
| EzPort Chip Select | EZPCS | Chip select for signalling the start and end of serial transfers. | I |
| EzPort Serial Data In | EZPD | EZPD is sampled on the rising edge of EZPCK. | I |
| EzPort Serial Data Out | EZPQ | EZPQ transitions on the falling edge of EZPCK. | O |

**Table 22. Thermal Characteristics (continued)**

| | Characteristic | | Symbol | Value | Unit |
|---|---|---|---|---|---|
| 81 MAPBGA | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 61[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 35[2,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 50[2,3] | °C/W |
| | Junction to ambient, (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 31[2,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 20[4] | °C/W |
| | Junction to case | — | $\theta_{JC}$ | 12[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |
| 64 LQFP | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 62[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 43[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 50[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 36[1,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 26[4] | °C/W |
| | Junction to case | — | $\theta_{JC}$ | 9[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 2[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |
| 64 QFN | Junction to ambient, natural convection | Single layer board (1s) | $\theta_{JA}$ | 68[1,2] | °C/W |
| | Junction to ambient, natural convection | Four layer board (2s2p) | $\theta_{JA}$ | 24[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Single layer board (1s) | $\theta_{JMA}$ | 55[1,3] | °C/W |
| | Junction to ambient (@200 ft/min) | Four layer board (2s2p) | $\theta_{JMA}$ | 19[1,3] | °C/W |
| | Junction to board | — | $\theta_{JB}$ | 8[4] | °C/W |
| | Junction to case (bottom) | — | $\theta_{JC}$ | 0.6[5] | °C/W |
| | Junction to top of package | Natural convection | $\Psi_{jt}$ | 3[6] | °C/W |
| | Maximum operating junction temperature | — | $T_j$ | 105 | °C |

1 $\theta_{JA}$ and $\Psi_{jt}$ parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of $\theta_{JA}$ and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the $\Psi_{jt}$ parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

3 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

## 2.5 ESD Protection

**Table 25. ESD Protection Characteristics[1, 2]**

| Characteristics | Symbol | Value | Units |
|---|---|---|---|
| ESD target for Human Body Model | HBM | 2000 | V |
| ESD target for Machine Model | MM | 200 | V |
| HBM circuit description | $R_{series}$ | 1500 | Ω |
| | C | 100 | pF |
| MM circuit description | $R_{series}$ | 0 | Ω |
| | C | 200 | pF |
| Number of pulses per pin (HBM)<br>• Positive pulses<br>• Negative pulses | <br>—<br>— | <br>1<br>1 | — |
| Number of pulses per pin (MM)<br>• Positive pulses<br>• Negative pulses | <br>—<br>— | <br>3<br>3 | — |
| Interval of pulses | — | 1 | sec |

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

## 2.6 DC Electrical Specifications

**Table 26. DC Electrical Specifications [1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage | $V_{DD}$ | 3.0 | 3.6 | V |
| Standby voltage | $V_{STBY}$ | 3.0 | 3.6 | V |
| Input high voltage | $V_{IH}$ | $0.7 \times V_{DD}$ | 4.0 | V |
| Input low voltage | $V_{IL}$ | $V_{SS} - 0.3$ | $0.35 \times V_{DD}$ | V |
| Input hysteresis | $V_{HYS}$ | $0.06 \times V_{DD}$ | — | mV |
| Low-voltage detect trip voltage ($V_{DD}$ falling) | $V_{LVD}$ | 2.15 | 2.3 | V |
| Low-voltage detect hysteresis ($V_{DD}$ rising) | $V_{LVDHYS}$ | 60 | 120 | mV |
| Input leakage current<br>$V_{in} = V_{DD}$ or $V_{SS}$, digital pins | $I_{in}$ | –1.0 | 1.0 | μA |
| Output high voltage (all input/output and all output pins)<br>$I_{OH} = -2.0$ mA | $V_{OH}$ | $V_{DD} - 0.5$ | — | V |
| Output low voltage (all input/output and all output pins)<br>$I_{OL} = 2.0$mA | $V_{OL}$ | — | 0.5 | V |

**Table 26. DC Electrical Specifications (continued)[1]**

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Output high voltage (high drive)<br>$I_{OH}$ = -5 mA | $V_{OH}$ | $V_{DD}$ – 0.5 | — | V |
| Output low voltage (high drive)<br>$I_{OL}$ = 5 mA | $V_{OL}$ | — | 0.5 | V |
| Output high voltage (low drive)<br>$I_{OH}$ = -2 mA | $V_{OH}$ | $V_{DD}$ - 0.5 | — | V |
| Output low voltage (low drive)<br>$I_{OL}$ = 2 mA | $V_{OL}$ | — | 0.5 | V |
| Weak internal pull Up device current, tested at $V_{IL}$ Max.[2] | $I_{APU}$ | –10 | –130 | µA |
| Input Capacitance [3]<br>• All input-only pins<br>• All input/output (three-state) pins | $C_{in}$ | <br>—<br>— | <br>7<br>7 | pF |

1 Refer to Table 27 for additional PLL specifications.

2 Refer to Table 3 for pins having internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

## 2.7 Clock Source Electrical Specifications

**Table 27. PLL Electrical Specifications**

($V_{DD}$ and $V_{DDPLL}$ = 2.7 to 3.6 V, $V_{SS}$ = $V_{SSPLL}$ = 0 V)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| PLL reference frequency range<br>• Crystal reference<br>• External reference | <br>$f_{ref\_crystal}$<br>$f_{ref\_ext}$ | <br>2<br>2 | <br>10.0<br>10.0 | MHz |
| System frequency [1]<br>• External clock mode<br>• On-chip PLL frequency | $f_{sys}$ | <br>0<br>$f_{ref}$ / 32 | <br>66.67 or 80[2]<br>66.67 or 80[2] | MHz |
| Loss of reference frequency [3, 5] | $f_{LOR}$ | 100 | 1000 | kHz |
| Self clocked mode frequency [4] | $f_{SCM}$ | 1 | 5 | MHz |
| Crystal start-up time [5, 6] | $t_{cst}$ | — | 10 | ms |
| EXTAL input high voltage<br>• External reference | $V_{IHEXT}$ | <br>2.0 | <br>$V_{DD}$ | V |
| EXTAL input low voltage<br>• External reference | $V_{ILEXT}$ | <br>$V_{SS}$ | <br>0.8 | V |
| PLL lock time[4,7] | $t_{lpll}$ | — | 500 | µs |
| Duty cycle of reference [4] | $t_{dc}$ | 40 | 60 | % $f_{ref}$ |

**Table 27. PLL Electrical Specifications (continued)**

($V_{DD}$ and $V_{DDPLL}$ = 2.7 to 3.6 V, $V_{SS}$ = $V_{SSPLL}$ = 0 V)

| Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Frequency un-LOCK range | $f_{UL}$ | –1.5 | 1.5 | % $f_{ref}$ |
| Frequency LOCK range | $f_{LCK}$ | –0.75 | 0.75 | % $f_{ref}$ |
| CLKOUT period jitter [4, 5, 8, 9], measured at $f_{SYS}$ Max<br>• Peak-to-peak (clock edge to clock edge)<br>• Long term (averaged over 2 ms interval) | $C_{jitter}$ | <br>—<br>— | <br>10<br>.01 | % $f_{sys}$ |
| On-chip oscillator frequency | $f_{oco}$ | 7.84 | 8.16 | MHz |

1 All internal registers retain data at 0 Hz.

2 Depending on packaging; see Table 2.

3 Loss of Reference Frequency is the reference frequency detected internally, which transitions the PLL into self clocked mode.

4 Self clocked mode frequency is the frequency at which the PLL operates when the reference frequency falls below $f_{LOR}$ with default MFD/RFD settings.

5 This parameter is characterized before qualification rather than 100% tested.

6 Proper PC board layout procedures must be followed to achieve specifications.

7 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).

8 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via $V_{DDPLL}$ and $V_{SSPLL}$ and variation in crystal oscillator frequency increase the $C_{jitter}$ percentage for a given interval.

9 Based on slow system clock of 40 MHz measured at $f_{sys}$ max.

## 2.8 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, timer, UART, and Interrupt interfaces. When in GPIO mode, the timing specification for these pins is given in Table 28 and Figure 5.

The GPIO timing is met under the following load test conditions:

- 50 pF / 50 Ω for high drive
- 25 pF / 25 Ω for low drive

**Table 28. GPIO Timing**

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| G1 | CLKOUT High to GPIO Output Valid | $t_{CHPOV}$ | — | 10 | ns |
| G2 | CLKOUT High to GPIO Output Invalid | $t_{CHPOI}$ | 1.5 | — | ns |
| G3 | GPIO Input Valid to CLKOUT High | $t_{PVCH}$ | 9 | — | ns |
| G4 | CLKOUT High to GPIO Input Invalid | $t_{CHPI}$ | 1.5 | — | ns |

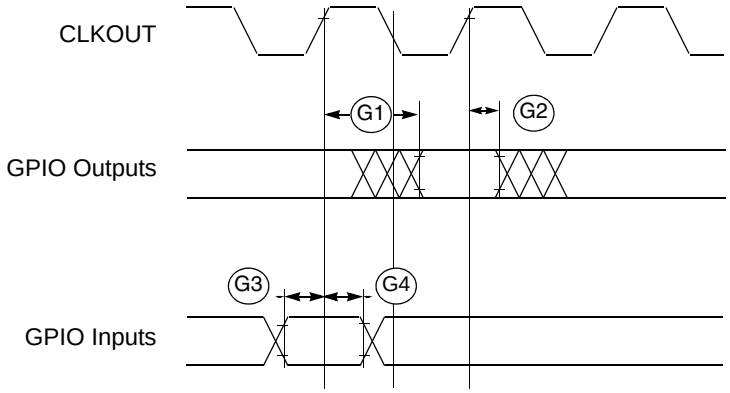


**Figure 5. GPIO Timing**

## 2.9 Reset Timing

**Table 29. Reset and Configuration Override Timing**

($V_{DD}$ = 2.7 to 3.6 V, $V_{SS}$ = 0 V, $T_A$ = $T_L$ to $T_H$)[1]

| NUM | Characteristic | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| R1 | $\overline{\text{RSTI}}$ input valid to CLKOUT High | $t_{RVCH}$ | 9 | — | ns |
| R2 | CLKOUT High to $\overline{\text{RSTI}}$ Input invalid | $t_{CHRI}$ | 1.5 | — | ns |
| R3 | $\overline{\text{RSTI}}$ input valid time [2] | $t_{RIVT}$ | 5 | — | $t_{CYC}$ |
| R4 | CLKOUT High to $\overline{\text{RSTO}}$ Valid | $t_{CHROV}$ | — | 10 | ns |

[1] All AC timing is shown with respect to 50% $V_{DD}$ levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

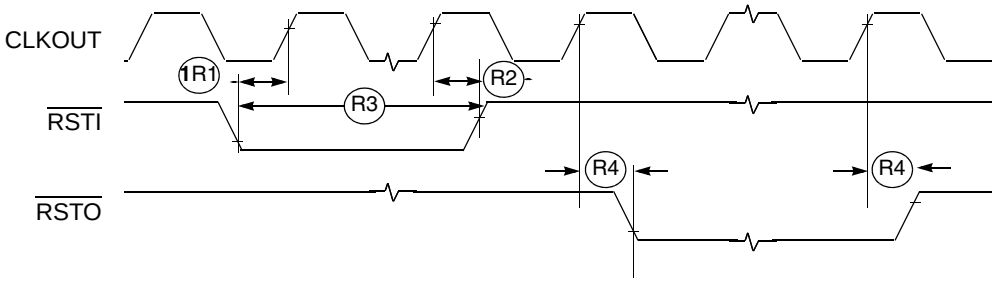


**Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing**

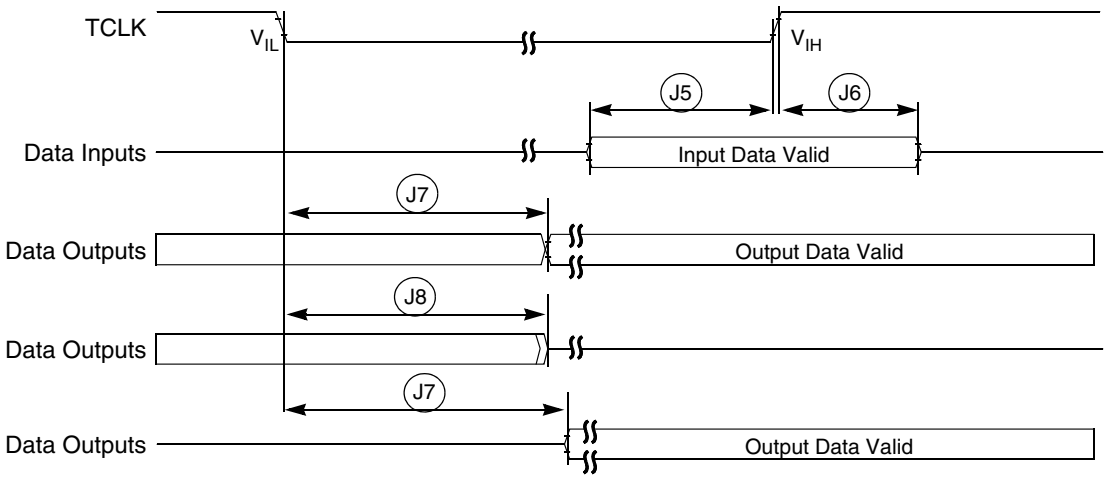


**Figure 11. Boundary Scan (JTAG) Timing**

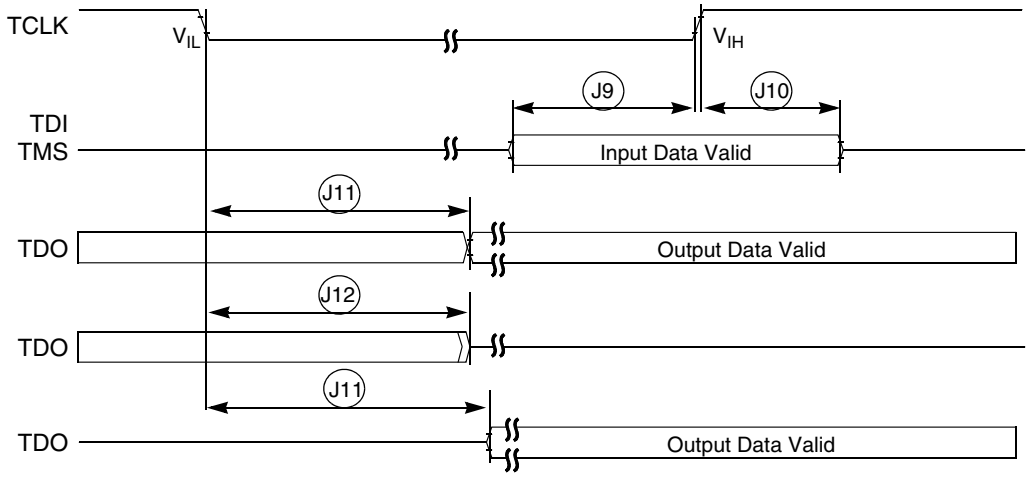


**Figure 12. Test Access Port Timing**

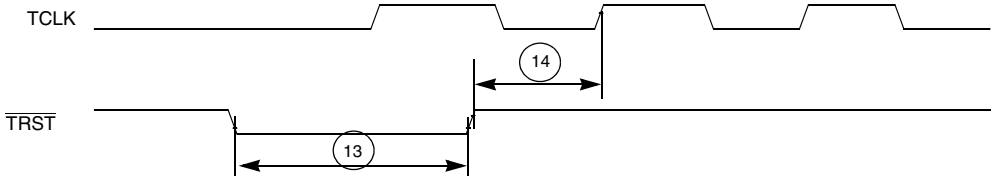


**Figure 13. TRST Timing**

Figure 15 shows BDM serial port AC timing for the values in Table 36.

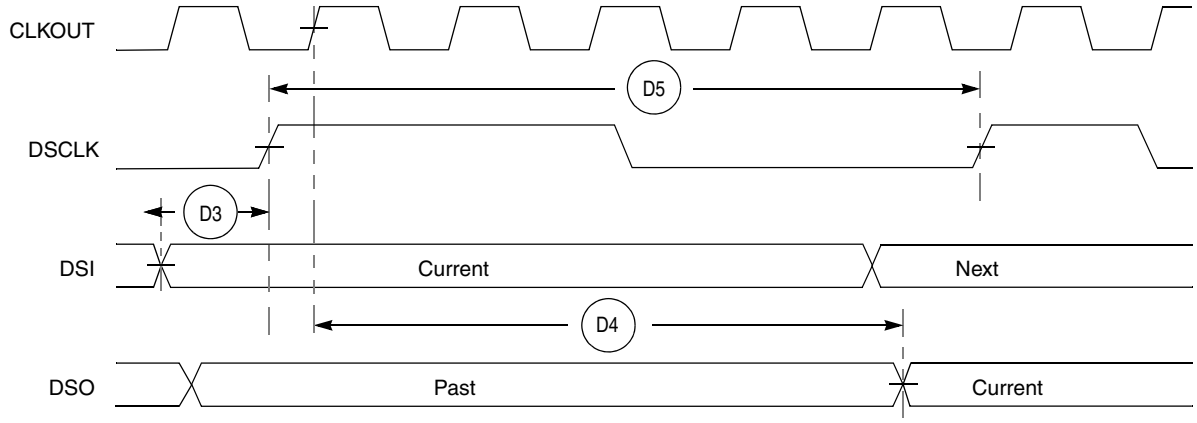


**Figure 15. BDM Serial Port AC Timing**

| | | |
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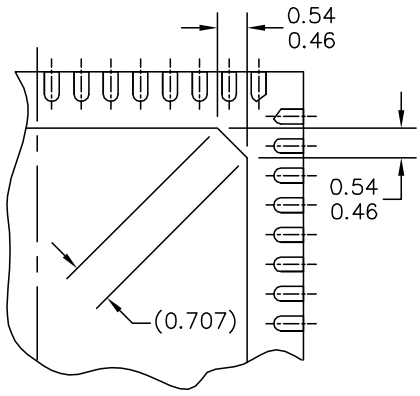
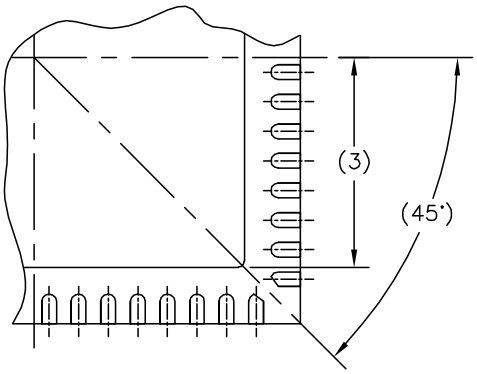
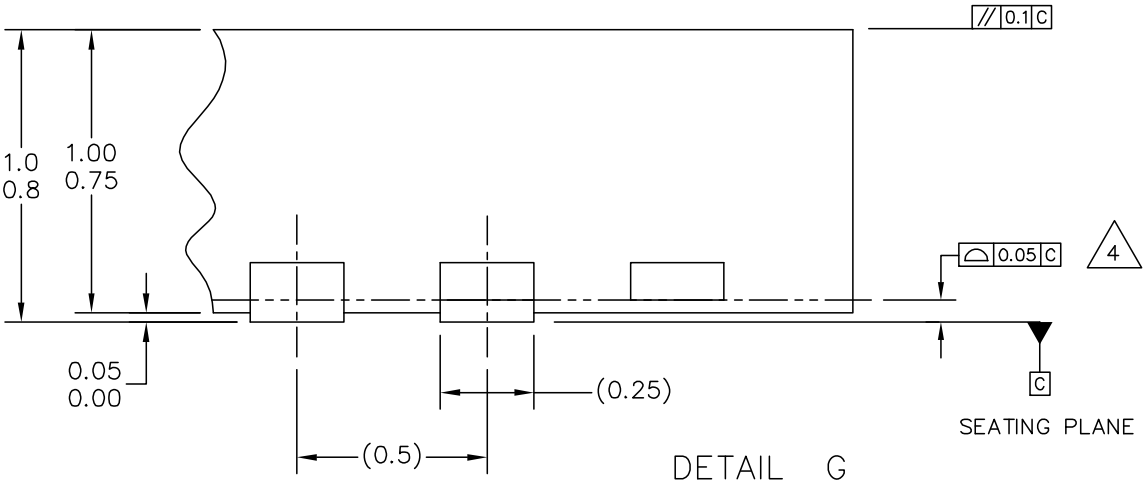



DETAIL M
PREFERRED PIN1 BACKSIDE IDENTIFIER




DETAIL N
PREFERRED CORNER CONFIGURATION




DETAIL G
VIEW ROTATED 90° CW

| | | |
|---|---|---|
| TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1) | CASE NUMBER: 1740-01 | |
| | STANDARD: JEDEC MO-220 VMMD-3 | |
| | PACKAGE CODE: 6200 | SHEET: 2 OF 4 |

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# REVISION HISTORY

DOCUMENT NO: 98ASA10690D
PAGE: 1740
REV: O

| LTR | ORIGINATOR | REVISIONS | DRAFTER | DATE |
|---|---|---|---|---|
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| | | |
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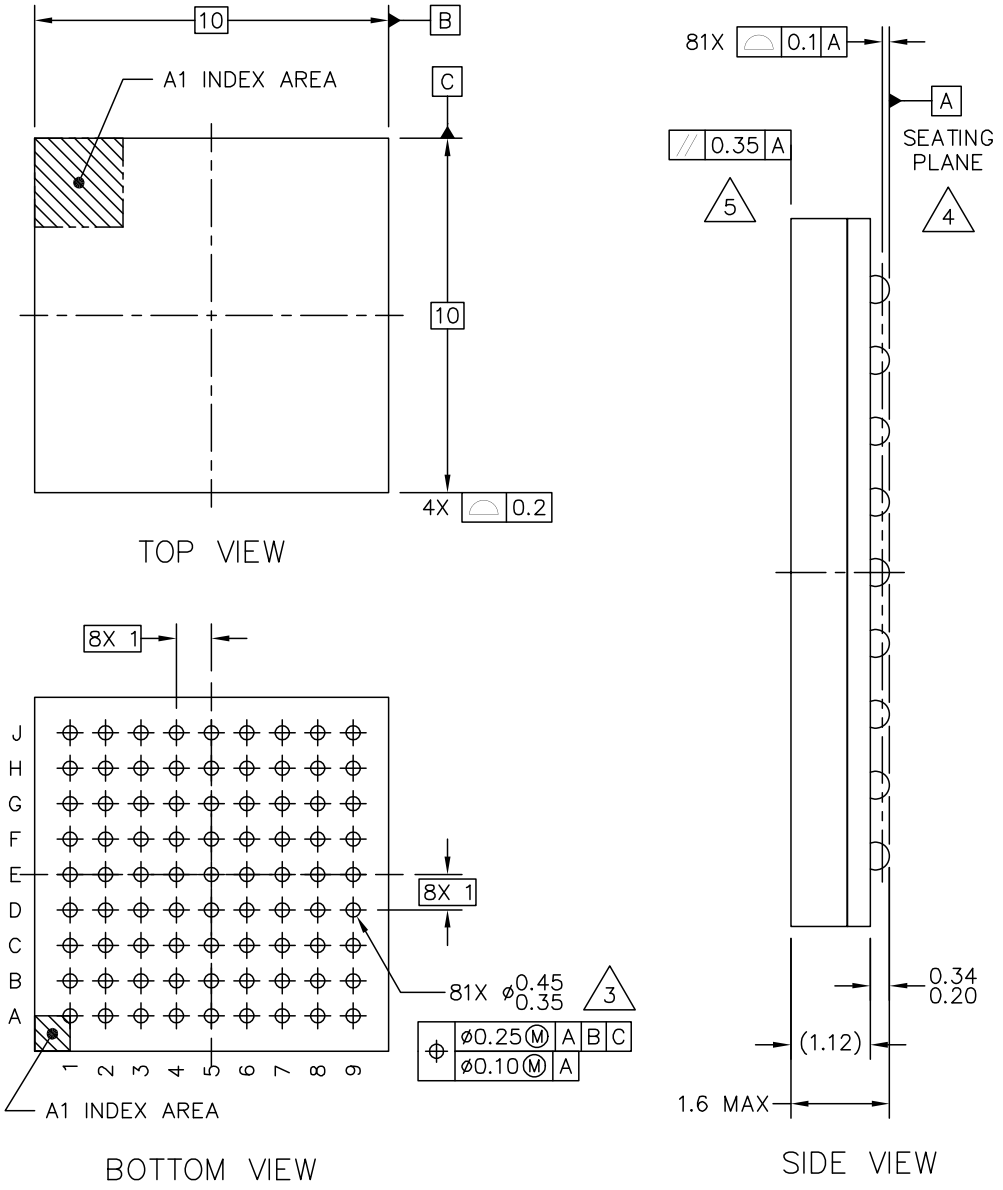
| | STANDARD: JEDEC MO-220 VMMD-3 | |
| | PACKAGE CODE: 6200 | SHEET: 4 OF 4 |

## 3.3 81 MAPBGA Package

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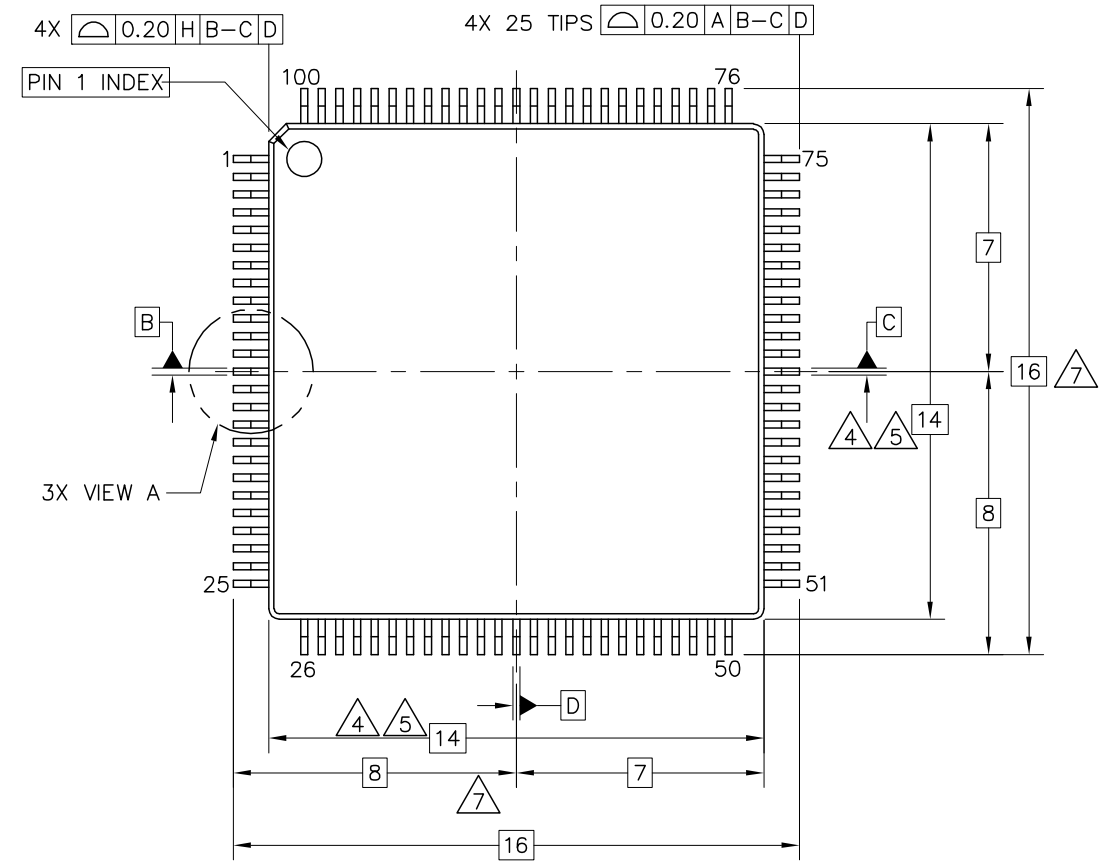
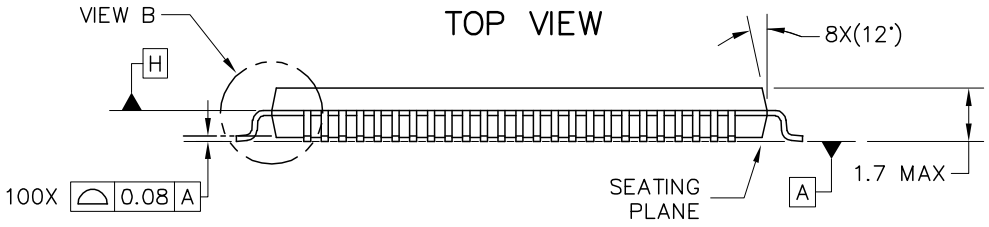
| | CASE NUMBER: 1662–01 | 04 FEB 2005 |
| | STANDARD: NON–JEDEC | |

## 3.4 100-pin LQFP Package

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|---|---|---|
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| | CASE NUMBER: 983–03 | 07 APR 2005 |
| | STANDARD: NON–JEDEC | |