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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	66MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5213caf66r

1 MCF5213 Family Configurations

Table 1. MCF5213 Family Configurations

Module	5211	5212	5213
ColdFire Version 2 Core with MAC (Multiply-Accumulate Unit)	●	●	●
System Clock	66, 80 MHz		
Performance (Dhrystone 2.1 MIPS)	63	up to 76	
Flash / Static RAM (SRAM)	128/16 Kbytes	256/32 Kbytes	
Interrupt Controller (INTC)	●	●	●
Fast Analog-to-Digital Converter (ADC)	●	●	●
FlexCAN 2.0B Module	See note[1]	—	●
Four-channel Direct-Memory Access (DMA)	●	●	●
Watchdog Timer Module (WDT)	●	●	●
Programmable Interval Timer Module (PIT)	2	2	2
Four-Channel General-Purpose Timer	3	3	3
32-bit DMA Timers	4	4	4
QSPI	●	●	●
UARTs	3	3	3
I^2C	●	●	●
PWM	8	8	8
General Purpose I/O Module (GPIO)	●	●	●
Chip Configuration and Reset Controller Module	●	●	●
Background Debug Mode (BDM)	●	●	●
JTAG - IEEE 1149.1 Test Access Port[2]	●	●	●
Package	64 LQFP 64 QFN 81 MAPBGA	64 LQFP 81 MAPBGA	81 MAPBGA 100 LQFP

1 FlexCAN is available on the MCF5211 only in the 64 QFN package.

2 The full debug/trace interface is available only on the 100-pin packages. A reduced debug interface is bonded on smaller packages.

Figure 1 shows a top-level block diagram of the MCF5213. Package options for this family are described later in this document.

  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.1.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5213 core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16×16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.1.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. The MCF5213 implements revision B+ of the ColdFire Debug Architecture.

The MCF5213's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF5213 includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

1.1.4 JTAG

The MCF5213 supports circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 256-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5213 implementation can:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF5213 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF5213 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

1.1.5 On-Chip Memories

1.1.5.1 SRAM

The dual-ported SRAM module provides a general-purpose 32-Kbyte memory block that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 32-Kbyte boundary within the 4-Gbyte address space. This memory is ideal for storing critical code or data structures and for use as the system stack. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by the DMA. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance.

1.1.5.2 Flash Memory

The ColdFire flash module (CFM) is a non-volatile memory (NVM) module that connects to the processor's high-speed local bus. The CFM is constructed with four banks of 32-Kbyte×16-bit flash memory arrays to generate 256 Kbytes of 32-bit flash memory. These electrically erasable and programmable arrays serve as non-volatile program and data memory. The flash memory is ideal for program and data storage for single-chip applications, allowing for field reprogramming without requiring an external high voltage source. The CFM interfaces to the ColdFire core through an optimized read-only memory controller that supports interleaved accesses from the 2-cycle flash memory arrays. A backdoor mapping of the flash memory is used for all program, erase, and verify operations, as well as providing a read datapath for the DMA. Flash memory may also be programmed via the EzPort, which is a serial flash memory programming interface that allows the flash memory to be read, erased and programmed by an external controller in a format compatible with most SPI bus flash memory chips.

1.1.6 Power Management

The MCF5213 incorporates several low-power modes of operation entered under program control and exited by several external trigger events. An integrated power-on reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises. The low voltage detector (LVD) monitors the supply voltage and is configurable to force a reset or interrupt condition if it falls below the LVD trip point. The RAM standby switch provides power to RAM when the supply voltage to the chip falls below the standby battery voltage.

1.1.20 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detector (LVD)

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

1.1.21 GPIO

Nearly all pins on the MCF5213 have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pins.

1.1.22 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Orderable Part Number Summary

Freescale Part Number	Description	Speed	Package	Temperature
MCF5211CAE66	MCF5211 ColdFire Microcontroller	66 MHz	64 LQFP	-40 to +85 °C
MCF5211CEP66	MCF5211 ColdFire Microcontroller, FlexCAN	66 MHz	64 QFN	-40 to +85 °C
MCF5211LCEP66	MCF5211 ColdFire Microcontroller	66 MHz	64 QFN	-40 to +85 °C
MCF5211LCVM66	MCF5211 ColdFire Microcontroller	66 MHz	81 MAPBGA	-40 to +85 °C
MCF5211LCVM80	MCF5211 ColdFire Microcontroller	80 MHz	81 MAPBGA	-40 to +85 °C
MCF5212CAE66	MCF5212 ColdFire Microcontroller	66 MHz	64 LQFP	-40 to +85 °C
MCF5212LCVM66	MCF5212 ColdFire Microcontroller	66 MHz	81 MAPBGA	-40 to +85 °C
MCF5212LCVM80	MCF5212 ColdFire Microcontroller	80 MHz	81 MAPBGA	-40 to +85 °C
MCF5213CAF66	MCF5213 ColdFire Microcontroller, FlexCAN	66 MHz	100 LQFP	-40 to +85 °C
MCF5213CAF80	MCF5213 ColdFire Microcontroller, FlexCAN	80 MHz	100 LQFP	-40 to +85 °C
MCF5213LCVM66	MCF5213 ColdFire Microcontroller, FlexCAN	66 MHz	81 MAPBGA	-40 to +85 °C
MCF5213LCVM80	MCF5213 ColdFire Microcontroller, FlexCAN	80 MHz	81 MAPBGA	-40 to +85 °C

Figure 3 shows the pinout configuration for the 81 MAPBGA.

	1	2	3	4	5	6	7	8	9
A	V_{SS}	UTXD1	$\overline{RSTI}$	$\overline{IRQ5}$	$\overline{IRQ3}$	ALLPST	TDO	TMS	V_{SS}
B	$\overline{URTS1}$	URXD1	$\overline{RSTO}$	$\overline{IRQ6}$	$\overline{IRQ2}$	$\overline{TRST}$	TDI	V_{DD}PLL	EXTAL
C	$\overline{UCTS0}$	TEST	$\overline{UCTS1}$	$\overline{IRQ7}$	$\overline{IRQ4}$	$\overline{IRQ1}$	TCLK	V_{SS}PLL	XTAL
D	URXD0	UTXD0	$\overline{URTS0}$	V_{SS}	V_{DD}	V_{SS}	PWM7	GPT3	GPT2
E	SCL	SDA	V_{DD}	V_{DD}	V_{DD}	V_{DD}	V_{DD}	PWM5	GPT1
F	QSPI_CS3	QSPI_CS2	QSPI_DIN	V_{SS}	V_{DD}	V_{SS}	GPT0	V_{STBY}	AN4
G	QSPI_DOUT	QSPI_CLK	$\overline{RCON}$	DTIN1	CLKMOD0	AN2	AN3	AN5	AN6
H	QSPI_CS0	QSPI_CS1	DTIN3	DTIN0	CLKMOD1	AN1	V_{SSA}	V_{DDA}	AN7
J	V_{SS}	JTAG_EN	DTIN2	PWM3	PWM1	AN0	V_{RL}	V_{RH}	V_{SSA}

Figure 3. 81 MAPBGA Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
Interrupts	$\overline{\text{IRQ7}}$	—	—	GPIO	Low	FAST	pull-up	95	C4	58
	$\overline{\text{IRQ6}}$	—	—	GPIO	Low	FAST	pull-up	94	B4	—
	$\overline{\text{IRQ5}}$	—	—	GPIO	Low	FAST	pull-up	91	A4	—
	$\overline{\text{IRQ4}}$	—	—	GPIO	Low	FAST	pull-up	90	C5	57
	$\overline{\text{IRQ3}}$	—	—	GPIO	Low	FAST	pull-up	89	A5	—
	$\overline{\text{IRQ2}}$	—	—	GPIO	Low	FAST	pull-up	88	B5	—
	$\overline{\text{IRQ1}}$	SYNCA	PWM1	GPIO	High	FAST	pull-up[5]	87	C6	56
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26	J2	17
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up[6]	64	C7	44
	TDI/DSI	—	—	—	N/A	N/A	pull-up[6]	79	B7	50
	TDO/DSO	—	—	—	High	FAST	—	80	A7	51
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[6]	76	A8	49
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up[6]	85	B6	54
Mode Selection[7]	CLKMOD0	—	—	—	N/A	N/A	pull-down[7]	40	G5	24
	CLKMOD1	—	—	—	N/A	N/A	pull-down[7]	39	H5	—
	$\overline{\text{RCON}}$/ EZPCS	—	—	—	N/A	N/A	pull-up	21	G3	16
PWM	PWM7	—	—	GPIO	PDSR[31]	PSRR[31]	—	63	D7	—
	PWM5	—	—	GPIO	PDSR[30]	PSRR[30]	—	60	E8	—
	PWM3	—	—	GPIO	PDSR[29]	PSRR[29]	—	33	J4	—
	PWM1	—	—	GPIO	PDSR[28]	PSRR[28]	—	38	J5	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
QSPI	QSPI_DIN/ EZPD	CANRX[4]	URXD1	GPIO	PDSR[2]	PSRR[2]	—	16	F3	12
	QSPI_DOUT/ EZPQ	CANTX[4]	UTXD1	GPIO	PDSR[1]	PSRR[1]	—	17	G1	13
	QSPI_CLK/ EZPCK	SCL	$\overline{\text{URTS1}}$	GPIO	PDSR[3]	PSRR[3]	pull-up[8]	18	G2	14
	QSPI_CS3	SYNCA	SYNCB	GPIO	PDSR[7]	PSRR[7]	—	12	F1	—
	QSPI_CS2	—	—	GPIO	PDSR[6]	PSRR[6]	—	13	F2	—
	QSPI_CS1	—	—	GPIO	PDSR[5]	PSRR[5]	—	19	H2	—
	QSPI_CS0	SDA	$\overline{\text{UCTS1}}$	GPIO	PDSR[4]	PSRR[4]	pull-up[8]	20	H1	15
Reset[9]	$\overline{\text{RSTI}}$	—	—	—	N/A	N/A	pull-up[9]	96	A3	59
	$\overline{\text{RSTO}}$	—	—	—	high	FAST	—	97	B3	60
Test	TEST	—	—	—	N/A	N/A	pull-down	5	C2	3
Timers, 16-bit	GPT3	—	PWM7	GPIO	PDSR[23]	PSRR[23]	pull-up[10]	62	D8	43
	GPT2	—	PWM5	GPIO	PDSR[22]	PSRR[22]	pull-up[10]	61	D9	42
	GPT1	—	PWM3	GPIO	PDSR[21]	PSRR[21]	pull-up[10]	59	E9	41
	GPT0	—	PWM1	GPIO	PDSR[20]	PSRR[20]	pull-up[10]	58	F7	40
Timers, 32-bit	DTIN3	DTOUT3	PWM6	GPIO	PDSR[19]	PSRR[19]	—	32	H3	19
	DTIN2	DTOUT2	PWM4	GPIO	PDSR[18]	PSRR[18]	—	31	J3	18
	DTIN1	DTOUT1	PWM2	GPIO	PDSR[17]	PSRR[17]	—	37	G4	23
	DTIN0	DTOUT0	PWM0	GPIO	PDSR[16]	PSRR[16]	—	36	H4	22
UART 0	$\overline{\text{UCTS0}}$	CANRX	—	GPIO	PDSR[11]	PSRR[11]	—	6	C1	4
	$\overline{\text{URTS0}}$	CANTX	—	GPIO	PDSR[10]	PSRR[10]	—	9	D3	7
	URXD0	—	—	GPIO	PDSR[9]	PSRR[9]	—	7	D1	5
	UTXD0	—	—	GPIO	PDSR[8]	PSRR[8]	—	8	D2	6

1.5 External Interrupt Signals

Table 8 describes the external interrupt signals.

Table 8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[7:1]	External interrupt sources.	I

1.6 Queued Serial Peripheral Interface (QSPI)

Table 9 describes the QSPI signals.

Table 9. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip select; can be programmed to be active high or low.	O

1.7 I^2C I/O Signals

Table 10 describes the I^2C serial interface module signals.

Table 10. I^2C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I^2C interface. When the bus is In master mode, this clock is driven by the I^2C module; when the bus is in slave mode, this clock becomes the clock input.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I^2C interface.	I/O

1.8 UART Module Signals

Table 11 describes the UART module signals.

Table 11. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	UTXD*n*	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, LSB first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	URXD*n*	Receiver serial data inputs for the UART modules. Data is received on this pin LSB first. When the UART clock is stopped for power-down mode, any transition on this pin restarts the clock.	I
Clear-to-Send	$\overline{\text{UCTS}}n$	Indication to the UART modules that they can begin data transmission.	I
Request-to-Send	$\overline{\text{URTS}}n$	Automatic request-to-send outputs from the UART modules. This signal can also be configured to be asserted and negated as a function of the RxFIFO level.	O

1.9 DMA Timer Signals

Table 12 describes the signals of the four DMA timer modules.

Table 12. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer Input	DTIN	Event input to the DMA timer modules.	I
DMA Timer Output	DTOUT	Programmable output from the DMA timer modules.	O

1.10 ADC Signals

Table 13 describes the signals of the Analog-to-Digital Converter.

Table 13. ADC Signals

Signal Name	Abbreviation	Function	I/O
Analog Inputs	AN[7:0]	Inputs to the analog-to-digital converter.	I
Analog Reference	V_{RH}	Reference voltage high and low inputs.	I
	V_{RL}		I
Analog Supply	V_{DDA}	Isolate the ADC circuitry from power supply noise.	—
	V_{SSA}		—
ADC Sync Inputs	SYNCA / SYNCB	These signals can initiate an analog-to-digital conversion process.	I

Table 21. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical[1] Active (SRAM)	Typical[1] Active (Flash)	Peak[2]	Unit
1 MHz core & I/O	I_{DD}	—	3.48	—	mA
8 MHz core & I/O		7.28	13.37	19.02	
16 MHz core & I/O		12.08	25.08	35.66	
64 MHz core & I/O		40.14	54.62	85.01	
80 MHz core & I/O		49.2	64.09	100.03	
RAM standby supply current • Normal operation: $V_{DD} > V_{STBY} - 0.3$ V • Transient condition: $V_{STBY} - 0.3$ V > $V_{DD} > V_{SS} + 0.5$ V • Standby operation: $V_{DD} < V_{SS} + 0.5$ V	I_{STBY}	N/A[3] N/A[3] N/A[3]		N/A[3] N/A[3] N/A[3]	µA mA µA
Analog supply current • Normal operation • Low-power stop	I_{DDA}	— —	— —	16 50	mA µA

1 Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).

2 Peak current measured with all modules active, and default drive strength with matching load.

3 Due to the errata “Non-functional RAM Standby Supply” in the *MCF5213 Device Errata*, V_{STBY} should be connected directly to V_{DD} and cannot be used for RAM standby operation.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33[1,3]	°C/W
	Junction to board	—	θ_{JB}	25[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Figure 7 shows timing for the values in Table 30 and Table 31.

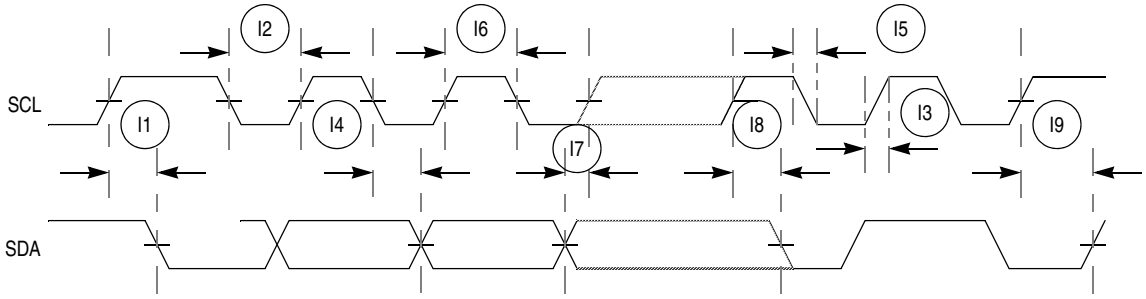


Figure 7. I²C Input/Output Timings

2.11 Analog-to-Digital Converter (ADC) Parameters

Table 32 lists specifications for the analog-to-digital converter.

Table 32. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 8	—	pF
X_{IN}	Input impedance	—	See Figure 8	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	m
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	TBD	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB

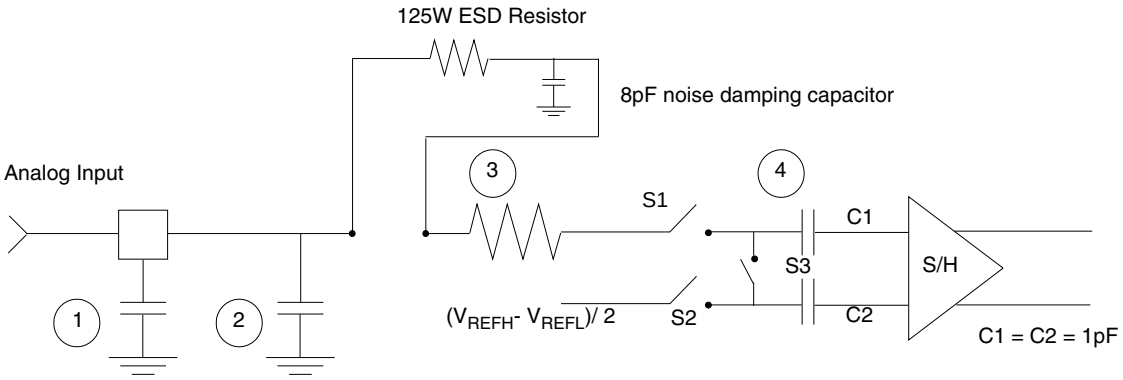
Table 32. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

1 All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground
2 INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$
3 LSB = Least Significant Bit
4 INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$
5 Includes power-up of ADC and V_{REF}
6 ADC clock cycles
7 Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.12 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to $(V_{REFH}-V_{REFL})/2$, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about $(V_{REFH}-V_{REFL})/2$. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. Equivalent resistance for the channel select mux; 100 Ωs
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4 \times 10^{-12})}$

Figure 8. Equivalent Circuit for A/D Loading

2.15 JTAG and Boundary Scan Timing

Table 35. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

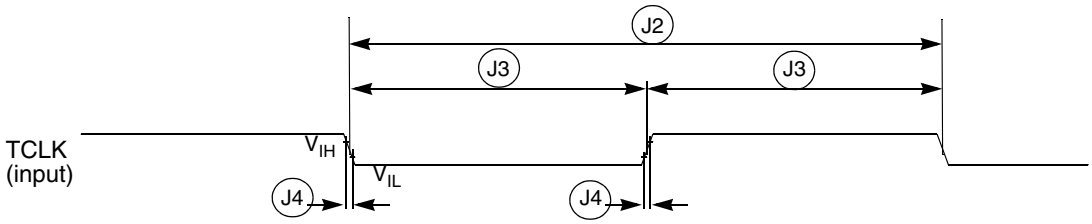


Figure 10. Test Clock Input Timing

Figure 15 shows BDM serial port AC timing for the values in Table 36.

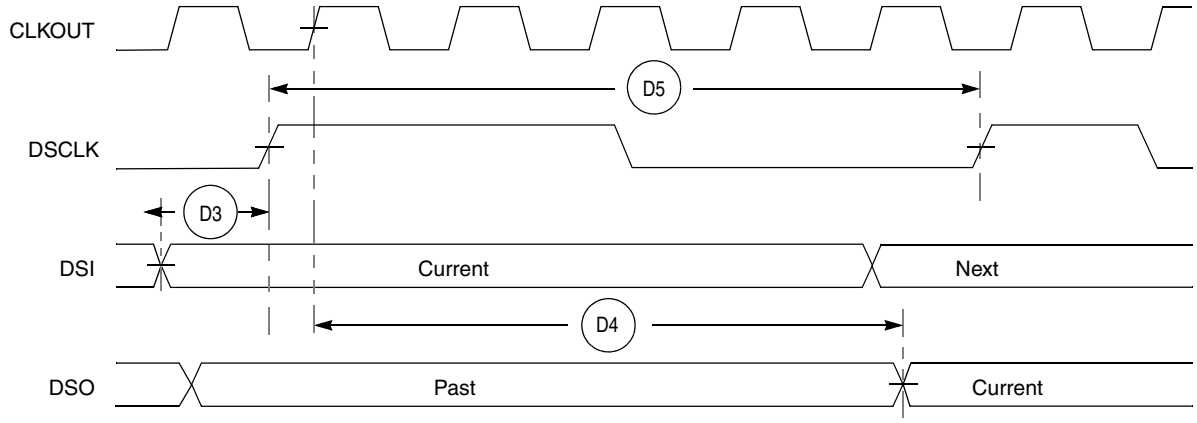


Figure 15. BDM Serial Port AC Timing

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

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TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: D
	CASE NUMBER: 840F-02	06 APR 2005
	STANDARD: JEDEC MS-026 BCD	

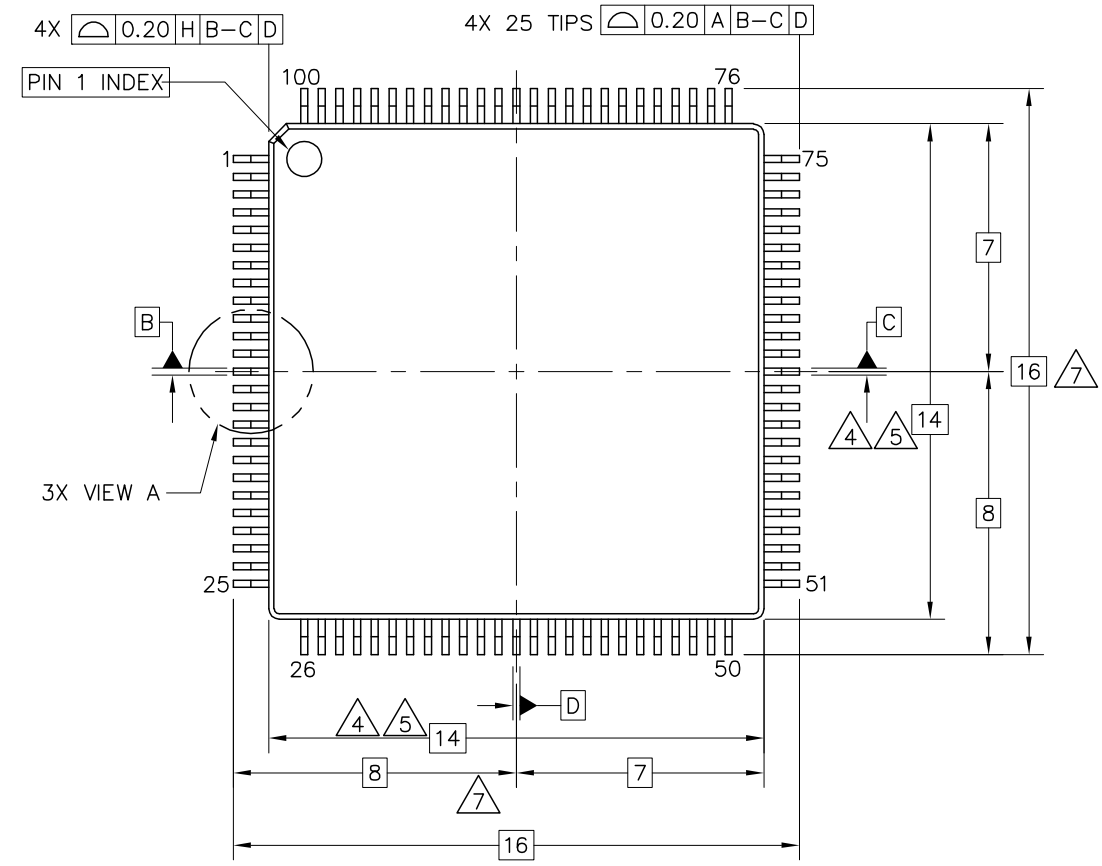
NOTES:

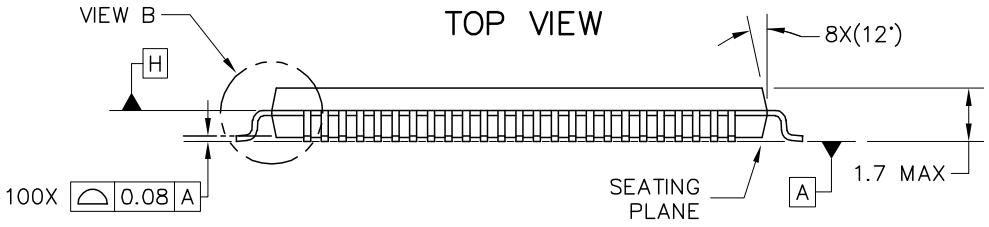
1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: PBGA, LOW PROFILE, 81 I/O, 10 X 10 PKG, 1 MM PITCH (MAP)	DOCUMENT NO: 98ASA10670D	REV: O
	CASE NUMBER: 1662–01	04 FEB 2005
	STANDARD: NON–JEDEC	

3.4 100-pin LQFP Package





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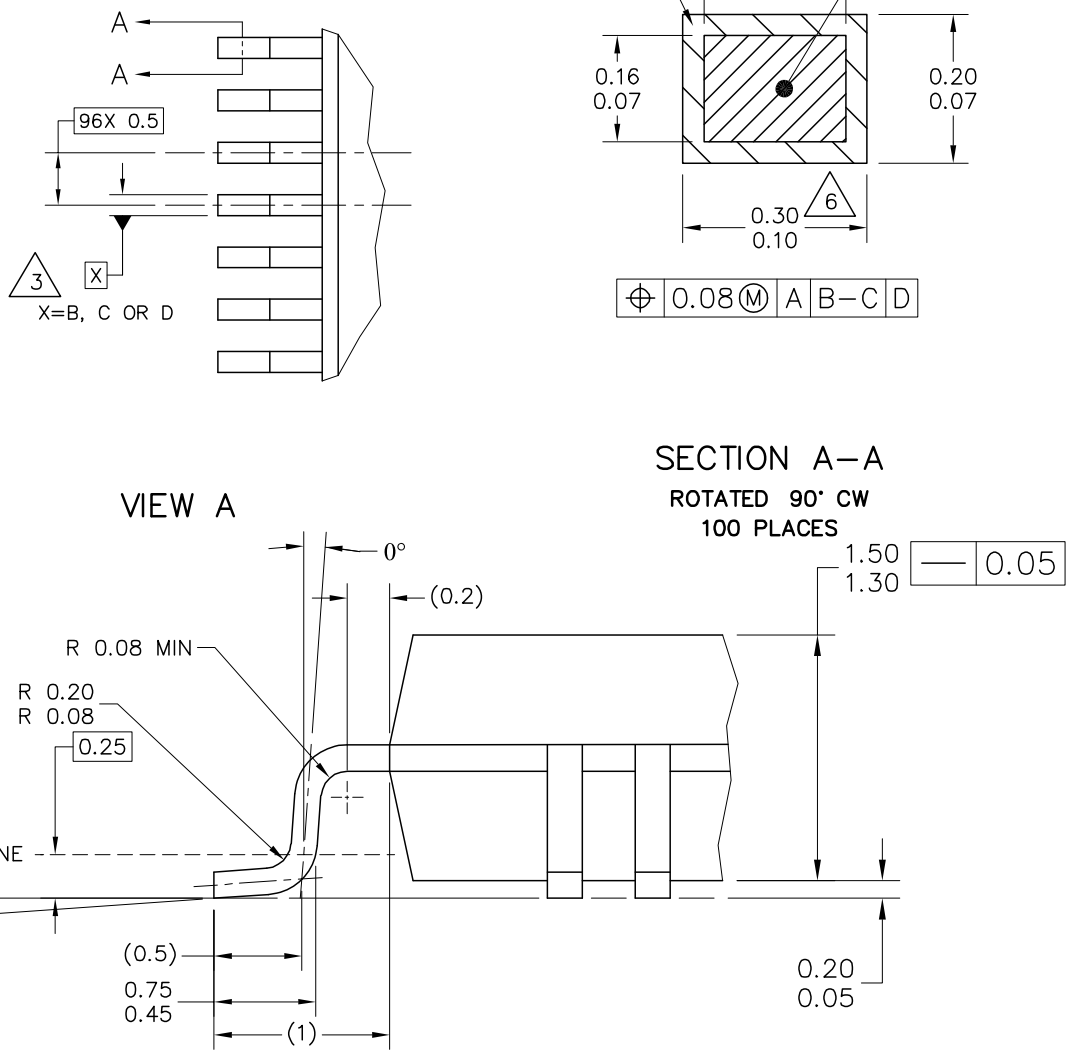
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	



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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	

4 Revision History

Table 37. Revision History

Revision	Description
2	• Formatting, layout, spelling, and grammar corrections. • Added revision history. • Corrected signal names in block diagram to match those in signal description table. • Added the following footnote to the MCF5211 FlexCAN entry: "FlexCAN is available on the MCF5211 only in the 64 QFN package." • Added an entry for standby voltage (V_{STBY}) to the "DC electrical specifications" table. • Deleted the PSTCLK cycle time row in the "Debug AC timing specifications" table. • Changed the frequency above the "Min" and "Max" column headings in the "Debug AC timing specifications" table (was 166 MHz, is 66/80 MHz). • Changed the minimum value for SNR, THD, SFDR, and SINAD in the "ADC parameters" table (was TBD, is "—"). • In the "Pin Functions by Primary and Alternate Purpose" table, changed the value in the "Pull-up/pull-down" column for $\overline{IRQ2}$-$\overline{IRQ6}$ (was "—", is "pull-up"). • Added values for I_{OH} and I_{OL} to the "DC electrical specifications" table. • Added load test condition information to the "General Purpose I/O Timing" section. • Deleted the "80 MHz (Peak)" column from the "Current Consumption in Low-Power Mode" table. • In the "Typical Active Current Consumption Specifications" table, changed the typical active (SRAM) and peak I_{DD} values for the 1 MHz core & I/O entry (were TBD, are "—"). • Changed the I_{STBY} values In the "Typical Active Current Consumption Specifications" table (were 0 or TBD, are "—") and added an explanatory footnote referring to the *MCF5213 Device Errata*. • Changed the I_{DDA} values In the "Typical Active Current Consumption Specifications" table (were TBD, are 16 mA for normal operation and 50 μA for low-power stop).
3	• Formatting, layout, spelling, and grammar corrections. • Synchronized the "Pin Functions by Primary and Alternate Purpose" table in this document and the reference manual. • Restructured the part number summary table to include full orderable parts, and changed its name (was "Part Number Summary", is "Orderable Part Number Summary"). • Updated the family configurations table to show that FlexCAN is not available on the MCF5212. • Added specifications for V_{LVD} and V_{LVDHYS} to the "DC electrical specifications" table.

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