NXP USA Inc. - MCF5213CAF80 Datasheet

Details	
Product Status	Not For New Designs
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	55
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5213caf80

Table of Contents

List of Figures

List of Tables

1 MCF5213 Family Configurations

Table 1. MCF5213 Family Configurations

Module	5211	5212	5213
ColdFire Version 2 Core with MAC (Multiply-Accumulate Unit)	●	●	●
System Clock	66, 80 MHz		
Performance (Dhrystone 2.1 MIPS)	63	up to 76	
Flash / Static RAM (SRAM)	128/16 Kbytes	256/32 Kbytes	
Interrupt Controller (INTC)	●	●	●
Fast Analog-to-Digital Converter (ADC)	●	●	●
FlexCAN 2.0B Module	See note[1]	—	●
Four-channel Direct-Memory Access (DMA)	●	●	●
Watchdog Timer Module (WDT)	●	●	●
Programmable Interval Timer Module (PIT)	2	2	2
Four-Channel General-Purpose Timer	3	3	3
32-bit DMA Timers	4	4	4
QSPI	●	●	●
UARTs	3	3	3
I^2C	●	●	●
PWM	8	8	8
General Purpose I/O Module (GPIO)	●	●	●
Chip Configuration and Reset Controller Module	●	●	●
Background Debug Mode (BDM)	●	●	●
JTAG - IEEE 1149.1 Test Access Port[2]	●	●	●
Package	64 LQFP 64 QFN 81 MAPBGA	64 LQFP 81 MAPBGA	81 MAPBGA 100 LQFP

[1] FlexCAN is available on the MCF5211 only in the 64 QFN package.

[2] The full debug/trace interface is available only on the 100-pin packages. A reduced debug interface is bonded on smaller packages.

Figure 1 shows a top-level block diagram of the MCF5213. Package options for this family are described later in this document.

- Version 2 ColdFire variable-length RISC processor core
    - Static operation
    - 32-bit address and data paths on-chip
    - Up to 80 MHz processor core frequency
    - Sixteen general-purpose, 32-bit data and address registers
    - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
    - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support $16\times16 \rightarrow 32$ or $32\times32 \rightarrow 32$ operations
    - Illegal instruction decode that allows for 68-Kbyte emulation support
- System debug support
    - Real-time trace for determining dynamic execution path
    - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
    - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
    - 32-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
    - 256 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
    - Fully static operation with processor sleep and whole chip stop modes
    - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
    - Clock enable/disable for each peripheral when not used
- FlexCAN 2.0B module
    - Based on and includes all existing features of the Freescale TouCAN module
    - Full implementation of the CAN protocol specification version 2.0B
        - Standard data and remote frames (up to 109 bits long)
        - Extended data and remote frames (up to 127 bits long)
        - Zero to eight bytes data length
        - Programmable bit rate up to 1 Mbit/sec
    - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
    - Unused MB space can be used as general purpose RAM space
    - Listen-only mode capability
    - Content-related addressing
    - No read/write semaphores
    - Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
    - Programmable transmit-first scheme: lowest ID or lowest buffer number
    - Time stamp based on 16-bit free-running timer
    - Global network time, synchronized by a specific message
    - Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
    - 16-bit divider for clock generation
    - Interrupt control logic with maskable interrupts
    - DMA support
    - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
    - Up to two stop bits in 1/16 increments

  - Programmable center or left aligned outputs on individual channels
  - Four clock sources (A, B, SA, and SB) provide for a wide range of frequencies
  - Emergency shutdown
- Two periodic interrupt timers (PITs)
  - 16-bit counter
  - Selectable as free running or count down
- Software watchdog timer
  - 32-bit counter
  - Low-power mode support
- Clock generation features
  - One to 48 MHz crystal, 8 MHz on-chip relaxation oscillator, or external oscillator reference options
  - Trimmed relaxation oscillator
  - Two to 10 MHz reference frequency for normal PLL mode with a pre-divider programmable from 1 to 8
  - System can be clocked from PLL or directly from crystal oscillator or relaxation oscillator
  - Low power modes supported
  - 2^n ($n \leq 0 \leq 15$) low-power divider for extremely low frequency operation
- Interrupt controller
  - Uniquely programmable vectors for all interrupt sources
  - Fully programmable level and priority for all peripheral interrupt sources
  - Seven external interrupt signals with fixed level and priority
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low-power modes
- DMA controller
  - Four fully programmable channels
  - Dual-address transfer support with 8-, 16-, and 32-bit data capability, along with support for 16-byte (4×32-bit) burst transfers
  - Source/destination address pointers that can increment or remain constant
  - 24-bit byte transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Software-programmable DMA requesters for the UARTs (3) and 32-bit timers (4)
- Reset
  - Separate reset in and reset out signals
  - Seven sources of reset:
    - Power-on reset (POR)
    - External
    - Software
    - Watchdog
    - Loss of clock
    - Loss of lock
    - Low-voltage detection (LVD)
  - Status flag indication of source of last reset
- Chip integration module (CIM)

1.1.20 Reset

The reset controller determines the source of reset, asserts the appropriate reset signals to the system, and keeps track of what caused the last reset. There are seven sources of reset:

- External reset input
- Power-on reset (POR)
- Watchdog timer
- Phase locked-loop (PLL) loss of lock
- PLL loss of clock
- Software
- Low-voltage detector (LVD)

Control of the LVD and its associated reset and interrupt are managed by the reset controller. Other registers provide status flags indicating the last source of reset and a control bit for software assertion of the $\overline{\text{RSTO}}$ pin.

1.1.21 GPIO

Nearly all pins on the MCF5213 have general purpose I/O capability and are grouped into 8-bit ports. Some ports do not use all eight bits. Each port has registers that configure, monitor, and control the port pins.

1.1.22 Part Numbers and Packaging

This product is RoHS-compliant. Refer to the product page at freescale.com or contact your sales office for up-to-date RoHS information.

Table 2. Orderable Part Number Summary

Freescale Part Number	Description	Speed	Package	Temperature
MCF5211CAE66	MCF5211 ColdFire Microcontroller	66 MHz	64 LQFP	-40 to +85 °C
MCF5211CEP66	MCF5211 ColdFire Microcontroller, FlexCAN	66 MHz	64 QFN	-40 to +85 °C
MCF5211LCEP66	MCF5211 ColdFire Microcontroller	66 MHz	64 QFN	-40 to +85 °C
MCF5211LCVM66	MCF5211 ColdFire Microcontroller	66 MHz	81 MAPBGA	-40 to +85 °C
MCF5211LCVM80	MCF5211 ColdFire Microcontroller	80 MHz	81 MAPBGA	-40 to +85 °C
MCF5212CAE66	MCF5212 ColdFire Microcontroller	66 MHz	64 LQFP	-40 to +85 °C
MCF5212LCVM66	MCF5212 ColdFire Microcontroller	66 MHz	81 MAPBGA	-40 to +85 °C
MCF5212LCVM80	MCF5212 ColdFire Microcontroller	80 MHz	81 MAPBGA	-40 to +85 °C
MCF5213CAF66	MCF5213 ColdFire Microcontroller, FlexCAN	66 MHz	100 LQFP	-40 to +85 °C
MCF5213CAF80	MCF5213 ColdFire Microcontroller, FlexCAN	80 MHz	100 LQFP	-40 to +85 °C
MCF5213LCVM66	MCF5213 ColdFire Microcontroller, FlexCAN	66 MHz	81 MAPBGA	-40 to +85 °C
MCF5213LCVM80	MCF5213 ColdFire Microcontroller, FlexCAN	80 MHz	81 MAPBGA	-40 to +85 °C

1.2 Reset Signals

Table 4 describes signals used to reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 1024 CPU clocks after the reset source has deasserted.	O

1.3 PLL and Clock Signals

Table 5 describes signals used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD1=1, then sampled as part of the clock mode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.4 Mode Selection

Table 6 describes signals used in mode selection; Table 7 describes the particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

Table 7. Clocking Modes

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator
10	1	PLL in normal mode, clock driven by on-chip oscillator
11	N/A	PLL in normal mode, clock driven by crystal

Table 16. Debug Support Signals (continued)

Signal Name	Abbreviation	Function	I/O
Development Serial Input	DSI	Development Serial Input - Internally synchronized input that provides data input for the serial communication port to the debug module, after the DSCLK has been seen as high (logic 1).	I
Development Serial Output	DSO	Development Serial Output - Provides serial output communication for debug module responses. DSO is registered internally. The output is delayed from the validation of DSCLK high.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Clock	PSTCLK	Processor Status Clock - Delayed version of the processor clock. Its rising edge appears in the center of valid PST and DDATA output. PSTCLK indicates when the development system should sample PST and DDATA values. If real-time trace is not used, setting CSR[PCD] keeps PSTCLK, and PST and DDATA outputs from toggling without disabling triggers. Non-quiescent operation can be reenabled by clearing CSR[PCD], although the external development systems must resynchronize with the PST and DDATA outputs. PSTCLK starts clocking only when the first non-zero PST value (0xC, 0xD, or 0xF) occurs during system reset exception processing.	O
Processor Status Outputs	PST[3:0]	Indicate core status. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O
All Processor Status Outputs	ALLPST	Logical AND of PST[3:0]. The CLKOUT signal can be used by the development system to know when to sample ALLPST.	O

1.14 EzPort Signal Descriptions

Table contains a list of EzPort external signals.

Table 17. EzPort Signal Descriptions

Signal Name	Abbreviation	Function	I/O
EzPort Clock	EZPCK	Shift clock for EzPort transfers.	I
EzPort Chip Select	EZPCS	Chip select for signalling the start and end of serial transfers.	I
EzPort Serial Data In	EZPD	EZPD is sampled on the rising edge of EZPCK.	I
EzPort Serial Data Out	EZPQ	EZPQ transitions on the falling edge of EZPCK.	O

1.15 Power and Ground Pins

The pins described in Table 18 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 18. Power and Ground Pins

Signal Name	Abbreviation	Function
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.
Positive Supply	VDD	These pins supply positive power to the core logic.
Ground	VSS	This pin is the negative supply (ground) to the chip.

2 Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF5213 microcontroller unit, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C
Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts
$P_{I/O}$ = power dissipation on input and output pins — user determined, watts

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^{\ 2} \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 23 and Table 24.

Table 23. SGFM Flash Program and Erase Characteristics

(V_{DDF} = 2.7 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	66.67 or 80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	66.67 or 80[1]	MHz

[1] Depending on packaging; see Table 2.
[2] Refer to the flash memory section for more information

Table 24. SGFM Flash Module Life Characteristics

(V_{DDF} = 2.7 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

[1] A program/erase cycle is defined as switching the bits from 1 → 0 → 1.
[2] Reprogramming of a flash memory array block prior to erase is not required.

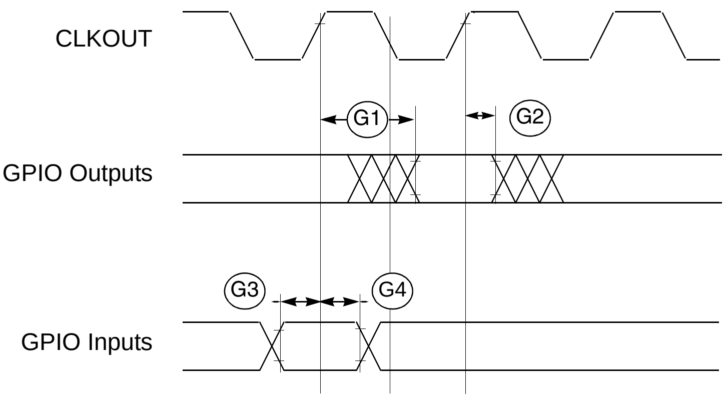


Figure 5. GPIO Timing

2.9 Reset Timing

Table 29. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

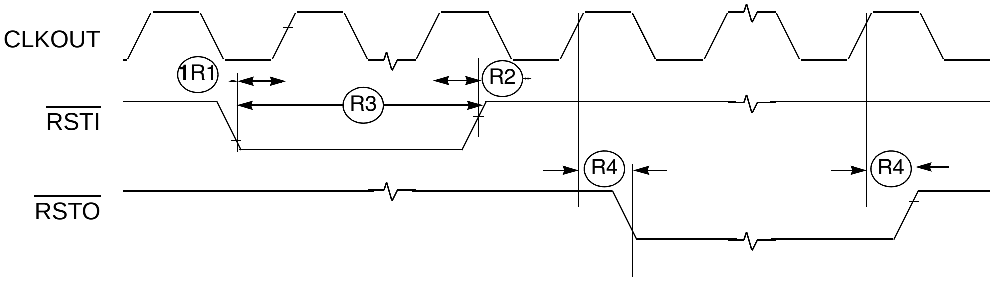


Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

2.10 I^2C Input/Output Timing Specifications

Table 30 lists specifications for the I^2C input timing parameters shown in Figure 7.

Table 30. I^2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11	Start condition hold time	$2 \times t_{CYC}$	—	ns
I2	Clock low period	$8 \times t_{CYC}$	—	ns
I3	SCL/SDA rise time ($V_{IL} = 0.5$ V to $V_{IH} = 2.4$ V)	—	1	ms
I4	Data hold time	0	—	ns
I5	SCL/SDA fall time ($V_{IH} = 2.4$ V to $V_{IL} = 0.5$ V)	—	1	ms
I6	Clock high time	$4 \times t_{CYC}$	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	$2 \times t_{CYC}$	—	ns
I9	Stop condition setup time	$2 \times t_{CYC}$	—	ns

Table 31 lists specifications for the I^2C output timing parameters shown in Figure 7.

Table 31. I^2C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
11[1]	Start condition hold time	$6 \times t_{CYC}$	—	ns
I2[1]	Clock low period	$10 \times t_{CYC}$	—	ns
I3[2]	I2C_SCL/I2C_SDA rise time ($V_{IL} = 0.5$ V to $V_{IH} = 2.4$ V)	—	—	µs
I4[1]	Data hold time	$7 \times t_{CYC}$	—	ns
I5[3]	I2C_SCL/I2C_SDA fall time ($V_{IH} = 2.4$ V to $V_{IL} = 0.5$ V)	—	3	ns
I6[1]	Clock high time	$10 \times t_{CYC}$	—	ns
I7[1]	Data setup time	$2 \times t_{CYC}$	—	ns
I8[1]	Start condition setup time (for repeated start condition only)	$20 \times t_{CYC}$	—	ns
I9[1]	Stop condition setup time	$10 \times t_{CYC}$	—	ns

[1] Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 31. The I^2C interface is designed to scale the actual data transition time to move it to the middle of the SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 31 are minimum values.

[2] Because SCL and SDA are open-collector-type outputs, which the processor can only actively drive low, the time SCL or SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.

[3] Specified at a nominal 50-pF load.

Figure 7 shows timing for the values in Table 30 and Table 31.

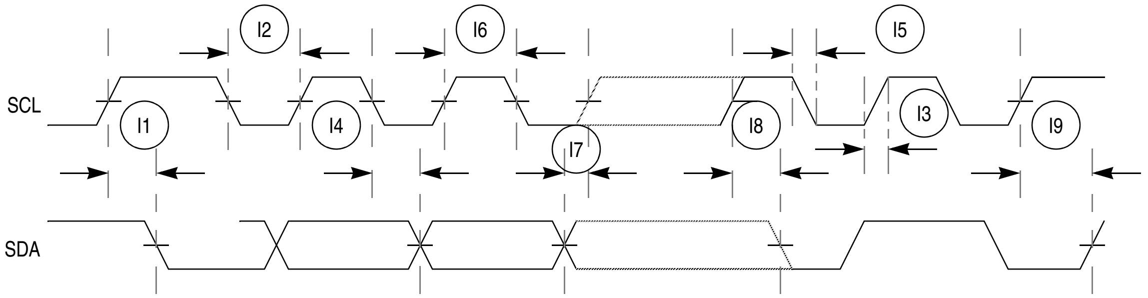


Figure 7. I^2C Input/Output Timings

2.11 Analog-to-Digital Converter (ADC) Parameters

Table 32 lists specifications for the analog-to-digital converter.

Table 32. ADC Parameters[1]

Name	Characteristic	Min	Typical	Max	Unit
V_{REFL}	Low reference voltage	V_{SS}	—	V_{REFH}	V
V_{REFH}	High reference voltage	V_{REFL}	—	V_{DDA}	V
V_{DDA}	ADC analog supply voltage	3.0	3.3	3.6	V
V_{ADIN}	Input voltages	V_{REFL}	—	V_{REFH}	V
RES	Resolution	12	—	12	Bits
INL	Integral non-linearity (full input signal range)[2]	—	±2.5	±3	LSB[3]
INL	Integral non-linearity (10% to 90% input signal range)[4]	—	±2.5	±3	LSB
DNL	Differential non-linearity	—	–1 < DNL < +1	<+1	LSB
Monotonicity		GUARANTEED			
f_{ADIC}	ADC internal clock	0.1	—	5.0	MHz
R_{AD}	Conversion range	V_{REFL}	—	V_{REFH}	V
t_{ADPU}	ADC power-up time[5]	—	6	13	t_{AIC} cycles[6]
t_{REC}	Recovery from auto standby	—	0	1	t_{AIC} cycles
t_{ADC}	Conversion time	—	6	—	t_{AIC} cycles
t_{ADS}	Sample time	—	1	—	t_{AIC} cycles
C_{ADI}	Input capacitance	—	See Figure 8	—	pF
X_{IN}	Input impedance	—	See Figure 8	—	W
I_{ADI}	Input injection current[7], per pin	—	—	3	mA
I_{VREFH}	V_{REFH} current	—	0	—	m
V_{OFFSET}	Offset voltage internal reference	—	±8	±15	mV
E_{GAIN}	Gain error (transfer path)	.99	1	1.01	—
V_{OFFSET}	Offset voltage external reference	—	±3	TBD	mV
SNR	Signal-to-noise ratio	—	62 to 66	—	dB

Table 32. ADC Parameters[1] (continued)

Name	Characteristic	Min	Typical	Max	Unit
THD	Total harmonic distortion	—	–75	—	dB
SFDR	Spurious free dynamic range	—	67 to 70.3	—	dB
SINAD	Signal-to-noise plus distortion	—	61 to 63.9	—	dB
ENOB	Effective number of bits	9.1	10.6	—	Bits

[1] All measurements are preliminary pending full characterization, and made at V_{DD} = 3.3V, V_{REFH} = 3.3V, and V_{REFL} = ground

[2] INL measured from $V_{IN} = V_{REFL}$ to $V_{IN} = V_{REFH}$

[3] LSB = Least Significant Bit

[4] INL measured from $V_{IN} = 0.1V_{REFH}$ to $V_{IN} = 0.9V_{REFH}$

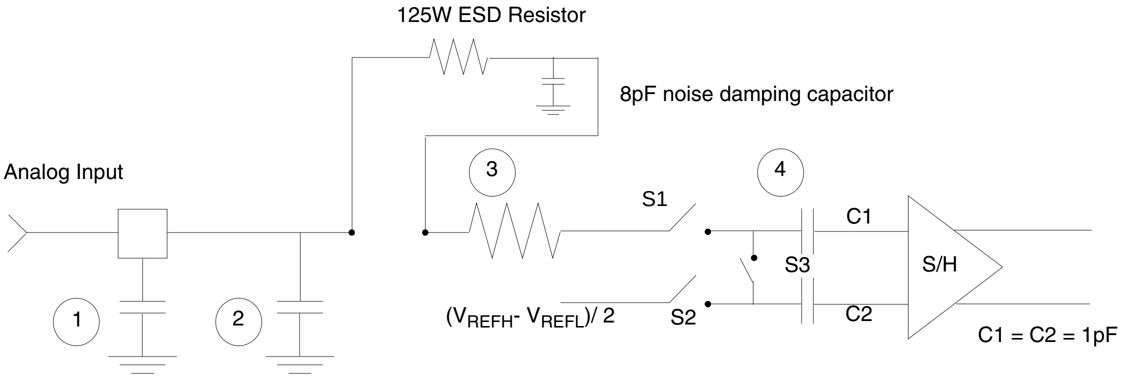
[5] Includes power-up of ADC and V_{REF}

[6] ADC clock cycles

[7] Current that can be injected or sourced from an unselected ADC signal input without impacting the performance of the ADC

2.12 Equivalent Circuit for ADC Inputs

Figure 10-17 shows the ADC input circuit during sample and hold. S1 and S2 are always open/closed at the same time that S3 is closed/open. When S1/S2 are closed & S3 is open, one input of the sample and hold circuit moves to (V_{REFH}-V_{REFL})/2, while the other charges to the analog input voltage. When the switches are flipped, the charge on C1 and C2 are averaged via S3, with the result that a single-ended analog input is switched to a differential voltage centered about (V_{REFH}-V_{REFL})/2. The switches switch on every cycle of the ADC clock (open one-half ADC clock, closed one-half ADC clock). There are additional capacitances associated with the analog input pad, routing, etc., but these do not filter into the S/H output voltage, as S1 provides isolation during the charge-sharing phase. One aspect of this circuit is that there is an on-going input current, which is a function of the analog input voltage, V_{REF} and the ADC clock frequency.



1. Parasitic capacitance due to package, pin-to-pin and pin-to-package base coupling; 1.8pF
2. Parasitic capacitance due to the chip bond pad, ESD protection devices and signal routing; 2.04pF
3. Equivalent resistance for the channel select mux; 100 Ωs
4. Sampling capacitor at the sample and hold circuit. Capacitor C1 is normally disconnected from the input and is only connected to it at sampling time; 1.4pF
5. Equivalent input impedance, when the input is selected = $\frac{1}{(\text{ADC Clock Rate}) \times (1.4\times10^{-12})}$

Figure 8. Equivalent Circuit for A/D Loading

2.15 JTAG and Boundary Scan Timing

Table 35. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK frequency of operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK cycle period	t_{JCYC}	$4 \times t_{CYC}$	—	ns
J3	TCLK clock pulse width	t_{JCW}	26	—	ns
J4	TCLK rise and fall times	t_{JCRF}	0	3	ns
J5	Boundary scan input data setup time to TCLK rise	t_{BSDST}	4	—	ns
J6	Boundary scan input data hold time after TCLK rise	t_{BSDHT}	26	—	ns
J7	TCLK low to boundary scan output data valid	t_{BSDV}	0	33	ns
J8	TCLK low to boundary scan output high Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI input data setup time to TCLK rise	t_{TAPBST}	4	—	ns
J10	TMS, TDI Input data hold time after TCLK rise	t_{TAPBHT}	10	—	ns
J11	TCLK low to TDO data valid	t_{TDODV}	0	26	ns
J12	TCLK low to TDO high Z	t_{TDODZ}	0	8	ns
J13	$\overline{\text{TRST}}$ assert time	t_{TRSTAT}	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	t_{TRSTST}	10	—	ns

[1] JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

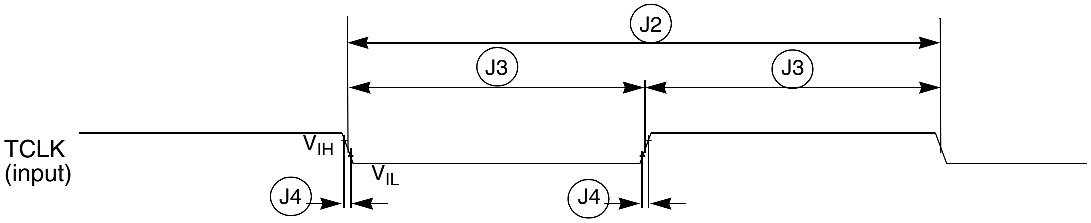


Figure 10. Test Clock Input Timing

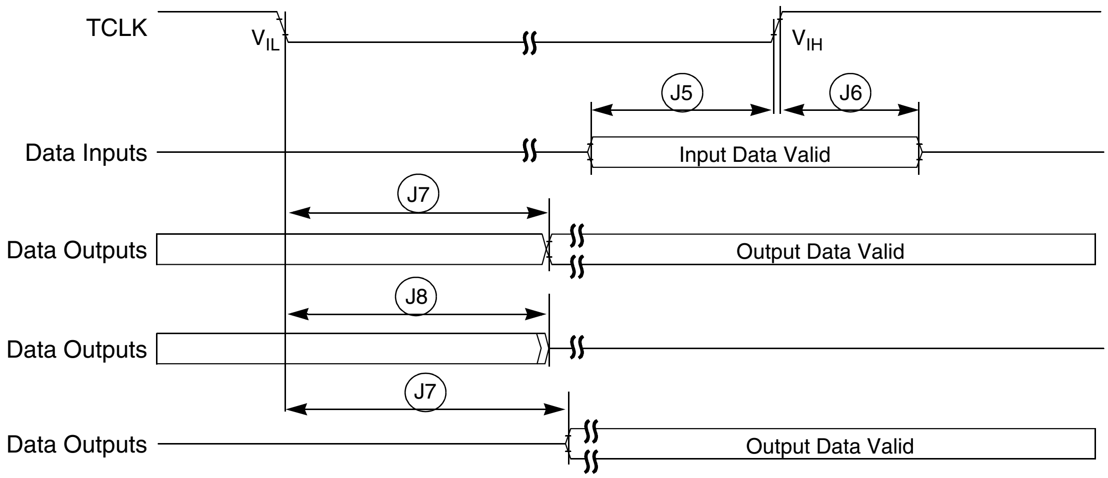


Figure 11. Boundary Scan (JTAG) Timing

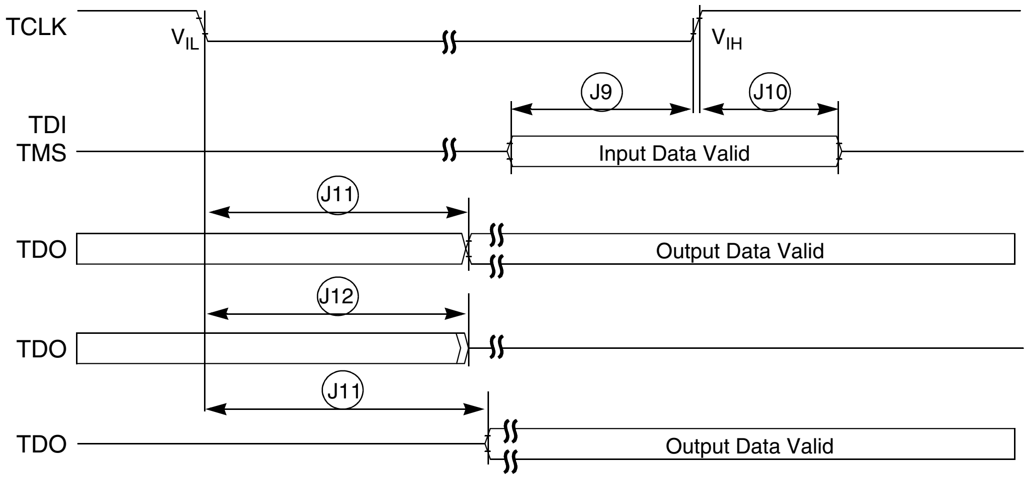


Figure 12. Test Access Port Timing

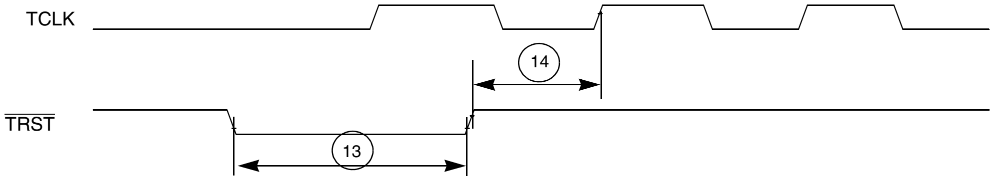


Figure 13. $\overline{\text{TRST}}$ Timing

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		PAGE: 1740
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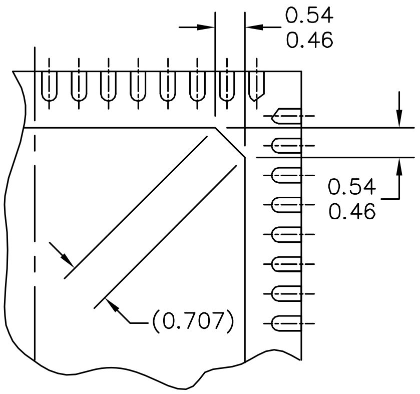
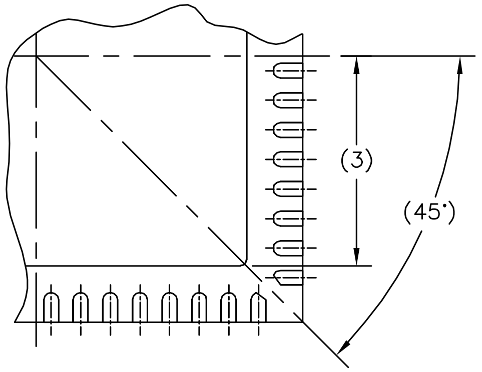


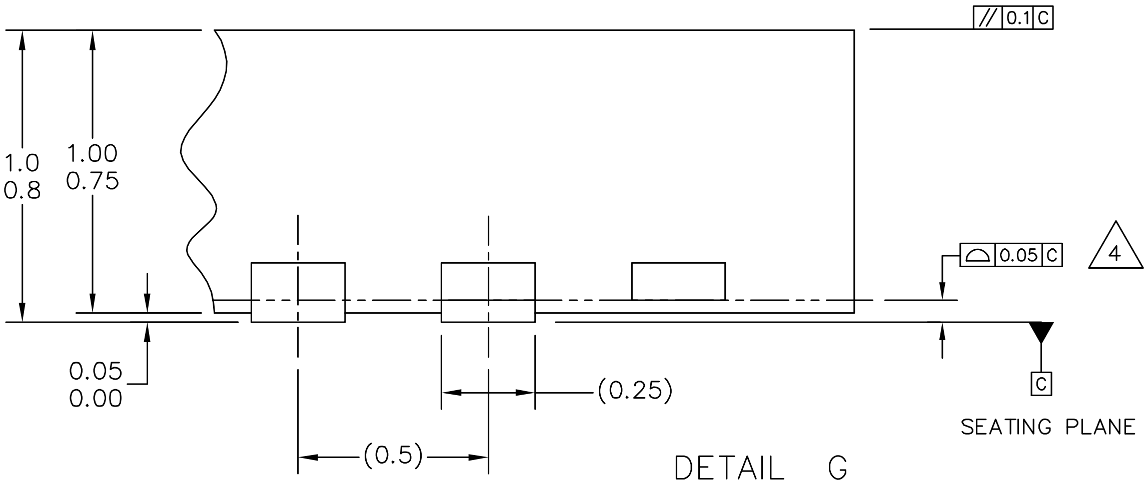
DETAIL M

PREFERRED PIN1 BACKSIDE IDENTIFIER



DETAIL N

PREFERRED CORNER CONFIGURATION



DETAIL G

VIEW ROTATED 90° CW

TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740–01	
	STANDARD: JEDEC MO–220 VMMD–3	
	PACKAGE CODE: 6200	SHEET: 2 OF 4

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		PAGE: 1740
	DO NOT SCALE THIS DRAWING	REV: O

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.

3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF−PQFN.

△4. COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

5. MIN METAL GAP SHOULD BE 0.2MM.

TITLE: THERMALLY ENHANCED QUAD FLAT NON−LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740−01	
	STANDARD: JEDEC MO−220 VMMD−3	
	PACKAGE CODE: 6200	SHEET: 3 OF 4

REVISION HISTORY

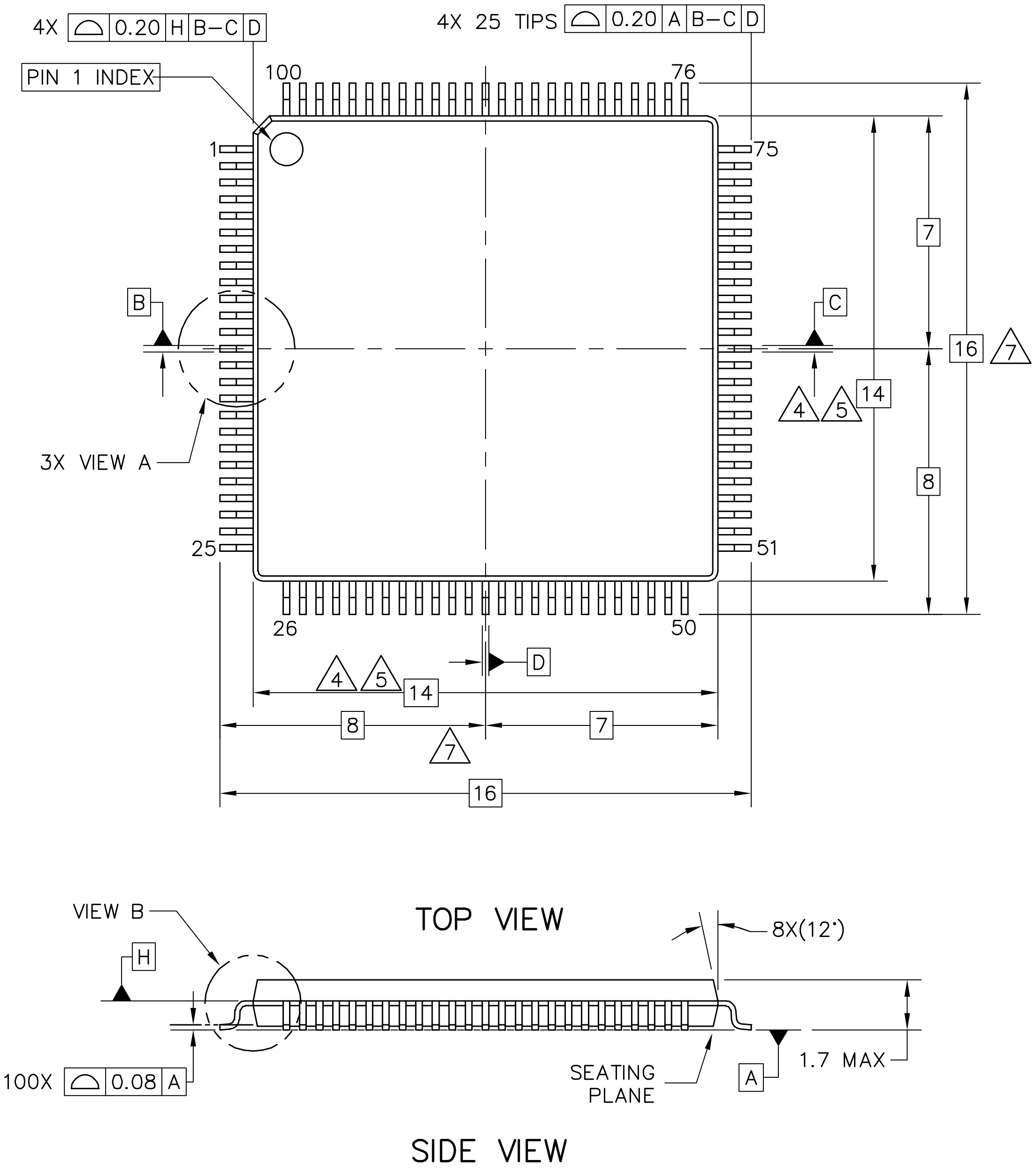
DOCUMENT NO: 98ASA10690D
PAGE: 1740
REV: O

LTR	ORIGINATOR	REVISIONS	DRAFTER	DATE
O	ERIC TRIPLETT	RELEASED FOR PRODUCTION	TAYLOR LIU	27JUL2005

TITLE: THERMALLY ENHANCED QUAD
FLAT NON-LEADED PACKAGE (QFN)
64 TERMINAL, 0.5 PITCH (9 X 9 X 1)

CASE NUMBER: 1740-01
STANDARD: JEDEC MO-220 VMMD-3
PACKAGE CODE: 6200
SHEET: 4 OF 4

3.4 100-pin LQFP Package



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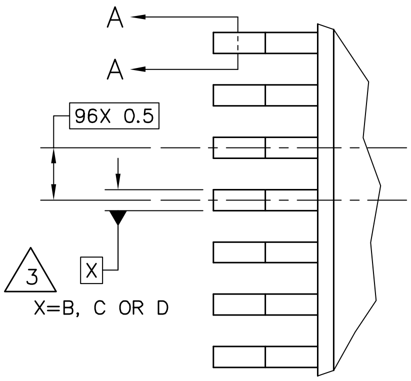
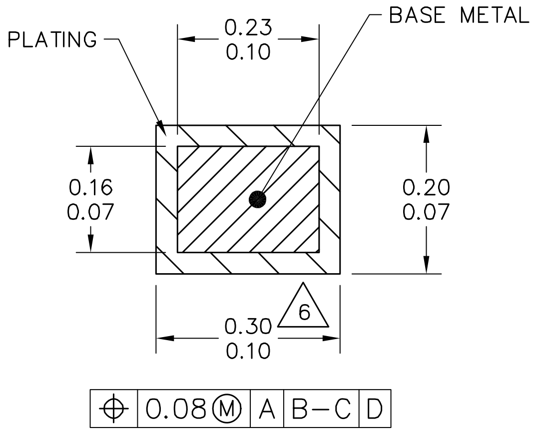
TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W	REV: G
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	



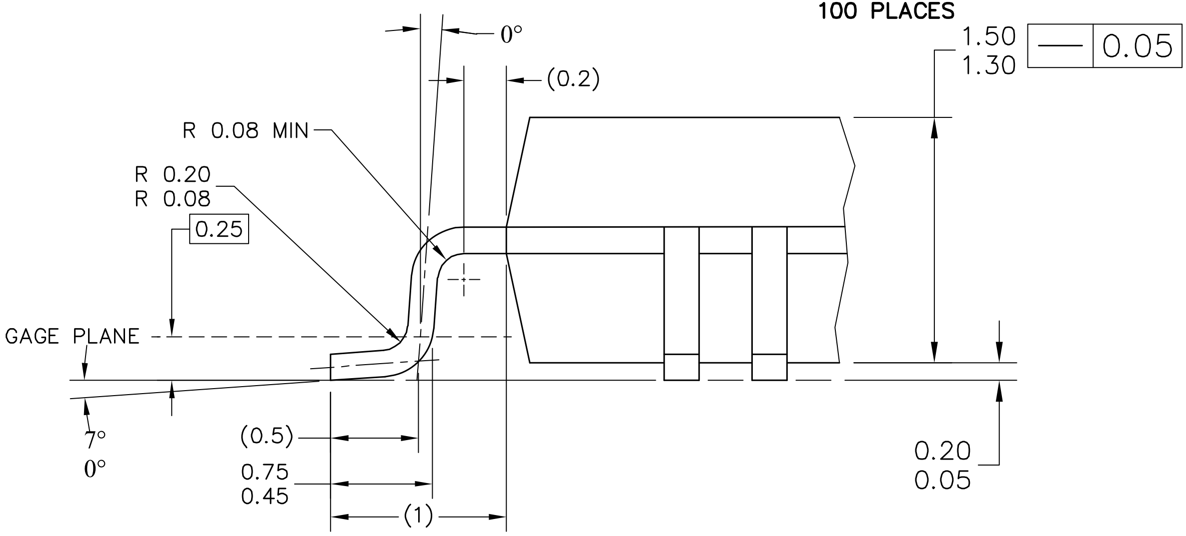
VIEW A



SECTION A–A

ROTATED 90° CW

100 PLACES



VIEW B

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TITLE: 100 LEAD LQFP 14 X 14, 0.5 PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23308W		REV: G
	CASE NUMBER: 983–03		07 APR 2005
	STANDARD: NON–JEDEC		