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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V2
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, SPI, UART/USART
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	56
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 8x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	81-LBGA
Supplier Device Package	81-MAPBGA (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf5213lcvm80j

- Version 2 ColdFire variable-length RISC processor core
  - Static operation
  - 32-bit address and data paths on-chip
  - Up to 80 MHz processor core frequency
  - Sixteen general-purpose, 32-bit data and address registers
  - Implements ColdFire ISA_A with extensions to support the user stack pointer register and four new instructions for improved bit processing (ISA_A+)
  - Multiply-Accumulate (MAC) unit with 32-bit accumulator to support 16×16 → 32 or 32×32 → 32 operations
  - Illegal instruction decode that allows for 68-Kbyte emulation support
- System debug support
  - Real-time trace for determining dynamic execution path
  - Background debug mode (BDM) for in-circuit debugging (DEBUG_B+)
  - Real-time debug support, with six hardware breakpoints (4 PC, 1 address and 1 data) configurable into a 1- or 2-level trigger
- On-chip memories
  - 32-Kbyte dual-ported SRAM on CPU internal bus, supporting core and DMA access with standby power supply support
  - 256 Kbytes of interleaved flash memory supporting 2-1-1-1 accesses
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Rapid response to interrupts from the low-power sleep mode (wake-up feature)
  - Clock enable/disable for each peripheral when not used
- FlexCAN 2.0B module
  - Based on and includes all existing features of the Freescale TouCAN module
  - Full implementation of the CAN protocol specification version 2.0B
    - Standard data and remote frames (up to 109 bits long)
    - Extended data and remote frames (up to 127 bits long)
    - Zero to eight bytes data length
    - Programmable bit rate up to 1 Mbit/sec
  - Flexible message buffers (MBs), totalling up to 16 message buffers of 0–8 byte data length each, configurable as Rx or Tx, all supporting standard and extended messages
  - Unused MB space can be used as general purpose RAM space
  - Listen-only mode capability
  - Content-related addressing
  - No read/write semaphores
  - Three programmable mask registers: global for MBs 0-13, special for MB14, and special for MB15
  - Programmable transmit-first scheme: lowest ID or lowest buffer number
  - Time stamp based on 16-bit free-running timer
  - Global network time, synchronized by a specific message
  - Maskable interrupts
- Three universal asynchronous/synchronous receiver transmitters (UARTs)
  - 16-bit divider for clock generation
  - Interrupt control logic with maskable interrupts
  - DMA support
  - Data formats can be 5, 6, 7 or 8 bits with even, odd, or no parity
  - Up to two stop bits in 1/16 increments

  - System configuration during reset
  - Selects one of six clock modes
  - Configures output pad drive strength
  - Unique part identification number and part revision number
- General purpose I/O interface
  - Up to 56 bits of general purpose I/O
  - Bit manipulation supported via set/clear functions
  - Programmable drive strengths
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing

1.1.2 V2 Core Overview

The version 2 ColdFire processor core is comprised of two separate pipelines decoupled by an instruction buffer. The two-stage instruction fetch pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the operand execution pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire instruction set architecture revision A+ with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the MCF5213 core includes the multiply-accumulate (MAC) unit for improved signal processing capabilities. The MAC implements a three-stage arithmetic pipeline, optimized for 16×16 bit operations, with support for one 32-bit accumulator. Supported operands include 16- and 32-bit signed and unsigned integers, signed fractional operands, and a complete set of instructions to process these data types. The MAC provides support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

1.1.3 Integrated Debug Module

The ColdFire processor core debug interface is provided to support system debugging with low-cost debug and emulator development tools. Through a standard debug interface, access to debug information and real-time tracing capability is provided on 100-lead packages. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators.

The on-chip breakpoint resources include a total of nine programmable 32-bit registers: an address and an address mask register, a data and a data mask register, four PC registers, and one PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single- or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception. The MCF5213 implements revision B+ of the ColdFire Debug Architecture.

The MCF5213's interrupt servicing options during emulator mode allow real-time critical interrupt service routines to be serviced while processing a debug interrupt event. This ensures the system continues to operate even during debugging.

To support program trace, the V2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate. The MCF5213 includes a new debug signal, ALLPST. This signal is the logical AND of the processor status (PST[3:0]) signals and is useful for detecting when the processor is in a halted state (PST[3:0] = 1111).

The full debug/trace interface is available only on the 100-pin packages. However, every product features the dedicated debug serial communication channel (DSI, DSO, DSCLK) and the ALLPST signal.

Figure 2 shows the pinout configuration for the 100 LQFP.

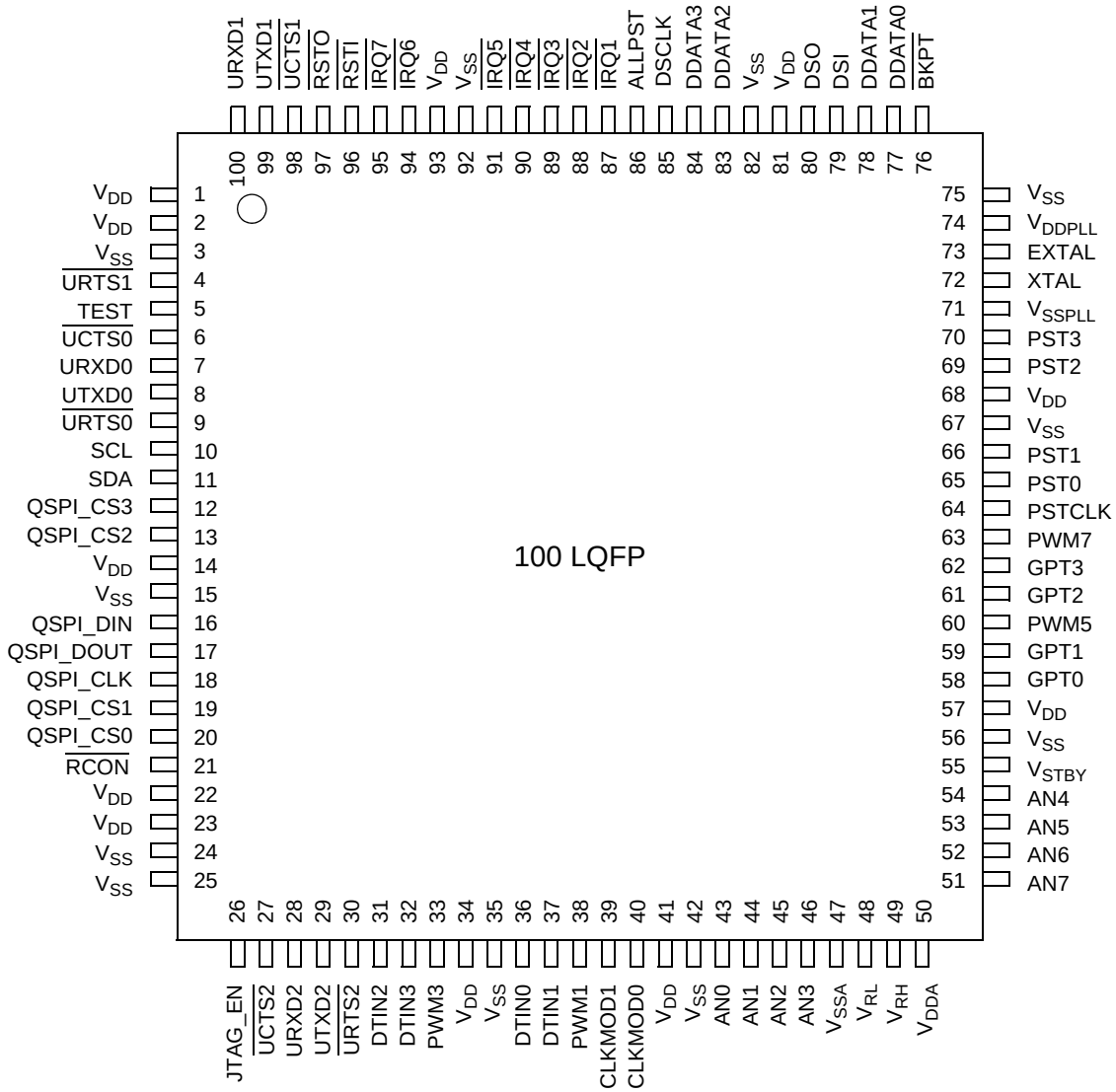


Figure 2. 100 LQFP Pin Assignments

Table 3. Pin Functions by Primary and Alternate Purpose

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
ADC	AN7	—	—	GPIO	Low	FAST	—	51	H9	33
	AN6	—	—	GPIO	Low	FAST	—	52	G9	34
	AN5	—	—	GPIO	Low	FAST	—	53	G8	35
	AN4	—	—	GPIO	Low	FAST	—	54	F9	36
	AN3	—	—	GPIO	Low	FAST	—	46	G7	28
	AN2	—	—	GPIO	Low	FAST	—	45	G6	27
	AN1	—	—	GPIO	Low	FAST	—	44	H6	26
	AN0	—	—	GPIO	Low	FAST	—	43	J6	25
	SYNCA[3]	—	—	—	N/A	N/A	—	—	—	—
	SYNCB[3]	—	—	—	N/A	N/A	—	—	—	—
	VDDA	—	—	—	N/A	N/A	—	50	H8	32
	VSSA	—	—	—	N/A	N/A	—	47	H7, J9	29
	VRH	—	—	—	N/A	N/A	—	49	J8	31
	VRL	—	—	—	N/A	N/A	—	48	J7	30
Clock Generation	EXTAL	—	—	—	N/A	N/A	—	73	B9	47
	XTAL	—	—	—	N/A	N/A	—	72	C9	46
	VDDPLL	—	—	—	N/A	N/A	—	74	B8	48
	VSSPLL	—	—	—	N/A	N/A	—	71	C8	45
Debug Data	ALLPST	—	—	—	High	FAST	—	86	A6	55
	DDATA[3:0]	—	—	GPIO	High	FAST	—	84,83,78,77	—	—
	PST[3:0]	—	—	GPIO	High	FAST	—	70,69,66,65	—	—
I^2C	SCL	CANTX[4]	UTXD2	GPIO	PDSR[0]	PSRR[0]	pull-up[5]	10	E1	8
	SDA	CANRX[3]	URXD2	GPIO	PDSR[0]	PSRR[0]	pull-up[5]	11	E2	9

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
Interrupts	$\overline{\text{IRQ7}}$	—	—	GPIO	Low	FAST	pull-up	95	C4	58
	$\overline{\text{IRQ6}}$	—	—	GPIO	Low	FAST	pull-up	94	B4	—
	$\overline{\text{IRQ5}}$	—	—	GPIO	Low	FAST	pull-up	91	A4	—
	$\overline{\text{IRQ4}}$	—	—	GPIO	Low	FAST	pull-up	90	C5	57
	$\overline{\text{IRQ3}}$	—	—	GPIO	Low	FAST	pull-up	89	A5	—
	$\overline{\text{IRQ2}}$	—	—	GPIO	Low	FAST	pull-up	88	B5	—
	$\overline{\text{IRQ1}}$	SYNCA	PWM1	GPIO	High	FAST	pull-up[5]	87	C6	56
JTAG/BDM	JTAG_EN	—	—	—	N/A	N/A	pull-down	26	J2	17
	TCLK/ PSTCLK	CLKOUT	—	—	High	FAST	pull-up[6]	64	C7	44
	TDI/DSI	—	—	—	N/A	N/A	pull-up[6]	79	B7	50
	TDO/DSO	—	—	—	High	FAST	—	80	A7	51
	TMS /$\overline{\text{BKPT}}$	—	—	—	N/A	N/A	pull-up[6]	76	A8	49
	$\overline{\text{TRST}}$ /DSCLK	—	—	—	N/A	N/A	pull-up[6]	85	B6	54
Mode Selection[7]	CLKMOD0	—	—	—	N/A	N/A	pull-down[7]	40	G5	24
	CLKMOD1	—	—	—	N/A	N/A	pull-down[7]	39	H5	—
	$\overline{\text{RCON}}$/ EZPCS	—	—	—	N/A	N/A	pull-up	21	G3	16
PWM	PWM7	—	—	GPIO	PDSR[31]	PSRR[31]	—	63	D7	—
	PWM5	—	—	GPIO	PDSR[30]	PSRR[30]	—	60	E8	—
	PWM3	—	—	GPIO	PDSR[29]	PSRR[29]	—	33	J4	—
	PWM1	—	—	GPIO	PDSR[28]	PSRR[28]	—	38	J5	—

Table 3. Pin Functions by Primary and Alternate Purpose (continued)

Pin Group	Primary Function	Secondary Function	Tertiary Function	Quaternary Function	Drive Strength / Control[1]	Slew Rate / Control[1]	Pull-up / Pull-down[2]	Pin on 100 LQFP	Pin on 81 MAPBGA	Pin on 64 LQFP/QFN
UART 1	$\overline{\text{UCTS1}}$	SYNCA	URXD2	GPIO	PDSR[15]	PSRR[15]	—	98	C3	61
	$\overline{\text{URTS1}}$	SYNCB	UTXD2	GPIO	PDSR[14]	PSRR[14]	—	4	B1	2
	URXD1	—	—	GPIO	PDSR[13]	PSRR[13]	—	100	B2	63
	UTXD1	—	—	GPIO	PDSR[12]	PSRR[12]	—	99	A2	62
UART 2	$\overline{\text{UCTS2}}$	—	—	GPIO	PDSR[27]	PSRR[27]	—	27	—	—
	$\overline{\text{URTS2}}$	—	—	GPIO	PDSR[26]	PSRR[26]	—	30	—	—
	URXD2	—	—	GPIO	PDSR[25]	PSRR[25]	—	28	—	—
	UTXD2	—	—	GPIO	PDSR[24]	PSRR[24]	—	29	—	—
FlexCAN	CANRX[4,11]				N/A	N/A	—	—	—	—
	CANTX[4,11]				N/A	N/A	—	—	—	—
VSTBY	VSTBY	—	—	—	N/A	N/A	—	55	F8	37
VDD	VDD	—	—	—	N/A	N/A	—	1,2,14,22, 23,34,41, 57,68,81,93	D5,E3–E7, F5	1,10,20,39,52
VSS	VSS	—	—	—	N/A	N/A	—	3,15,24,25,35,42,56, 67,75,82,92	A1,A9,D4,D6,F4,F6,J1	11,21,38, 53,64

1 The PDSR and PSSR registers are described in the General Purpose I/O chapter. All programmable signals default to 2 mA drive and FAST slew rate in normal (single-chip) mode.
2 All signals have a pull-up in GPIO mode.
3 These signals are multiplexed on other pins.
4 The multiplexed CANTX and CANRX signals are not available on the MCF5211 or MCF5212.
5 For primary and GPIO functions only.
6 Only when JTAG mode is enabled.
7 CLKMOD0 and CLKMOD1 have internal pull-down resistors; however, the use of external resistors is very strongly recommended.
8 For secondary and GPIO functions only.
9 $\overline{\text{RSTI}}$ has an internal pull-up resistor; however, the use of an external resistor is very strongly recommended.
10 For GPIO function. Primary Function has pull-up control within the GPT module.
11 CANTX and CANRX are secondary functions only.

1.2 Reset Signals

Table 4 describes signals used to reset the chip or as a reset indication.

Table 4. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RSTI}}$	Primary reset input to the device. Asserting $\overline{\text{RSTI}}$ for at least 8 CPU clock cycles immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTO}}$	Driven low for 1024 CPU clocks after the reset source has deasserted.	O

1.3 PLL and Clock Signals

Table 5 describes signals used to support the on-chip clock generation circuitry.

Table 5. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Crystal oscillator or external clock input except when the on-chip relaxation oscillator is used.	I
Crystal	XTAL	Crystal oscillator output except when CLKMOD1=1, then sampled as part of the clock mode selection mechanism.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

1.4 Mode Selection

Table 6 describes signals used in mode selection; Table 7 describes the particular clocking modes.

Table 6. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Selects the clock boot mode.	I
Reset Configuration	RCON	The Serial Flash Programming mode is entered by asserting the $\overline{\text{RCON}}$ pin (with the TEST pin negated) as the chip comes out of reset. During this mode, the EzPort has access to the flash memory which can be programmed from an external device.	
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I

Table 7. Clocking Modes

CLKMOD[1:0]	XTAL	Configure the clock mode.
00	0	PLL disabled, clock driven by external oscillator
00	1	PLL disabled, clock driven by on-chip oscillator
01	N/A	PLL disabled, clock driven by crystal
10	0	PLL in normal mode, clock driven by external oscillator
10	1	PLL in normal mode, clock driven by on-chip oscillator
11	N/A	PLL in normal mode, clock driven by crystal

1.5 External Interrupt Signals

Table 8 describes the external interrupt signals.

Table 8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[7:1]	External interrupt sources.	I

1.6 Queued Serial Peripheral Interface (QSPI)

Table 9 describes the QSPI signals.

Table 9. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Synchronous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable.	O
Synchronous Peripheral Chip Selects	QSPI_CS[3:0]	QSPI peripheral chip select; can be programmed to be active high or low.	O

1.7 I^2C I/O Signals

Table 10 describes the I^2C serial interface module signals.

Table 10. I^2C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	SCL	Open-drain clock signal for the for the I^2C interface. When the bus is In master mode, this clock is driven by the I^2C module; when the bus is in slave mode, this clock becomes the clock input.	I/O
Serial Data	SDA	Open-drain signal that serves as the data input/output for the I^2C interface.	I/O

Table 21. Typical Active Current Consumption Specifications

Characteristic	Symbol	Typical[1] Active (SRAM)	Typical[1] Active (Flash)	Peak[2]	Unit
1 MHz core & I/O	I_{DD}	—	3.48	—	mA
8 MHz core & I/O		7.28	13.37	19.02	
16 MHz core & I/O		12.08	25.08	35.66	
64 MHz core & I/O		40.14	54.62	85.01	
80 MHz core & I/O		49.2	64.09	100.03	
RAM standby supply current • Normal operation: $V_{DD} > V_{STBY} - 0.3$ V • Transient condition: $V_{STBY} - 0.3$ V > $V_{DD} > V_{SS} + 0.5$ V • Standby operation: $V_{DD} < V_{SS} + 0.5$ V	I_{STBY}	N/A[3] N/A[3] N/A[3]		N/A[3] N/A[3] N/A[3]	µA mA µA
Analog supply current • Normal operation • Low-power stop	I_{DDA}	— —	— —	16 50	mA µA

1 Tested at room temperature with CPU polling a status register. All clocks were off except the UART and CFM (when running from flash memory).

2 Peak current measured with all modules active, and default drive strength with matching load.

3 Due to the errata “Non-functional RAM Standby Supply” in the *MCF5213 Device Errata*, V_{STBY} should be connected directly to V_{DD} and cannot be used for RAM standby operation.

2.3 Thermal Characteristics

Table 22 lists thermal resistance values.

Table 22. Thermal Characteristics

	Characteristic		Symbol	Value	Unit
100 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	53[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	39[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	42[1,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	33[1,3]	°C/W
	Junction to board	—	θ_{JB}	25[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

Table 22. Thermal Characteristics (continued)

	Characteristic		Symbol	Value	Unit
81 MAPBGA	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	61[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	35[2,3]	°C/W
	Junction to ambient, (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50[2,3]	°C/W
	Junction to ambient, (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	31[2,3]	°C/W
	Junction to board	—	θ_{JB}	20[4]	°C/W
	Junction to case	—	θ_{JC}	12[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 LQFP	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	62[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	43[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	50[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	36[1,3]	°C/W
	Junction to board	—	θ_{JB}	26[4]	°C/W
	Junction to case	—	θ_{JC}	9[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	2[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C
64 QFN	Junction to ambient, natural convection	Single layer board (1s)	θ_{JA}	68[1,2]	°C/W
	Junction to ambient, natural convection	Four layer board (2s2p)	θ_{JA}	24[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Single layer board (1s)	θ_{JMA}	55[1,3]	°C/W
	Junction to ambient (@200 ft/min)	Four layer board (2s2p)	θ_{JMA}	19[1,3]	°C/W
	Junction to board	—	θ_{JB}	8[4]	°C/W
	Junction to case (bottom)	—	θ_{JC}	0.6[5]	°C/W
	Junction to top of package	Natural convection	Ψ_{jt}	3[6]	°C/W
	Maximum operating junction temperature	—	T_j	105	°C

1 θ_{JA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Freescale recommends the use of θ_{JA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.

2 Per JEDEC JESD51-2 with the single-layer board (JESD51-3) horizontal.

3 Per JEDEC JESD51-6 with the board JESD51-7) horizontal.

4 Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

5 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

6 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = ambient temperature, °C

Θ_{JA} = package thermal resistance, junction-to-ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = chip internal power, $I_{DD} \times V_{DD}$, watts

$P_{I/O}$ = power dissipation on input and output pins — user determined, watts

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

2.4 Flash Memory Characteristics

The flash memory characteristics are shown in Table 23 and Table 24.

Table 23. SGFM Flash Program and Erase Characteristics

(V_{DDF} = 2.7 to 3.6 V)

Parameter	Symbol	Min	Typ	Max	Unit
System clock (read only)	$f_{sys(R)}$	0	—	66.67 or 80[1]	MHz
System clock (program/erase)[2]	$f_{sys(P/E)}$	0.15	—	66.67 or 80[1]	MHz

1 Depending on packaging; see Table 2.

2 Refer to the flash memory section for more information

Table 24. SGFM Flash Module Life Characteristics

(V_{DDF} = 2.7 to 3.6 V)

Parameter	Symbol	Value	Unit
Maximum number of guaranteed program/erase cycles[1] before failure	P/E	10,000[2]	Cycles
Data retention at average operating temperature of 85°C	Retention	10	Years

1 A program/erase cycle is defined as switching the bits from 1 → 0 → 1.

2 Reprogramming of a flash memory array block prior to erase is not required.

Table 26. DC Electrical Specifications (continued)[1]

Characteristic	Symbol	Min	Max	Unit
Output high voltage (high drive) I_{OH} = -5 mA	V_{OH}	V_{DD} – 0.5	—	V
Output low voltage (high drive) I_{OL} = 5 mA	V_{OL}	—	0.5	V
Output high voltage (low drive) I_{OH} = -2 mA	V_{OH}	V_{DD} - 0.5	—	V
Output low voltage (low drive) I_{OL} = 2 mA	V_{OL}	—	0.5	V
Weak internal pull Up device current, tested at V_{IL} Max.[2]	I_{APU}	–10	–130	µA
Input Capacitance [3] • All input-only pins • All input/output (three-state) pins	C_{in}	 — —	 7 7	pF

1 Refer to Table 27 for additional PLL specifications.

2 Refer to Table 3 for pins having internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.

2.7 Clock Source Electrical Specifications

Table 27. PLL Electrical Specifications

(V_{DD} and V_{DDPLL} = 2.7 to 3.6 V, V_{SS} = V_{SSPLL} = 0 V)

Characteristic	Symbol	Min	Max	Unit
PLL reference frequency range • Crystal reference • External reference	 $f_{ref\_crystal}$ f_{ref_ext}	 2 2	 10.0 10.0	MHz
System frequency [1] • External clock mode • On-chip PLL frequency	f_{sys}	 0 f_{ref} / 32	 66.67 or 80[2] 66.67 or 80[2]	MHz
Loss of reference frequency [3, 5]	f_{LOR}	100	1000	kHz
Self clocked mode frequency [4]	f_{SCM}	1	5	MHz
Crystal start-up time [5, 6]	t_{cst}	—	10	ms
EXTAL input high voltage • External reference	V_{IHEXT}	 2.0	 V_{DD}	V
EXTAL input low voltage • External reference	V_{ILEXT}	 V_{SS}	 0.8	V
PLL lock time[4,7]	t_{lpll}	—	500	µs
Duty cycle of reference [4]	t_{dc}	40	60	% f_{ref}

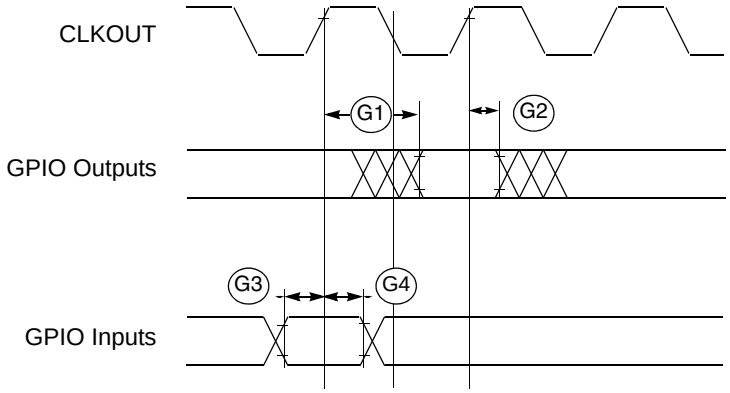


Figure 5. GPIO Timing

2.9 Reset Timing

Table 29. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RSTI}}$ input valid to CLKOUT High	t_{RVCH}	9	—	ns
R2	CLKOUT High to $\overline{\text{RSTI}}$ Input invalid	t_{CHRI}	1.5	—	ns
R3	$\overline{\text{RSTI}}$ input valid time [2]	t_{RIVT}	5	—	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTO}}$ Valid	t_{CHROV}	—	10	ns

[1] All AC timing is shown with respect to 50% V_{DD} levels unless otherwise noted.

[2] During low power STOP, the synchronizers for the $\overline{\text{RSTI}}$ input are bypassed and $\overline{\text{RSTI}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RSTI}}$ must be held a minimum of 100 ns.

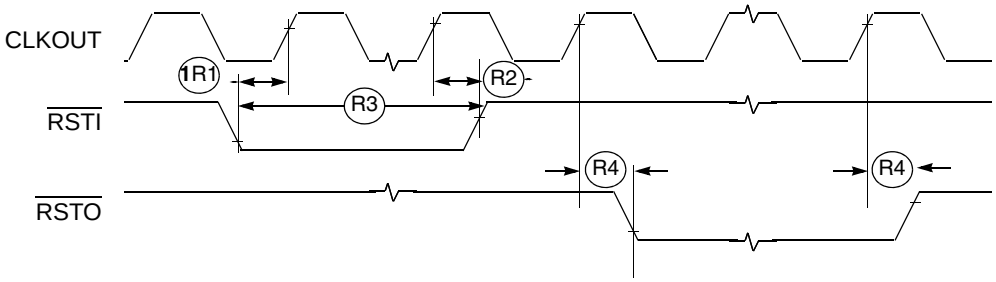
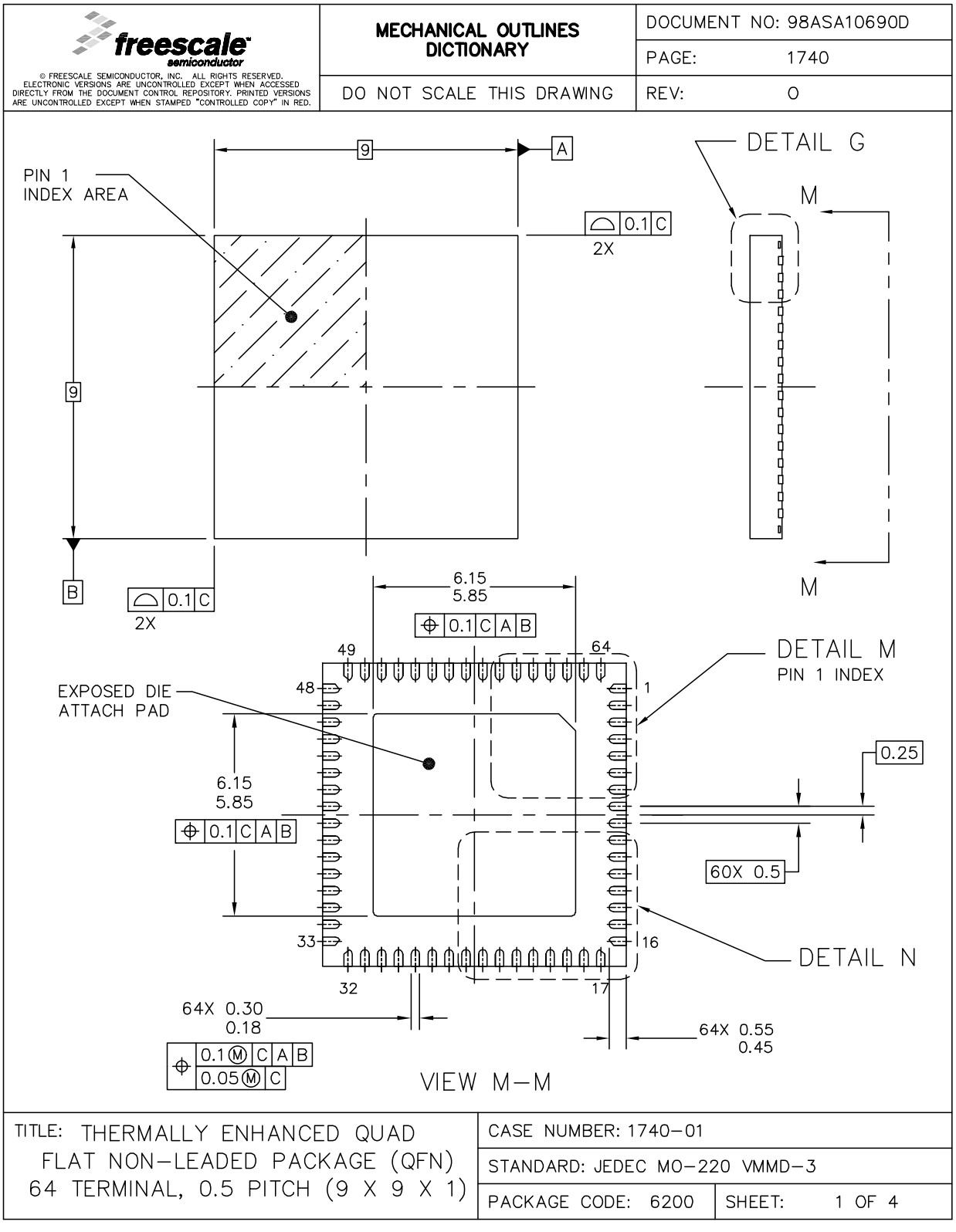


Figure 6. $\overline{\text{RSTI}}$ and Configuration Override Timing

3.2 64 QFN Package



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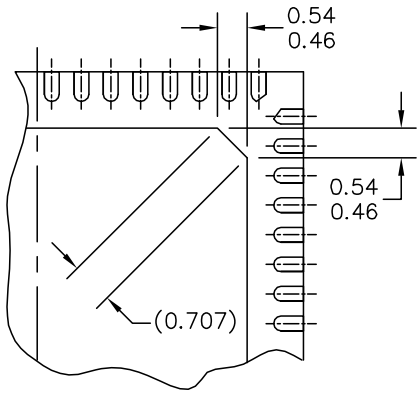
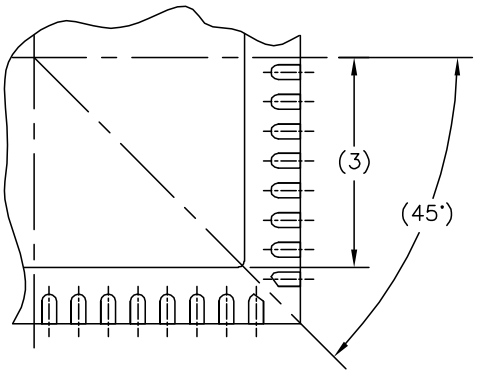
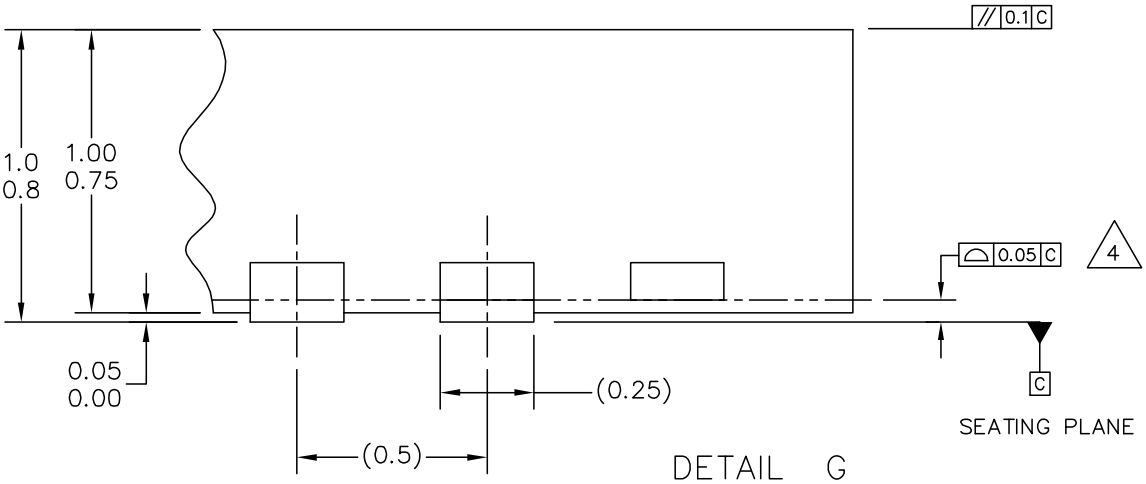


DETAIL M
PREFERRED PIN1 BACKSIDE IDENTIFIER



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL G
VIEW ROTATED 90° CW

TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 64 TERMINAL, 0.5 PITCH (9 X 9 X 1)	CASE NUMBER: 1740-01	
	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 2 OF 4

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REVISION HISTORY

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O	ERIC TRIPLETT	RELEASED FOR PRODUCTION	TAYLOR LIU	27JUL2005

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	STANDARD: JEDEC MO-220 VMMD-3	
	PACKAGE CODE: 6200	SHEET: 4 OF 4

NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

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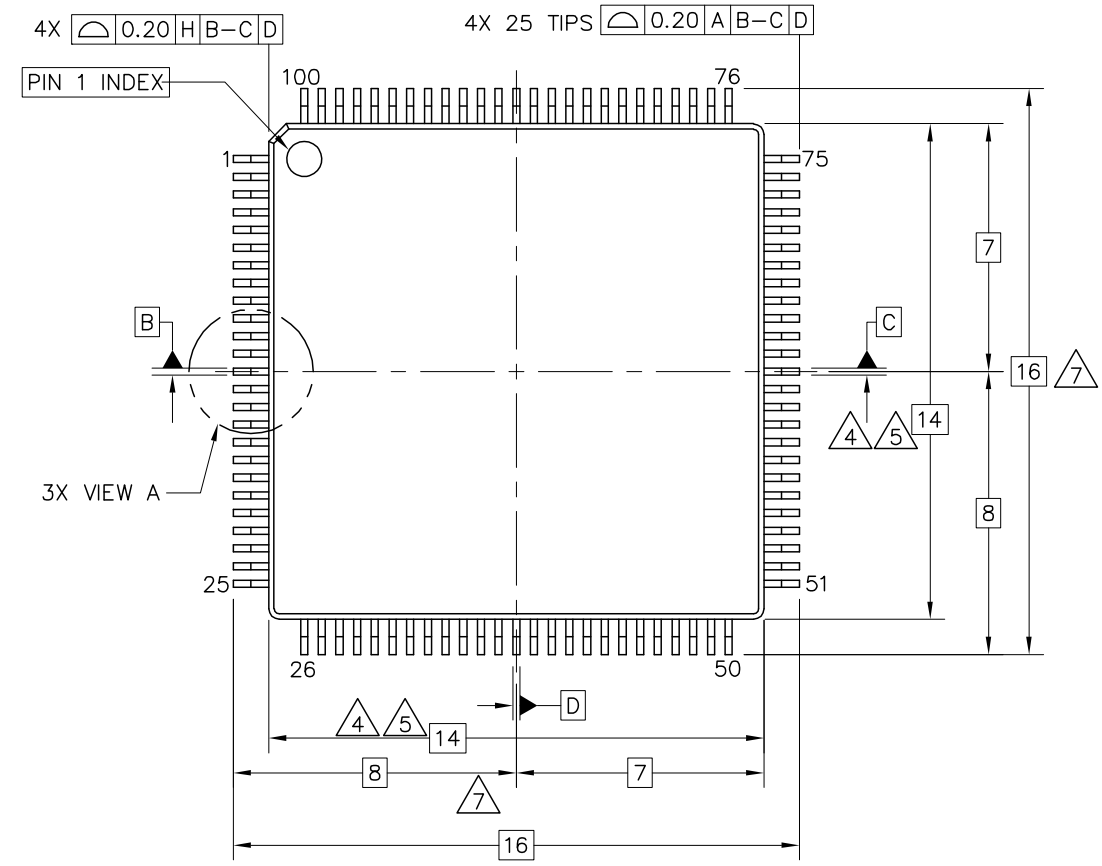
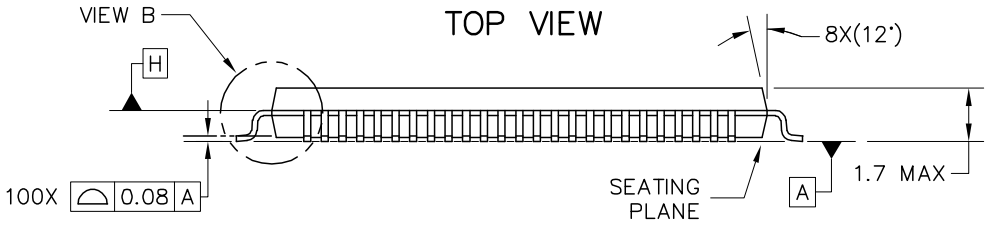
	STANDARD: NON–JEDEC	

3.4 100-pin LQFP Package





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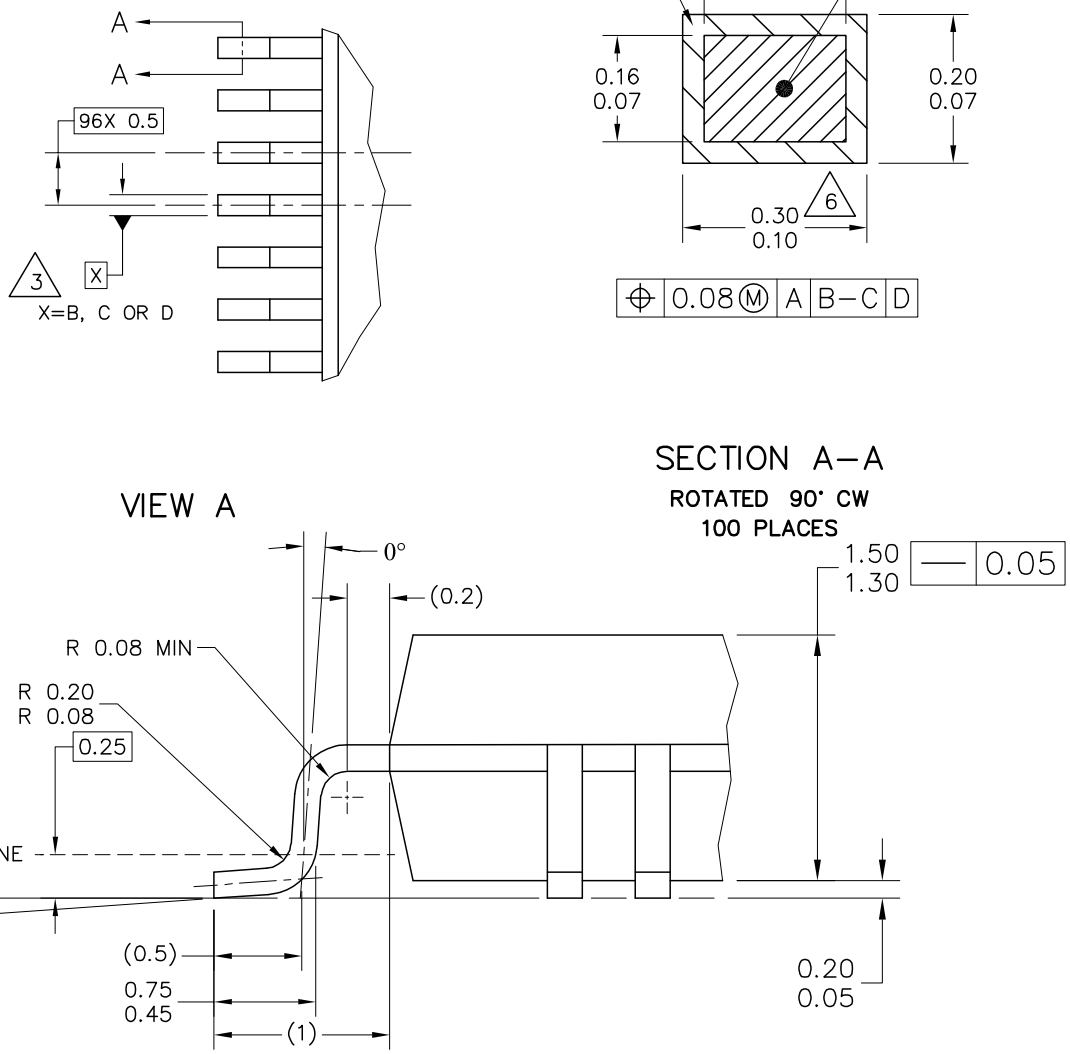
	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	



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	CASE NUMBER: 983–03	07 APR 2005
	STANDARD: NON–JEDEC	

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