Renesas Electronics America Inc - R5F21346CNFP#U0 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	43
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	2.5K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 12x10b; D/A 2x8b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21346cnfp-u0

Table 1.5 Pin Name Information by Pin Number (2)

Pin Number	Control Pin	Port	I/O Pin Functions for Peripheral Modules					
			Interrupt	Timer	Serial Interface	SSU	I^2C bus	A/D Converter, D/A Converter, Comparator B
36		P1_0	$\overline{KI0}$	(TRCIOD)				AN8
37		P0_7		(TRCIOC)				AN0/DA1
38		P0_6		(TRCIOD)				AN1/DA0
39		P0_5		(TRCIOB)				AN2
40		P0_4		TREO (/TRCIOB)				AN3
41		P0_3		(TRCIOB)	(CLK1)			AN4
42		P0_2		(TRCIOA/ TRCTRG)	(RXD1)			AN5
43		P0_1		(TRCIOA/ TRCTRG)	(TXD1)			AN6
44		P0_0		(TRCIOA/ TRCTRG)				AN7
45		P6_4			(RXD1)			
46		P6_3			(TXD1)			
47		P6_2			(CLK1)			
48		P6_1						

Note:
1. Can be assigned to the pin in parentheses by a program.

Table 1.7 Pin Functions (2)

Item	Pin Name	I/O Type	Description
Reference voltage input	VREF	I	Reference voltage input pin to A/D converter and D/A converter
A/D converter	AN0 to AN11	I	Analog input pins to A/D converter
	$\overline{\text{ADTRG}}$	I	A/D external trigger input pin
D/A converter	DA0, DA1	O	D/A converter output pins
Comparator B	IVCMP1, IVCMP3	I	Comparator B analog voltage input pins
	IVREF1, IVREF3	I	Comparator B reference voltage input pins
I/O port	P0_0 to P0_7, P1_0 to P1_7, P2_0 to P2_7, P3_0, P3_1, P3_3 to P3_5, P3_7, P4_3 to P4_7, P6_0 to P6_7	I/O	CMOS I/O ports. Each port has an I/O select direction register, allowing each pin in the port to be directed for input or output individually. Any port set to input can be set to use a pull-up resistor or not by a program. All ports can be used as LED drive ports.
Input port	P4_2	I	Input-only port

I: Input O: Output I/O: Input and output

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 to R3. R0 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R1H and R1L are analogous to R0H and R0L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). R3R1 is analogous to R2R0.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 is analogous to A0. A1 can be combined with A0 and as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the starting address of an interrupt vector table.

2.5 Program Counter (PC)

PC is 20 bits wide and indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of FLG is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register indicating the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated by the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. Set it to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0; otherwise to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value; otherwise to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is set to 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow; otherwise to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts.
Interrupts are disabled when the I flag is set to 0, and are enabled when the I flag is set to 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to 0; USP is selected when the U flag is set to 1.
The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns processor interrupt priority levels from level 0 to level 7.
If a requested interrupt has higher priority than IPL, the interrupt is enabled.

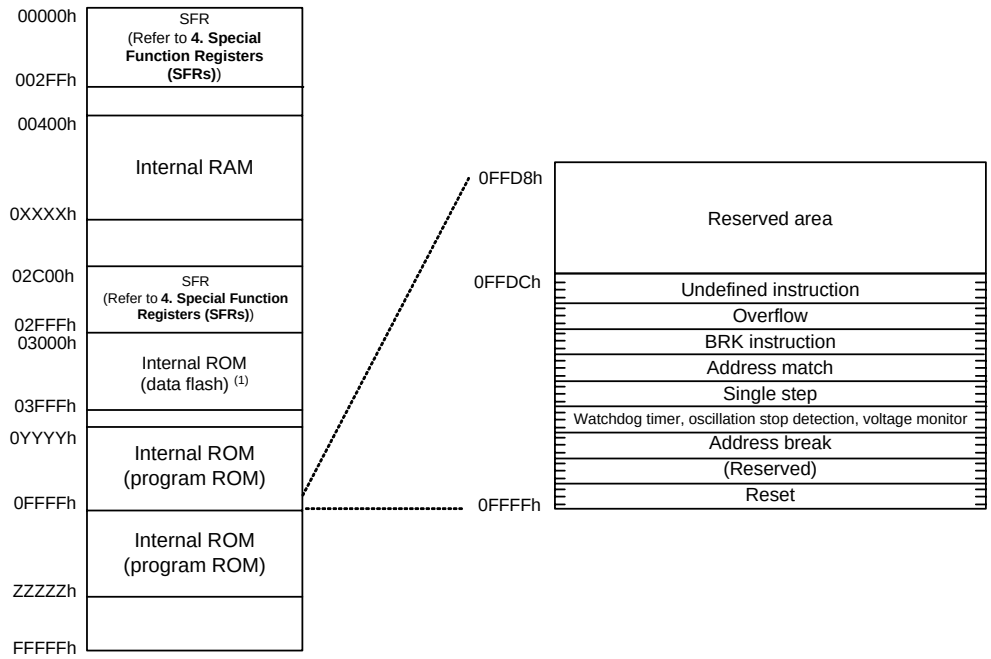
2.8.10 Reserved Bit

If necessary, set to 0. When read, the content is undefined.

3. Memory

3.1 R8C/34C Group

Figure 3.1 is a Memory Map of R8C/34C Group. The R8C/34C Group has a 1-Mbyte address space from addresses 00000h to FFFFFh. The internal ROM (program ROM) is allocated lower addresses, beginning with address 0FFFFh. For example, a 32-Kbyte internal ROM area is allocated addresses 08000h to 0FFFFh.
The fixed interrupt vector table is allocated addresses 0FFDCh to 0FFFFh. The starting address of each interrupt routine is stored here.
The internal ROM (data flash) is allocated addresses 03000h to 03FFFh.
The internal RAM is allocated higher addresses, beginning with address 00400h. For example, a 2.5-Kbyte internal RAM area is allocated addresses 00400h to 00DFFh. The internal RAM is used not only for data storage but also as a stack area when a subroutine is called or when an interrupt request is acknowledged.
Special function registers (SFRs) are allocated addresses 00000h to 002FFh and 02C00h to 02FFFh. Peripheral function control registers are allocated here. All unallocated spaces within the SFRs are reserved and cannot be accessed by users.



Notes:
1. Data flash indicates block A (1 Kbyte), block B (1 Kbyte), block C (1 Kbyte), and block D (1 Kbyte).
2. The blank areas are reserved and cannot be accessed by users.

Part Number	Internal ROM			Internal RAM	
	Size	Address 0YYYYh	Address ZZZZZh	Size	Address 0XXXXh
R5F21344CNFP, R5F21344CDFP	16 Kbytes	0C000h	–	1.5 Kbytes	009FFh
R5F21345CNFP, R5F21345CDFP	24 Kbytes	0A000h	–	2 Kbytes	00BFFh
R5F21346CNFP, R5F21346CDFP	32 Kbytes	08000h	–	2.5 Kbytes	00DFFh

Figure 3.1 Memory Map of R8C/34C Group

Table 4.7 SFR Information (7) (1)

Address	Register	Symbol	After Reset
0180h	Timer RA Pin Select Register	TRASR	00h
0181h	Timer RB/RC Pin Select Register	TRBRCSR	00h
0182h	Timer RC Pin Select Register 0	TRCPSR0	00h
0183h	Timer RC Pin Select Register 1	TRCPSR1	00h
0184h	Timer RD Pin Select Register 0	TRDPSR0	00h
0185h	Timer RD Pin Select Register 1	TRDPSR1	00h
0186h	Timer Pin Select Register	TIMSR	00h
0187h			
0188h	UART0 Pin Select Register	U0SR	00h
0189h	UART1 Pin Select Register	U1SR	00h
018Ah	UART2 Pin Select Register 0	U2SR0	00h
018Bh	UART2 Pin Select Register 1	U2SR1	00h
018Ch	SSU/IIC Pin Select Register	SSUIICSR	00h
018Dh			
018Eh	INT Interrupt Input Pin Select Register	INTSR	00h
018Fh	I/O Function Pin Select Register	PINSR	00h
0190h			
0191h			
0192h			
0193h	SS Bit Counter Register	SSBR	11111000b
0194h	SS Transmit Data Register L / IIC bus Transmit Data Register (2)	SSTDR / ICDRT	FFh
0195h	SS Transmit Data Register H (2)	SSTDRH	FFh
0196h	SS Receive Data Register L / IIC bus Receive Data Register (2)	SSRDR / ICDRR	FFh
0197h	SS Receive Data Register H (2)	SSRDRH	FFh
0198h	SS Control Register H / IIC bus Control Register 1 (2)	SSCRH / ICCR1	00h
0199h	SS Control Register L / IIC bus Control Register 2 (2)	SSCRL / ICCR2	01111101b
019Ah	SS Mode Register / IIC bus Mode Register (2)	SSMR / ICMR	00010000b / 00011000b
019Bh	SS Enable Register / IIC bus Interrupt Enable Register (2)	SSER / ICIER	00h
019Ch	SS Status Register / IIC bus Status Register (2)	SSSR / ICSR	00h / 0000X000b
019Dh	SS Mode Register 2 / Slave Address Register (2)	SSMR2 / SAR	00h
019Eh			
019Fh			
01A0h			
01A1h			
01A2h			
01A3h			
01A4h			
01A5h			
01A6h			
01A7h			
01A8h			
01A9h			
01AAh			
01ABh			
01ACh			
01ADh			
01AEh			
01AFh			
01B0h			
01B1h			
01B2h	Flash Memory Status Register	FST	10000X00b
01B3h			
01B4h	Flash Memory Control Register 0	FMR0	00h
01B5h	Flash Memory Control Register 1	FMR1	00h
01B6h	Flash Memory Control Register 2	FMR2	00h
01B7h			
01B8h			
01B9h			
01BAh			
01BBh			
01BCh			
01BDh			
01BEh			
01BFh			

X: Undefined

Notes:

1. The blank areas are reserved and cannot be accessed by users.
2. Selectable by the IICSEL bit in the SSUIICSR register.

Table 4.11 SFR Information (11) (1)

Address	Register	Symbol	After Reset
2CB0h	DTC Control Data 14	DTCD14	XXh
2CB1h			XXh
2CB2h			XXh
2CB3h			XXh
2CB4h			XXh
2CB5h			XXh
2CB6h			XXh
2CB7h			XXh
2CB8h	DTC Control Data 15	DTCD15	XXh
2CB9h			XXh
2CBAh			XXh
2CBBh			XXh
2CBCh			XXh
2CBDh			XXh
2CBEh			XXh
2CBFh			XXh
2CC0h	DTC Control Data 16	DTCD16	XXh
2CC1h			XXh
2CC2h			XXh
2CC3h			XXh
2CC4h			XXh
2CC5h			XXh
2CC6h			XXh
2CC7h			XXh
2CC8h	DTC Control Data 17	DTCD17	XXh
2CC9h			XXh
2CCAh			XXh
2CCBh			XXh
2CCCh			XXh
2CCDh			XXh
2CCEh			XXh
2CCFh			XXh
2CD0h	DTC Control Data 18	DTCD18	XXh
2CD1h			XXh
2CD2h			XXh
2CD3h			XXh
2CD4h			XXh
2CD5h			XXh
2CD6h			XXh
2CD7h			XXh
2CD8h	DTC Control Data 19	DTCD19	XXh
2CD9h			XXh
2CDAh			XXh
2CDBh			XXh
2CDCh			XXh
2CDDh			XXh
2CDEh			XXh
2CDFh			XXh
2CE0h	DTC Control Data 20	DTCD20	XXh
2CE1h			XXh
2CE2h			XXh
2CE3h			XXh
2CE4h			XXh
2CE5h			XXh
2CE6h			XXh
2CE7h			XXh
2CE8h	DTC Control Data 21	DTCD21	XXh
2CE9h			XXh
2CEAh			XXh
2CEBh			XXh
2CECh			XXh
2CEDh			XXh
2CEEh			XXh
2CEFh			XXh

X: Undefined

Note:

1. The blank areas are reserved and cannot be accessed by users.

Table 4.12 SFR Information (12) (1)

Address	Register	Symbol	After Reset
2CF0h	DTC Control Data 22	DTCD22	XXh
2CF1h			XXh
2CF2h			XXh
2CF3h			XXh
2CF4h			XXh
2CF5h			XXh
2CF6h			XXh
2CF7h			XXh
2CF8h	DTC Control Data 23	DTCD23	XXh
2CF9h			XXh
2CFAh			XXh
2CFBh			XXh
2CFCh			XXh
2CFDh			XXh
2CFEh			XXh
2CFFh			XXh
2D00h			
:			
2FFFh			

X: Undefined
Note:
1. The blank areas are reserved and cannot be accessed by users.

Table 4.13 ID Code Areas and Option Function Select Area

Address	Area Name	Symbol	After Reset
:			
FFDBh	Option Function Select Register 2	OFS2	(Note 1)
:			
FFDFh	ID1		(Note 2)
:			
FFE3h	ID2		(Note 2)
:			
FFEBh	ID3		(Note 2)
:			
FFEFh	ID4		(Note 2)
:			
FFF3h	ID5		(Note 2)
:			
FFF7h	ID6		(Note 2)
:			
FFFBh	ID7		(Note 2)
:			
FFFFh	Option Function Select Register	OFS	(Note 1)

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the option function select area. If the block including the option function select area is erased, the option function select area is set to FFh.
When blank products are shipped, the option function select area is set to FFh. It is set to the written value after written by the user.
When factory-programming products are shipped, the value of the option function select area is the value programmed by the user.
2. The ID code areas are allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program.
Do not write additions to the ID code areas. If the block including the ID code areas is erased, the ID code areas are set to FFh.
When blank products are shipped, the ID code areas are set to FFh. They are set to the written value after written by the user.
When factory-programming products are shipped, the value of the ID code areas is the value programmed by the user.

Table 5.2 Recommended Operating Conditions

Symbol	Parameter				Conditions	Standard			Unit
						Min.	Typ.	Max.	
V_{CC}/AV_{CC}	Supply voltage					1.8	–	5.5	V
V_{SS}/AV_{SS}	Supply voltage					–	0	–	V
V_{IH}	Input “H” voltage	Other than CMOS input				0.8 V_{CC}	–	V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.5 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.55 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.65 V_{CC}	–	V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.65 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.7 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.8 V_{CC}	–	V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0.85 V_{CC}	–	V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0.85 V_{CC}	–	V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0.85 V_{CC}	–	V_{CC}	V
		External clock input (XOUT)				1.2	–	V_{CC}	V
V_{IL}	Input “L” voltage	Other than CMOS input				0	–	0.2 V_{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection : 0.35 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.2 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.2 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.5 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.4 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.3 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.2 V_{CC}	V
				Input level selection : 0.7 V_{CC}	4.0 V ≤ V_{CC} ≤ 5.5 V	0	–	0.55 V_{CC}	V
					2.7 V ≤ V_{CC} < 4.0 V	0	–	0.45 V_{CC}	V
					1.8 V ≤ V_{CC} < 2.7 V	0	–	0.35 V_{CC}	V
		External clock input (XOUT)				0	–	0.4	V
$I_{OH(sum)}$	Peak sum output “H” current	Sum of all pins $I_{OH(peak)}$				–	–	–160	mA
$I_{OH(sum)}$	Average sum output “H” current	Sum of all pins $I_{OH(avg)}$				–	–	–80	mA
$I_{OH(peak)}$	Peak output “H” current	Drive capacity Low				–	–	–10	mA
		Drive capacity High				–	–	–40	mA
$I_{OH(avg)}$	Average output “H” current	Drive capacity Low				–	–	–5	mA
		Drive capacity High				–	–	–20	mA
$I_{OL(sum)}$	Peak sum output “L” current	Sum of all pins $I_{OL(peak)}$				–	–	160	mA
$I_{OL(sum)}$	Average sum output “L” current	Sum of all pins $I_{OL(avg)}$				–	–	80	mA
$I_{OL(peak)}$	Peak output “L” current	Drive capacity Low				–	–	10	mA
		Drive capacity High				–	–	40	mA
$I_{OL(avg)}$	Average output “L” current	Drive capacity Low				–	–	5	mA
		Drive capacity High				–	–	20	mA
$f_{(XIN)}$	XIN clock input oscillation frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
$f_{(XCIN)}$	XCIN clock input oscillation frequency				1.8 V ≤ V_{CC} ≤ 5.5 V	–	32.768	50	kHz
fOCO40M	When used as the count source for timer RC or timer RD (3)				2.7 V ≤ V_{CC} ≤ 5.5 V	32	–	40	MHz
fOCO-F	fOCO-F frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
–	System clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz
$f_{(BCLK)}$	CPU clock frequency				2.7 V ≤ V_{CC} ≤ 5.5 V	–	–	20	MHz
					1.8 V ≤ V_{CC} < 2.7 V	–	–	5	MHz

Notes:
1. V_{CC} = 1.8 to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The average output current indicates the average value of current measured during 100 ms.
3. fOCO40M can be used as the count source for timer RC or timer RD in the range of V_{CC} = 2.7 V to 5.5V.

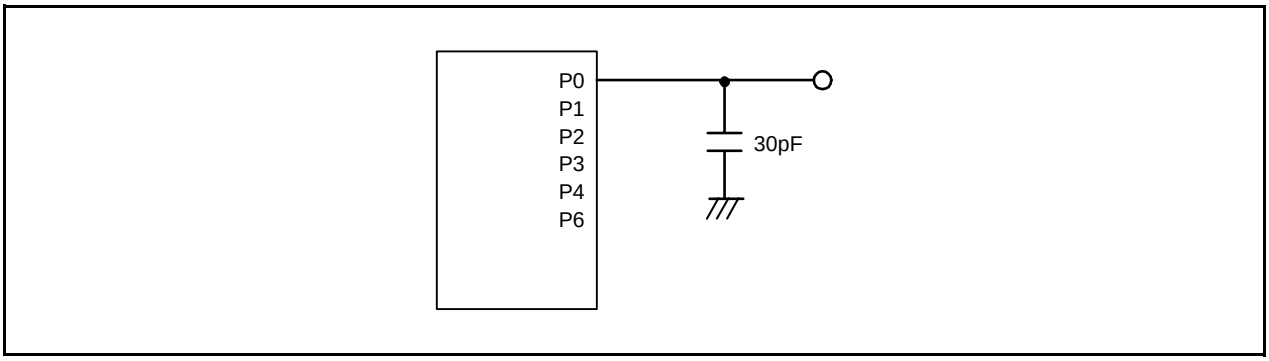


Figure 5.1 Ports P0 to P4, P6 Timing Measurement Circuit

Table 5.3 A/D Converter Characteristics

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
–	Resolution		V_{ref} = AV_{CC}		–	–	10	Bit
–	Absolute accuracy	10-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±3	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±5	LSB
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.3 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 3.0 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
			V_{ref} = AV_{CC} = 2.2 V	AN0 to AN7 input, AN8 to AN11 input	–	–	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	20	MHz
			3.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	16	MHz
			2.7 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	10	MHz
			2.2 V ≤ V_{ref} = AV_{CC} ≤ 5.5 V (2)		2	–	5	MHz
–	Tolerance level impedance				–	3	–	kΩ
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
		8-bit mode	V_{ref} = AV_{CC} = 5.0 V, ϕAD = 20 MHz		2.2	–	–	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	–	–	µs
I_{Vref}	V_{ref} current		V_{CC} = 5 V, XIN = f1 = ϕAD = 20 MHz		–	45	–	µA
V_{ref}	Reference voltage				2.2	–	AV_{CC}	V
V_{IA}	Analog input voltage (3)				0	–	V_{ref}	V
OCVREF	On-chip reference voltage		2 MHz ≤ ϕAD ≤ 4 MHz		1.19	1.34	1.49	V

Notes:
1. V_{CC}/AV_{CC} = V_{ref} = 2.2 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. The A/D conversion result will be undefined in wait mode, stop mode, when the flash memory stops, and in low-current-consumption mode. Do not perform A/D conversion in these states or transition to these states during A/D conversion.
3. When the analog input voltage is over the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 5.8 Voltage Detection 0 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (2)		1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (2)		2.15	2.35	2.50	V
	Voltage detection level Vdet0_2 (2)		2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (2)		3.55	3.80	4.05	V
–	Voltage detection 0 circuit response time (4)	At the falling of V_{CC} from 5 V to (Vdet0_0 – 0.1) V	–	6	150	µs
–	Voltage detection circuit self power consumption	VCA25 = 1, V_{CC} = 5.0 V	–	1.5	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VDSEL0 and VDSEL1 in the OFS register.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.
4. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.

Table 5.9 Voltage Detection 1 Circuit Electrical Characteristics

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det1}	Voltage detection level Vdet1_0 (2)	At the falling of Vcc	2.00	2.20	2.40	V
	Voltage detection level Vdet1_1 (2)	At the falling of Vcc	2.15	2.35	2.55	V
	Voltage detection level Vdet1_2 (2)	At the falling of Vcc	2.30	2.50	2.70	V
	Voltage detection level Vdet1_3 (2)	At the falling of Vcc	2.45	2.65	2.85	V
	Voltage detection level Vdet1_4 (2)	At the falling of Vcc	2.60	2.80	3.00	V
	Voltage detection level Vdet1_5 (2)	At the falling of Vcc	2.75	2.95	3.15	V
	Voltage detection level Vdet1_6 (2)	At the falling of Vcc	2.85	3.10	3.40	V
	Voltage detection level Vdet1_7 (2)	At the falling of Vcc	3.00	3.25	3.55	V
	Voltage detection level Vdet1_8 (2)	At the falling of Vcc	3.15	3.40	3.70	V
	Voltage detection level Vdet1_9 (2)	At the falling of Vcc	3.30	3.55	3.85	V
	Voltage detection level Vdet1_A (2)	At the falling of Vcc	3.45	3.70	4.00	V
	Voltage detection level Vdet1_B (2)	At the falling of Vcc	3.60	3.85	4.15	V
	Voltage detection level Vdet1_C (2)	At the falling of Vcc	3.75	4.00	4.30	V
	Voltage detection level Vdet1_D (2)	At the falling of Vcc	3.90	4.15	4.45	V
	Voltage detection level Vdet1_E (2)	At the falling of Vcc	4.05	4.30	4.60	V
	Voltage detection level Vdet1_F (2)	At the falling of Vcc	4.20	4.45	4.75	V
–	Hysteresis width at the rising of Vcc in voltage detection 1 circuit	Vdet1_0 to Vdet1_5 selected	–	0.07	–	V
		Vdet1_6 to Vdet1_F selected	–	0.10	–	V
–	Voltage detection 1 circuit response time (3)	At the falling of V_{CC} from 5 V to (Vdet1_0 – 0.1) V	–	60	150	µs
–	Voltage detection circuit self power consumption	VCA26 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (4)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Select the voltage detection level with bits VD1S0 to VD1S3 in the VD1LS register.
3. Time until the voltage monitor 1 interrupt request is generated after the voltage passes V_{det1}.
4. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA26 bit in the VCA2 register to 0.

Table 5.10 Voltage Detection 2 Circuit Electrical Characteristics

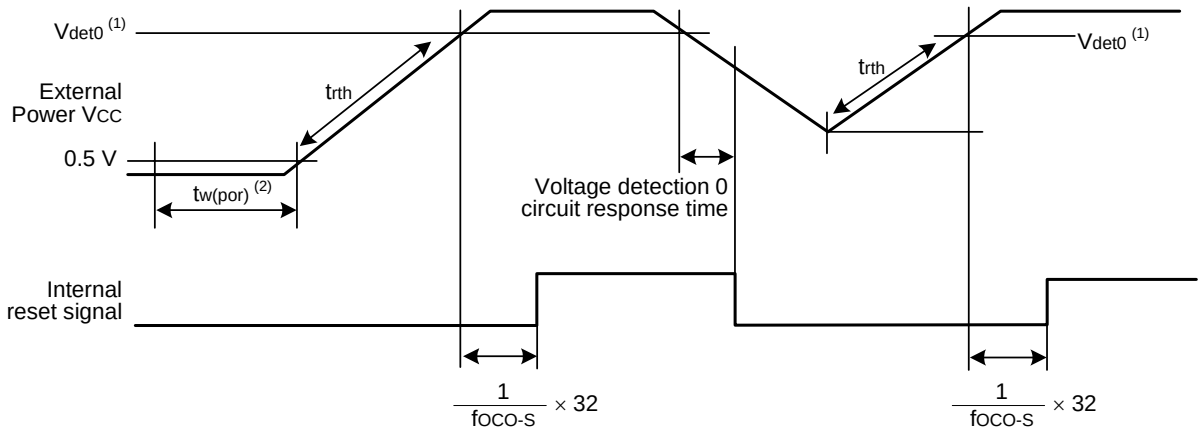
Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
V_{det2}	Voltage detection level Vdet2_0	At the falling of V_{CC}	3.70	4.00	4.30	V
–	Hysteresis width at the rising of Vcc in voltage detection 2 circuit		–	0.10	–	V
–	Voltage detection 2 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet2_0 – 0.1) V	–	20	150	µs
–	Voltage detection circuit self power consumption	VCA27 = 1, V_{CC} = 5.0 V	–	1.7	–	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		–	–	100	µs

Notes:
1. The measurement condition is V_{CC} = 1.8 V to 5.5 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version).
2. Time until the voltage monitor 2 interrupt request is generated after the voltage passes V_{det2}.
3. Necessary time until the voltage detection circuit operates after setting to 1 again after setting the VCA27 bit in the VCA2 register to 0.

Table 5.11 Power-on Reset Circuit (2)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{rth}	External power V_{CC} rise gradient	(1)	0	–	50,000	mV/msec

Notes:
1. The measurement condition is T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.



Notes:
1. V_{det0} indicates the voltage detection level of the voltage detection 0 circuit. Refer to **6. Voltage Detection Circuit** of User's Manual: Hardware (REJ09B0586) for details.
2. $t_{w(por)}$ indicates the duration the external power V_{CC} must be held below the valid voltage (0.5 V) to enable a power-on reset. When turning on the power after it falls with voltage monitor 0 reset disabled, maintain $t_{w(por)}$ for 1 ms or more.

Figure 5.3 Power-on Reset Circuit Electrical Characteristics

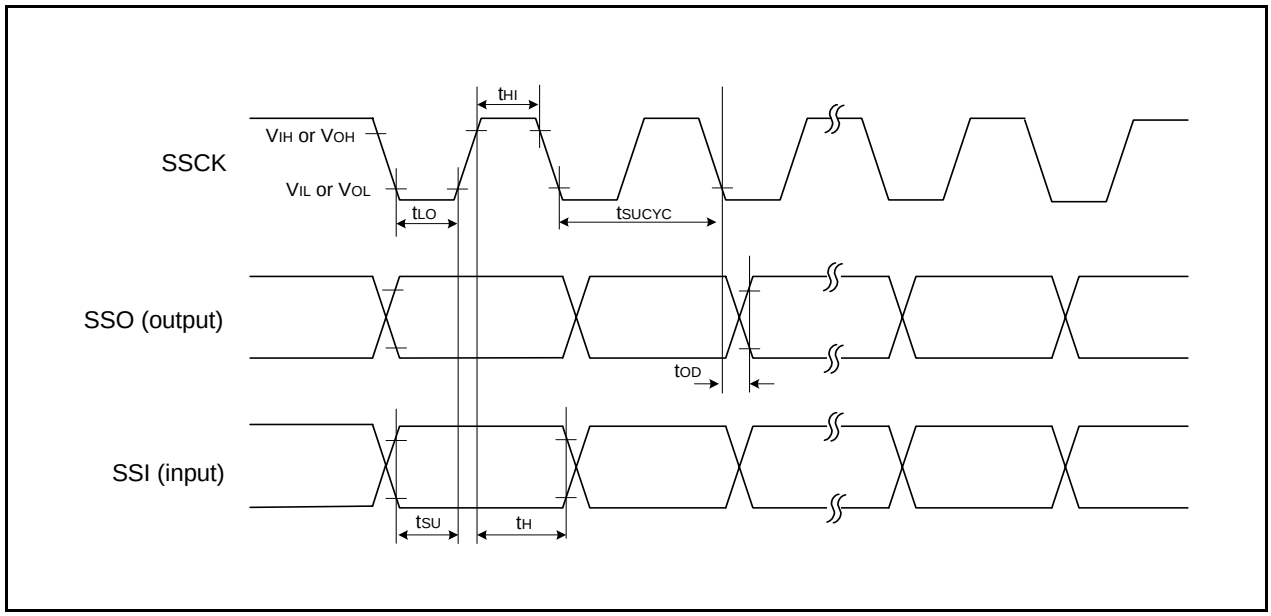
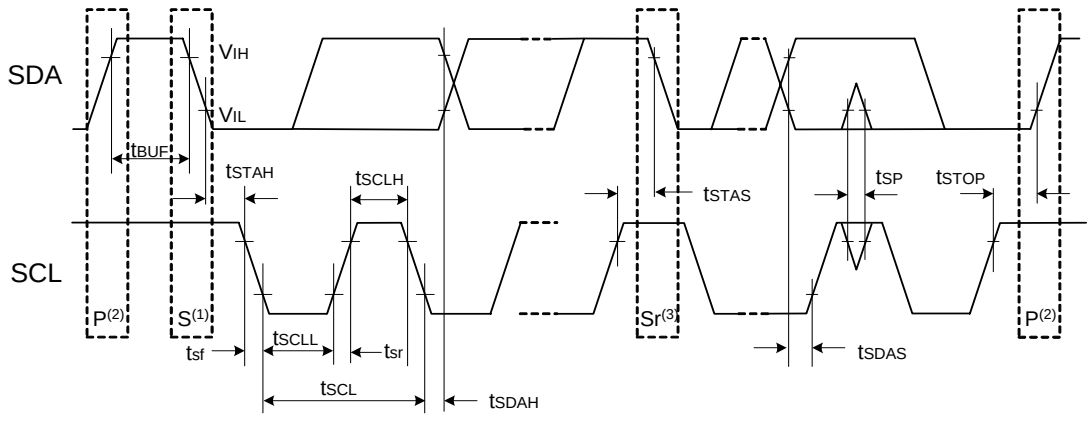


Figure 5.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 5.16 Timing Requirements of I²C bus Interface (1)

Symbol	Parameter	Condition	Standard			Unit
			Min.	Typ.	Max.	
t_{SCL}	SCL input cycle time		$12t_{CYC} + 600$ (2)	–	–	ns
t_{SCLH}	SCL input “H” width		$3t_{CYC} + 300$ (2)	–	–	ns
t_{SCLL}	SCL input “L” width		$5t_{CYC} + 500$ (2)	–	–	ns
t_{sf}	SCL, SDA input fall time		–	–	300	ns
t_{SP}	SCL, SDA input spike pulse rejection time		–	–	$1t_{CYC}$ (2)	ns
t_{BUF}	SDA input bus-free time		$5t_{CYC}$ (2)	–	–	ns
t_{STAH}	Start condition input hold time		$3t_{CYC}$ (2)	–	–	ns
t_{STAS}	Retransmit start condition input setup time		$3t_{CYC}$ (2)	–	–	ns
t_{STOP}	Stop condition input setup time		$3t_{CYC}$ (2)	–	–	ns
t_{SDAS}	Data input setup time		$1t_{CYC} + 40$ (2)	–	–	ns
t_{SDAH}	Data input hold time		10	–	–	ns

Notes:
1. V_{CC} = 1.8 to 5.5 V, V_{SS} = 0 V and T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.
2. $1t_{CYC} = 1/f1(s)$



Notes:
1. Start condition
2. Stop condition
3. Retransmit start condition

Figure 5.7 I/O Timing of I²C bus Interface

Table 5.17 Electrical Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V]

Symbol	Parameter		Condition		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output “H” voltage	Other than XOUT	Drive capacity High V_{CC} = 5V	I_{OH} = –20 mA	V_{CC} – 2.0	–	V_{CC}	V
			Drive capacity Low V_{CC} = 5V	I_{OH} = –5 mA	V_{CC} – 2.0	–	V_{CC}	V
		XOUT	V_{CC} = 5V	I_{OH} = –200 µA	1.0	–	V_{CC}	V
V_{OL}	Output “L” voltage	Other than XOUT	Drive capacity High V_{CC} = 5V	I_{OL} = 20 mA	–	–	2.0	V
			Drive capacity Low V_{CC} = 5V	I_{OL} = 5 mA	–	–	2.0	V
		XOUT	V_{CC} = 5V	I_{OL} = 200 µA	–	–	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$, $\overline{INT1}$, $\overline{INT2}$, $\overline{INT3}$, $\overline{INT4}$, $\overline{KI0}$, $\overline{KI1}$, $\overline{KI2}$, $\overline{KI3}$, TRAIO, TRBO, TRCIOA, TRCIOB, TRCIOC, TRCIOD, TRDIOA0, TRDIOB0, TRDIOC0, TRDIOD0, TRDIOA1, TRDIOB1, TRDIOC1, TRDIOD1, $\overline{TRCTRG}$, TRCCLK, $\overline{ADTRG}$, RXD0, RXD1, RXD2, CLK0, CLK1, CLK2, SSI, SCL, SDA, SSO			0.1	1.2	–	V
		$\overline{RESET}$			0.1	1.2	–	V
I_{IH}	Input “H” current		VI = 5 V, V_{CC} = 5.0 V		–	–	5.0	µA
I_{IL}	Input “L” current		VI = 0 V, V_{CC} = 5.0 V		–	–	–5.0	µA
R_{PULLUP}	Pull-up resistance		VI = 0 V, V_{CC} = 5.0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			–	0.3	–	MΩ
R_{fXCIN}	Feedback resistance	XCIN			–	8	–	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	–	–	V

Note:
1. 4.2 V ≤ V_{CC} ≤ 5.5 V at T_{opr} = –20 to 85°C (N version) / –40 to 85°C (D version), f(XIN) = 20 MHz, unless otherwise specified.

Table 5.24 Electrical Characteristics (4) [2.7 V ≤ Vcc < 3.3 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
ICC	Power supply current (VCC = 2.7 to 3.3 V) Single-chip mode, output pins are open, other pins are VSS	High-speed clock mode	XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	3.5	10	mA
			XIN = 10 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	7.5	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	7.0	15	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 20 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	3.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	4.0	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 10 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.5	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	390	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	400	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0, VCA20 = 1	–	3.5	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5.0	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	µA

Timing Requirements
(Unless Otherwise Specified: Vcc = 3 V, Vss = 0 V at Topr = 25°C)

Table 5.25 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(XOUT)}$	XOUT input cycle time	50	–	ns
$t_{WH(XOUT)}$	XOUT input “H” width	24	–	ns
$t_{WL(XOUT)}$	XOUT input “L” width	24	–	ns
$t_{c(XCIN)}$	XCIN input cycle time	14	–	µs
$t_{WH(XCIN)}$	XCIN input “H” width	7	–	µs
$t_{WL(XCIN)}$	XCIN input “L” width	7	–	µs

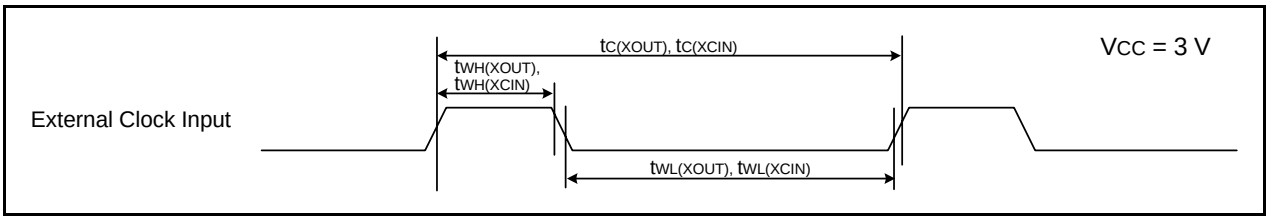


Figure 5.12 External Clock Input Timing Diagram when VCC = 3 V

Table 5.26 TRAIO Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TRAIO)}$	TRAIO input cycle time	300	–	ns
$t_{WH(TRAIO)}$	TRAIO input “H” width	120	–	ns
$t_{WL(TRAIO)}$	TRAIO input “L” width	120	–	ns

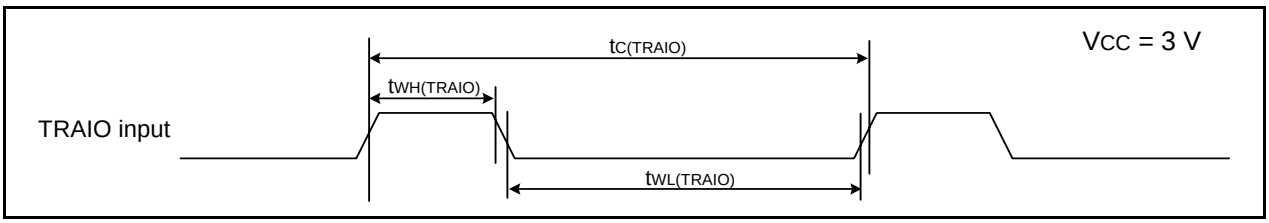


Figure 5.13 TRAIO Input Timing Diagram when Vcc = 3 V

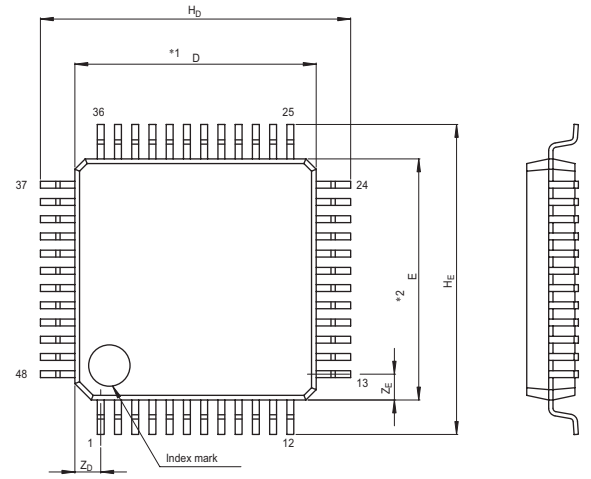
Table 5.30 Electrical Characteristics (6) [1.8 V ≤ Vcc < 2.7 V]
(Topr = –20 to 85°C (N version) / –40 to 85°C (D version), unless otherwise specified.)

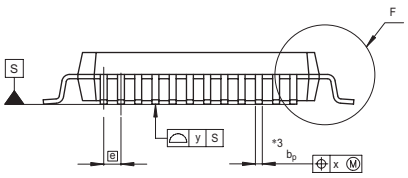
Symbol	Parameter	Condition		Standard			Unit
				Min.	Typ.	Max.	
Icc	Power supply current (Vcc = 1.8 to 2.7 V) Single-chip mode, output pins are open, other pins are Vss	High-speed clock mode	XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz No division	–	2.2	–	mA
			XIN = 5 MHz (square wave) High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	0.8	–	mA
		High-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz No division	–	2.5	10	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 5 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-8	–	1.7	–	mA
			XIN clock off High-speed on-chip oscillator on fOCO-F = 4 MHz Low-speed on-chip oscillator on = 125 kHz Divide-by-16 MSTIIC = MSTTRD = MSTTRC = 1	–	1	–	mA
		Low-speed on-chip oscillator mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz Divide-by-8, FMR27 = 1, VCA20 = 0	–	90	300	µA
		Low-speed clock mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division FMR27 = 1, VCA20 = 0	–	80	350	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz No division Program operation on RAM Flash memory off, FMSTP = 1, VCA20 = 0	–	40	–	µA
		Wait mode	XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock operation VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	15	90	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator on = 125 kHz While a WAIT instruction is executed Peripheral clock off VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	4	80	µA
			XIN clock off High-speed on-chip oscillator off Low-speed on-chip oscillator off XCIN clock oscillator on = 32 kHz (peripheral clock off) While a WAIT instruction is executed VCA27 = VCA26 = VCA25 = 0 VCA20 = 1	–	3.5	–	µA
		Stop mode	XIN clock off, Topr = 25°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	2.0	5	µA
			XIN clock off, Topr = 85°C High-speed on-chip oscillator off Low-speed on-chip oscillator off CM10 = 1 Peripheral clock off VCA27 = VCA26 = VCA25 = 0	–	5.0	–	µA

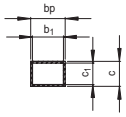
Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

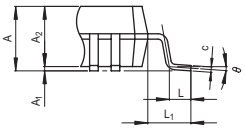
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP48-7x7-0.50	PLQP0048KB-A	48P6Q-A	0.2g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A_2	—	1.4	—
H_D	8.8	9.0	9.2
H_E	8.8	9.0	9.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	0.75	—
Z_E	—	0.75	—
L	0.35	0.5	0.65
L_1	—	1.0	—