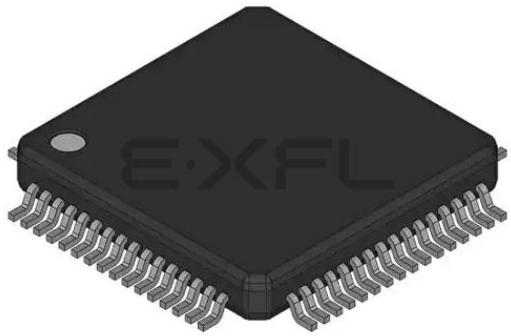

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- Prior to executing BCLR instruction

```
MOV.B   #3F,  R0L
MOV.B   R0L,  @RAM0
MOV.B   R0L,  @PCR5
```

The PCR5 value (H'3F) is written to a work area in memory (RAM0) as well as to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	Low level
PCR5	0	0	1	1	1	1	1	1
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	1

- BCLR instruction executed

```
BCLR    #0,     @RAM0
```

The BCLR instructions executed for the PCR5 work area (RAM0).

- After executing BCLR instruction

```
MOV.B   @RAM0, R0L
MOV.B   R0L,  @PCR5
```

The work area (RAM0) value is written to PCR5.

	P57	**P56**	**P55**	**P54**	**P53**	**P52**	**P51**	**P50**
Input/output	Input	Input	Output	Output	Output	Output	Output	Output
Pin state	Low level	High level	Low level	Low level	Low level	Low level	Low level	High level
PCR5	0	0	1	1	1	1	1	0
PDR5	1	0	0	0	0	0	0	0
RAM0	0	0	1	1	1	1	1	0

When the address break is specified in the data read cycle

Register setting
- ABRKCR = H'A0
- BAR = H'025A

Program

```
  0258   NOP
  025A   NOP
* 025C   MOV.W @H'025A,R0
  0260   NOP
  0262   NOP
   :      :
```

Underline indicates the address to be stacked.

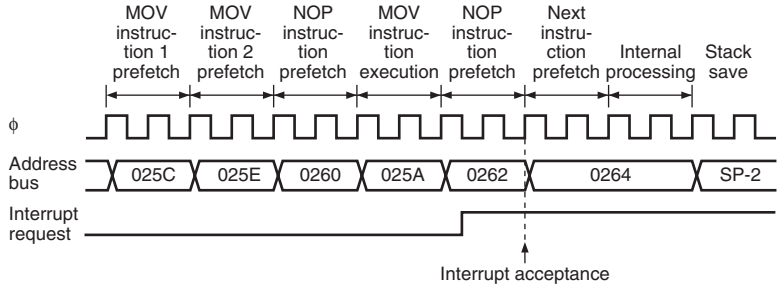


Figure 4.2 Address Break Interrupt Operation Example (2)

9.1.2 Port Control Register 1 (PCR1)

PCR1 selects inputs/outputs in bit units for pins to be used as general I/O ports of port 1.

Bit	Bit Name	Initial Value	R/W	Description
7	PCR17	0	W	When the corresponding pin is designated in PMR1 as a general I/O pin, setting a PCR1 bit to 1 makes the corresponding pin an output port, while clearing the bit to 0 makes the pin an input port.
6	PCR16	0	W	
5	PCR15	0	W	
4	PCR14	0	W	Bit 3 is a reserved bit.
3	—	—	—	
2	PCR12	0	W	
1	PCR11	0	W	
0	PCR10	0	W	

9.1.3 Port Data Register 1 (PDR1)

PDR1 is a general I/O port data register of port 1.

Bit	Bit Name	Initial Value	R/W	Description
7	P17	0	R/W	PDR1 stores output data for port 1 pins.
6	P16	0	R/W	If PDR1 is read while PCR1 bits are set to 1, the value stored in PDR1 are read. If PDR1 is read while PCR1 bits are cleared to 0, the pin states are read regardless of the value stored in PDR1.
5	P15	0	R/W	
4	P14	0	R/W	
3	—	1	—	Bit 3 is a reserved bit. This bit is always read as 1.
2	P12	0	R/W	
1	P11	0	R/W	
0	P10	0	R/W	

12.5.2 Pulse Output with Arbitrary Pulse Width and Delay from TRGV Input

The trigger function can be used to output a pulse with an arbitrary pulse width at an arbitrary delay from the TRGV input, as shown in figure 12.10. To set up this output:

1. Set bits CCLR1 and CCLR0 in TCRV0 so that TCNTV will be cleared by compare match with TCORB.
2. Set bits OS3 to OS0 in TCSRV so that the output will go to 1 at compare match with TCORA and to 0 at compare match with TCORB.
3. Set bits TVEG1 and TVEG0 in TCRV1 and set TRGE to select the falling edge of the TRGV input.
4. Set bits CKS2 to CKS0 in TCRV0 and bit ICKS0 in TCRV1 to select the desired clock source.
5. After these settings, a pulse waveform will be output without further software intervention, with a delay determined by TCORA from the TRGV input, and a pulse width determined by (TCORB – TCORA).

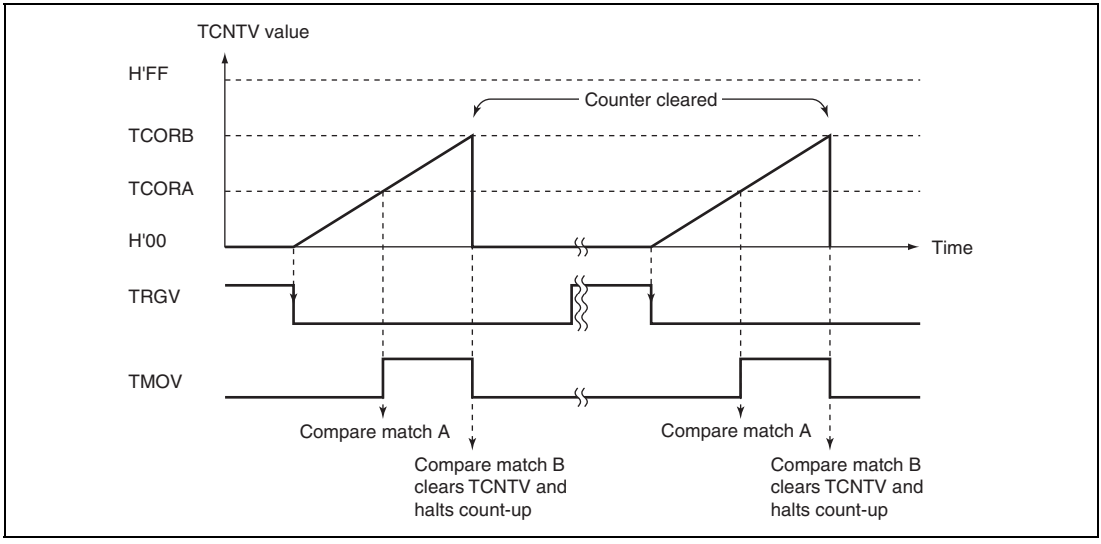


Figure 12.10 Example of Pulse Output Synchronized to TRGV Input

13.4.4 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing). Synchronous operation enables GR to be increased with respect to a single time base.

Figure 13.19 shows an example of the synchronous operation setting procedure.

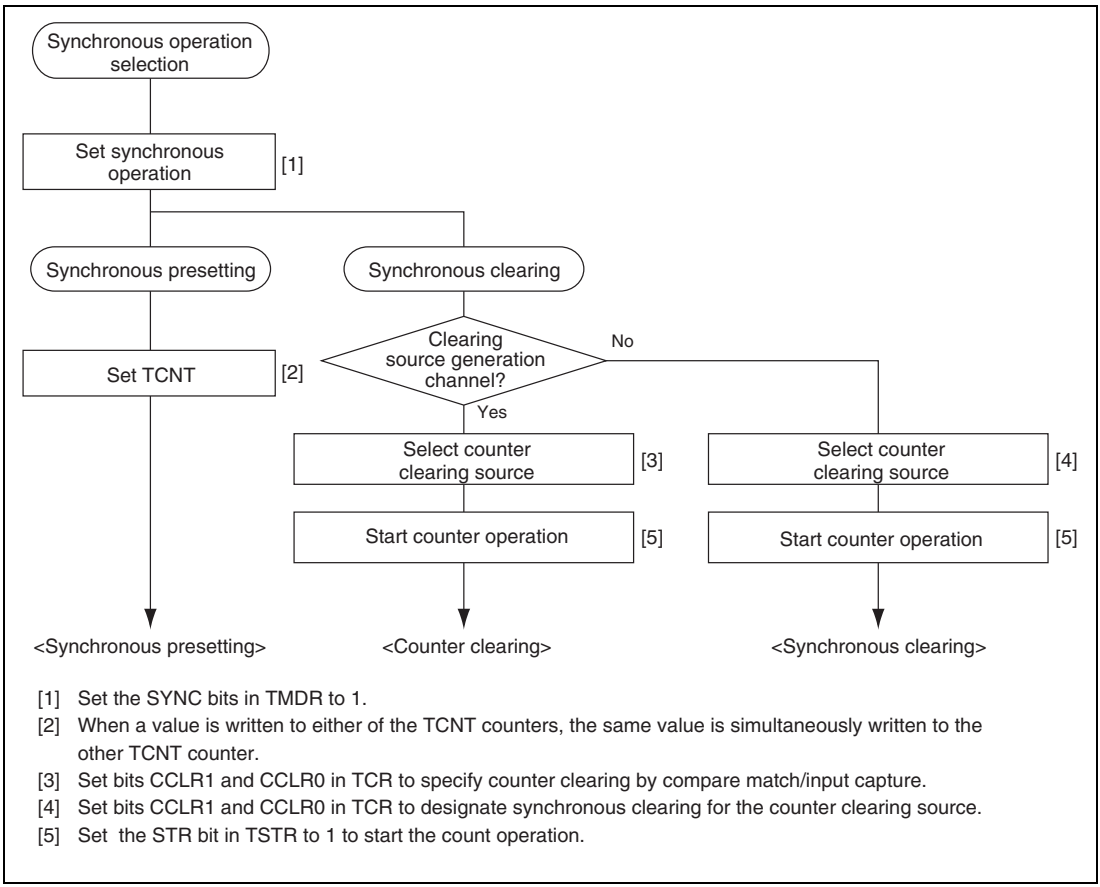


Figure 13.19 Example of Synchronous Operation Setting Procedure

Figure 13.22 shows an example of operation in PWM mode. The output signals go to 1 and TCNT is reset at compare match A, and the output signals go to 0 at compare match B, C, and D (TOB, TOC, and TOD = 1, POLB, POLC, and POLD = 0).

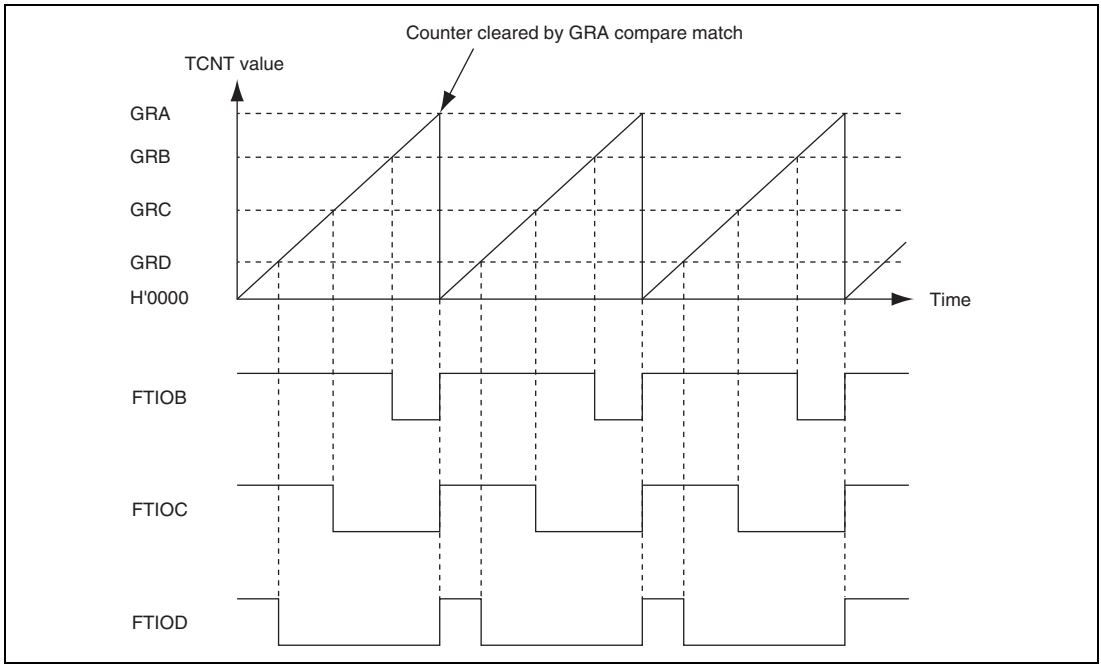
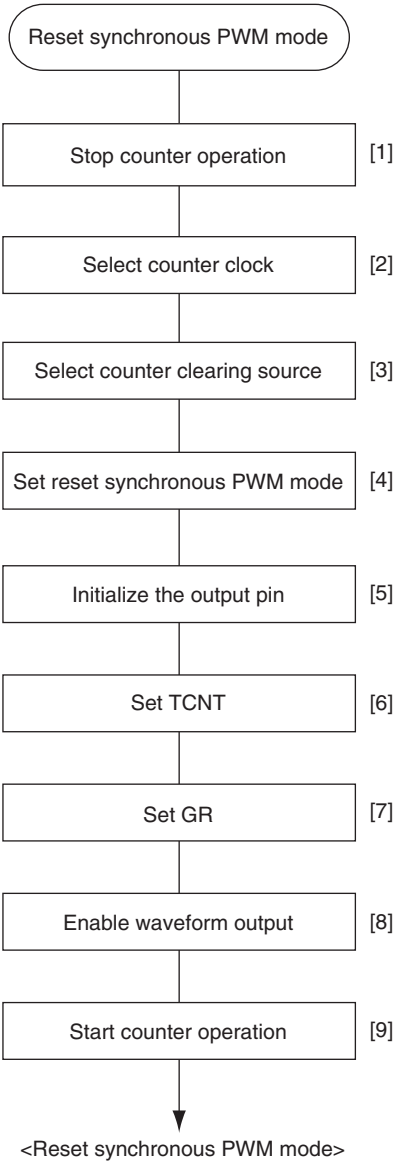


Figure 13.22 Example of PWM Mode Operation (1)

Figure 13.23 shows another example of operation in PWM mode. The output signals go to 0 and TCNT is reset at compare match A, and the output signals go to 1 at compare match B, C, and D (TOB, TOC, and TOD = 0, POLB, POLC, and POLD = 1).



[1] Clear bit STR0 in TSTR to 0 and stop the counter operation of TCNT_0. Set reset synchronous PWM mode after TCNT_0 stops.
[2] Select the counter clock with bits TPSC2 to TOSC0 in TCR. When an external clock is selected, select the external clock edge with bits CKEG1 and CKEG0 in TCR.
[3] Use bits CCLR1 and CCLR0 in TCR to select counter clearing source GRA_0.
[4] Select the reset synchronous PWM mode with bits CMD1 and CMD0 in TFCR. FTIOB0 to FTIOD0 and FTIOA1 to FTIOD1 become PWM output pins automatically.
[5] Set H'00 to TOCR.
[6] Set TCNT_0 as H'0000. TCNT1 does not need to be set.
[7] GRA_0 is a cycle register. Set a cycle for GRA_0. Set the changing point timing of the PWM output waveform for GRB_0, GRA_1, and GRB_1.
[8] Enable or disable the timer output by TOER.
[9] Set the STR bit in TSTR to 1 and start the counter operation.

Figure 13.26 Example of Reset Synchronous PWM Mode Setting Procedure

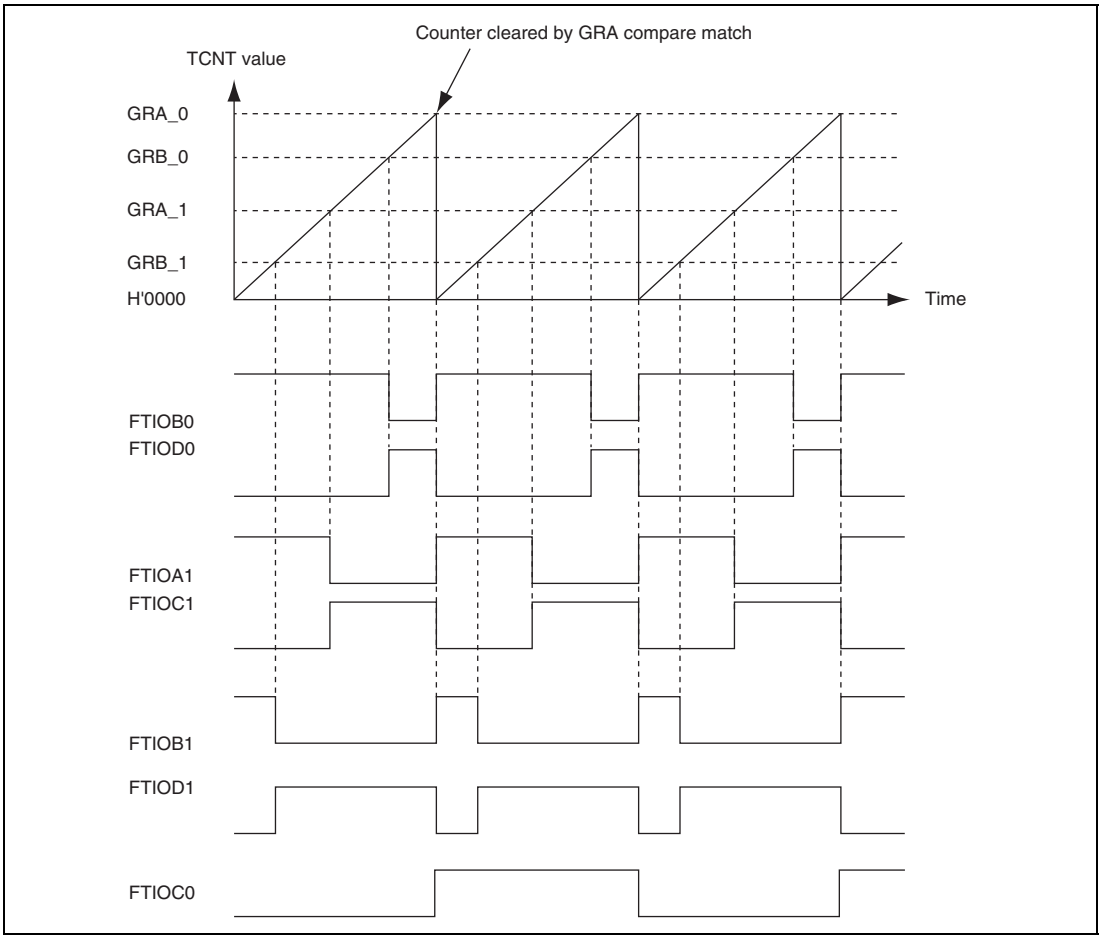


Figure 13.28 Example of Reset Synchronous PWM Mode Operation (OLS0 = OLS1 = 0)

In reset synchronous PWM mode, TCNT_0 and TCNT_1 perform increment and independent operations, respectively. However, GRA_1 and GRB_1 are separated from TCNT_1. When a compare match occurs between TCNT_0 and GRA_0, a counter is cleared and an increment operation is restarted from H'0000.

The PWM pin outputs 0 or 1 whenever a compare match between GRB_0, GRA_1, GRB_1 and TCNT_0 or counter clearing occur.

For details on operations when reset synchronous PWM mode and buffer operation are simultaneously set, refer to section 13.4.8, Buffer Operation.

13.4.8 Buffer Operation

Buffer operation differs depending on whether GR has been designated for an input capture register or an output compare register, or in reset synchronous PWM mode or complementary PWM mode.

Table 13.8 shows the register combinations used in buffer operation.

Table 13.8 Register Combinations in Buffer Operation

General Register	Buffer Register
GRA	GRC
GRB	GRD

1. When GR is an output compare register

   When a compare match occurs, the value in the buffer register of the corresponding channel is transferred to the general register.

   This operation is illustrated in figure 13.35.

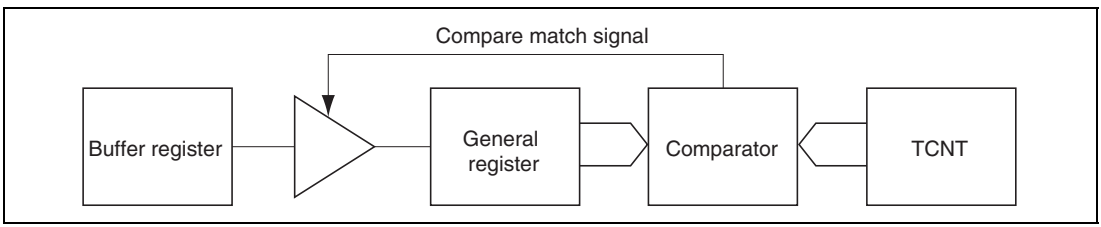


Figure 13.35 Compare Match Buffer Operation

2. When GR is an input capture register

   When an input capture occurs, the value in TCNT is transferred to the general register and the value previously stored in the general register is transferred to the buffer register.

   This operation is illustrated in figure 13.36.

6. Examples of Buffer Operation

Figure 13.38 shows an operation example in which GRA has been designated as an output compare register, and buffer operation has been designated for GRA and GRC.

This is an example of TCNT operating as a periodic counter cleared by compare match B.

Pins FTIOA and FTIOB are set for toggle output by compare match A and B.

As buffer operation has been set, when compare match A occurs, the FTIOA pin performs toggle outputs and the value in buffer register is simultaneously transferred to the general register. This operation is repeated each time that compare match A occurs.

The timing to transfer data is shown in figure 13.39.

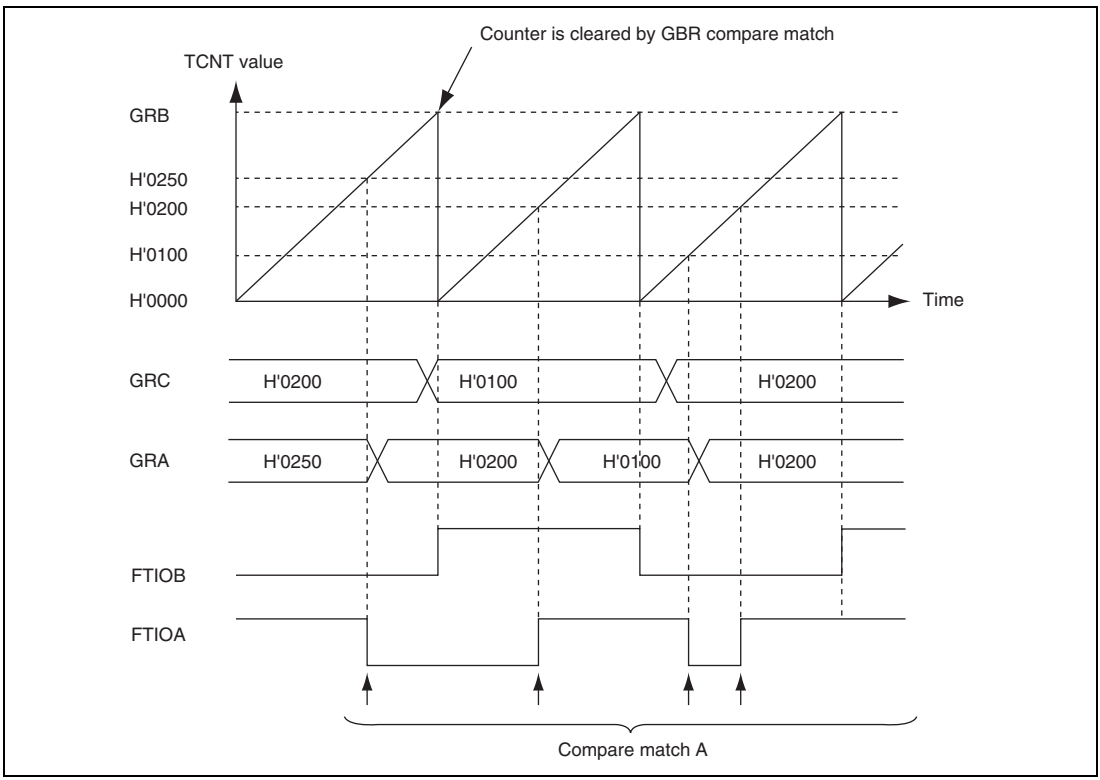


Figure 13.38 Example of Buffer Operation (1)
(Buffer Operation for Output Compare Register)

Bit	Bit Name	Initial Value	R/W	Description
3	MPIE	0	R/W	Multiprocessor Interrupt Enable (enabled only when the MP bit in SMR is 1 in asynchronous mode) When this bit is set to 1, receive data in which the multiprocessor bit is 0 is skipped, and setting of the RDRF, FER, and OER status flags in SSR is disabled. On receiving data in which the multiprocessor bit is 1, this bit is automatically cleared and normal reception is resumed. For details, refer to section 16.6, Multiprocessor Communication Function.
2	TEIE	0	R/W	Transmit End Interrupt Enable When this bit is set to 1, TEI interrupt request is enabled.
1	CKE1	0	R/W	Clock Enable 0 and 1
0	CKE0	0	R/W	Selects the clock source. • Asynchronous mode 00: On-chip baud rate generator 01: On-chip baud rate generator Outputs a clock of the same frequency as the bit rate from the SCK3 pin. 10: External clock Inputs a clock with a frequency 16 times the bit rate from the SCK3 pin. 11: Reserved • Clocked synchronous mode 00: On-chip clock (SCK3 pin functions as clock output) 01: Reserved 10: External clock (SCK3 pin functions as clock input) 11: Reserved

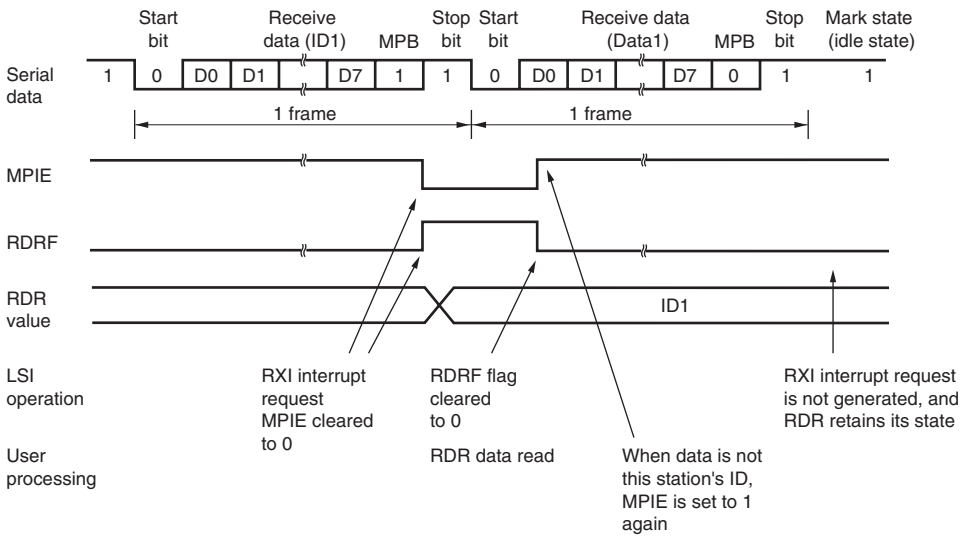
Table 16.3 Examples of BRR Settings for Various Bit Rates (Asynchronous Mode) (2)

	Operating Frequency ϕ (MHz)								
	6			6.144			7.3728		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	106	–0.44	2	108	0.08	2	130	–0.07
150	2	77	0.16	2	79	0.00	2	95	0.00
300	1	155	0.16	1	159	0.00	1	191	0.00
600	1	77	0.16	1	79	0.00	1	95	0.00
1200	0	155	0.16	0	159	0.00	0	191	0.00
2400	0	77	0.16	0	79	0.00	0	95	0.00
4800	0	38	0.16	0	39	0.00	0	47	0.00
9600	0	19	–2.34	0	19	0.00	0	23	0.00
19200	0	9	–2.34	0	9	0.00	0	11	0.00
31250	0	5	0.00	0	5	2.40	0	6	5.33
38400	0	4	–2.34	0	4	0.00	0	5	0.00

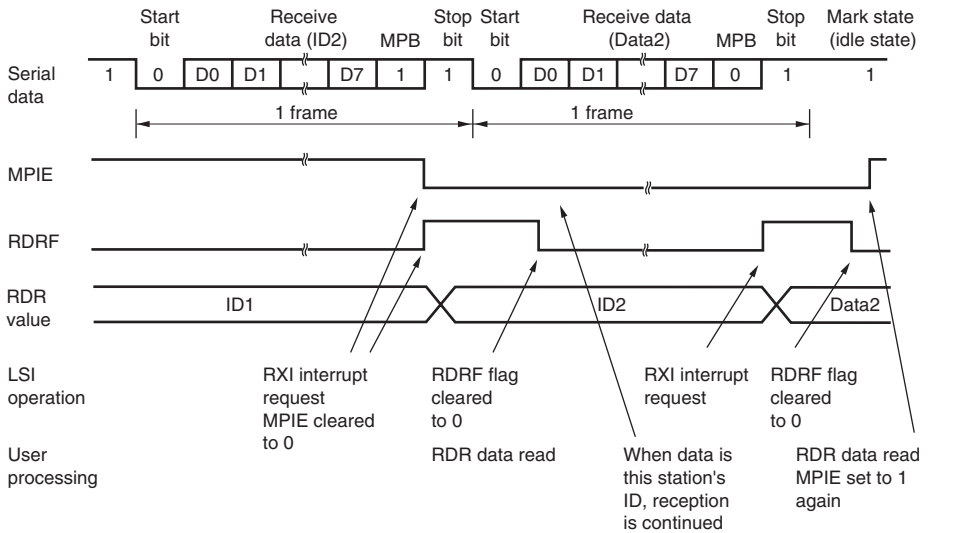
	Operating Frequency ϕ (MHz)											
	8			9.8304			10			12		
Bit Rate (bit/s)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	–0.26	2	177	–0.25	2	212	0.03
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16
9600	0	25	0.16	0	31	0.00	0	32	–1.36	0	38	0.16
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	–2.34
31250	0	7	0.00	0	9	–1.70	0	9	0.00	0	11	0.00
38400	0	6	-6.99	0	7	0.00	0	7	1.73	0	9	–2.34

Legend:

—: A setting is available but error occurs.



(a) When data does not match this receiver's ID



(b) When data matches this receiver's ID

Figure 16.18 Example of SCI3 Reception Using Multiprocessor Format (Example with 8-Bit Data, Multiprocessor Bit, One Stop Bit)

Bit	Bit Name	Initial Value	R/W	Description
5, 4	—	All 1	—	Reserved These bits are always read as 1, and cannot be modified.
3	BCWP	1	R/W	BC Write Protect This bit controls the BC2 to BC0 modifications. When modifying BC2 to BC0, this bit should be cleared to 0 and use the MOV instruction. In clock synchronous serial mode, BC should not be modified. 0: When writing, values of BC2 to BC0 are set. 1: When reading, 1 is always read. When writing, settings of BC2 to BC0 are invalid.
2	BC2	0	R/W	Bit Counter 2 to 0 These bits specify the number of bits to be transferred next. When read, the remaining number of transfer bits is indicated. With the I²C bus format, the data is transferred with one addition acknowledge bit. Bit BC2 to BC0 settings should be made during an interval between transfer frames. If bits BC2 to BC0 are set to a value other than 000, the setting should be made while the SCL pin is low. The value returns to 000 at the end of a data transfer, including the acknowledge bit. With the clock synchronous serial format, these bits should not be modified. I²C Bus Format / Clock Synchronous Serial Format 000: 9 bits / 000: 8 bits 001: 2 bits / 001: 1 bits 010: 3 bits / 010: 2 bits 011: 4 bits / 011: 3 bits 100: 5 bits / 100: 4 bits 101: 6 bits / 101: 5 bits 110: 7 bits / 110: 6 bits 111: 8 bits / 111: 7 bits
1	BC1	0	R/W	
0	BC0	0	R/W	

17.4.6 Clocked Synchronous Serial Format

This module can be operated with the clocked synchronous serial format, by setting the FS bit in SAR to 1. When the MST bit in ICCR1 is 1, the transfer clock output from SCL is selected. When MST is 0, the external clock input is selected.

Data Transfer Format

Figure 17.13 shows the clocked synchronous serial transfer format.

The transfer data is output from the rise to the fall of the SCL clock, and the data at the rising edge of the SCL clock is guaranteed. The MLS bit in ICMR sets the order of data transfer, in either the MSB first or LSB first. The output level of SDA can be changed during the transfer wait, by the SDAO bit in ICCR2.

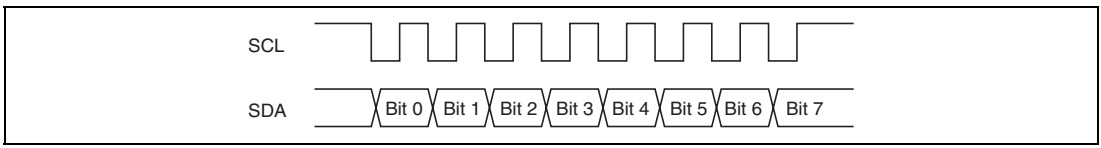


Figure 17.13 Clocked Synchronous Serial Transfer Format

Transmit Operation

In transmit mode, transmit data is output from SDA, in synchronization with the fall of the transfer clock. The transfer clock is output when MST in ICCR1 is 1, and is input when MST is 0. For transmit mode operation timing, refer to figure 17.14. The transmission procedure and operations in transmit mode are described below.

1. Set the ICE bit in ICCR1 to 1. Set the MST and CKS3 to CKS0 bits in ICCR1 to 1. (Initial setting)
2. Set the TRS bit in ICCR1 to select the transmit mode. Then, TDRE in ICSR is set.
3. Confirm that TDRE has been set. Then, write the transmit data to ICDRT. The data is transferred from ICDRT to ICDRS, and TDRE is set automatically. The continuous transmission is performed by writing data to ICDRT every time TDRE is set. When changing from transmit mode to receive mode, clear TRS while TDRE is 1.

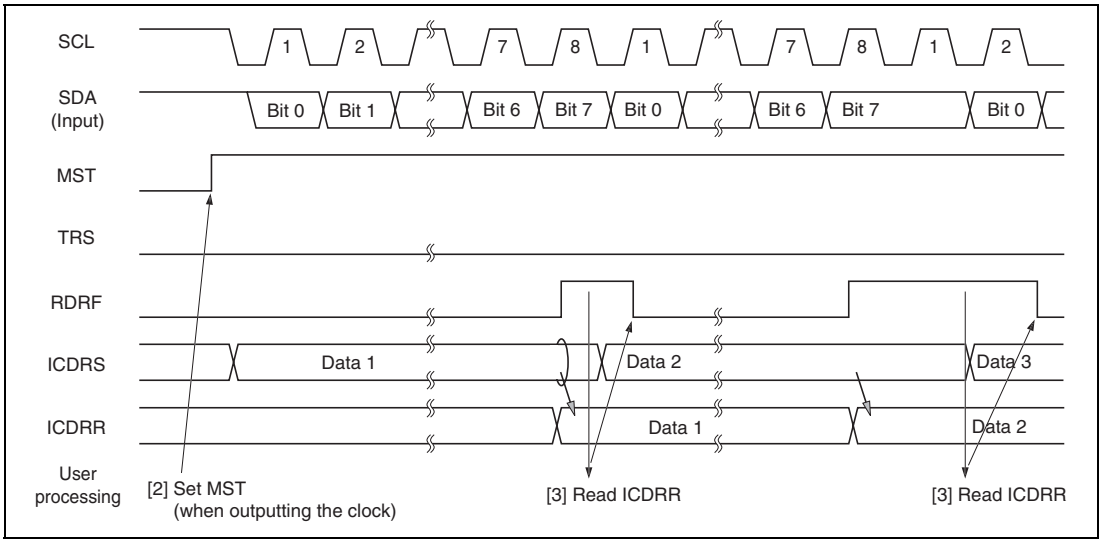


Figure 17.15 Receive Mode Operation Timing

17.4.7 Noise Canceler

The logic levels at the SCL and SDA pins are routed through noise cancelers before being latched internally. Figure 17.16 shows a block diagram of the noise canceler circuit.

The noise canceler consists of two cascaded latches and a match detector. The SCL (or SDA) input signal is sampled on the system clock, but is not passed forward to the next circuit unless the outputs of both latches agree. If they do not agree, the previous value is held.

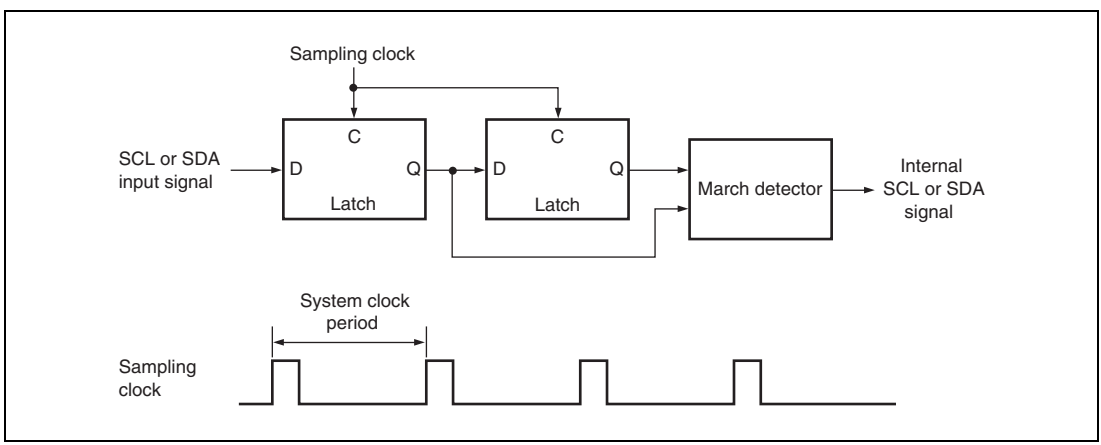


Figure 17.16 Block Diagram of Noise Conceler

Register Name	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
PDR2	Initialized	—	—	—	—	—	I/O port
PDR3	Initialized	—	—	—	—	—	
PDR5	Initialized	—	—	—	—	—	
PDR6	Initialized	—	—	—	—	—	
PDR7	Initialized	—	—	—	—	—	
PDR8	Initialized	—	—	—	—	—	
PDRB	Initialized	—	—	—	—	—	
PMR1	Initialized	—	—	—	—	—	
PMR5	Initialized	—	—	—	—	—	
PMR3	Initialized	—	—	—	—	—	
PCR1	Initialized	—	—	—	—	—	
PCR2	Initialized	—	—	—	—	—	
PCR3	Initialized	—	—	—	—	—	
PCR5	Initialized	—	—	—	—	—	
PCR6	Initialized	—	—	—	—	—	
PCR7	Initialized	—	—	—	—	—	
PCR8	Initialized	—	—	—	—	—	
SYSCR1	Initialized	—	—	—	—	—	Low power
SYSCR2	Initialized	—	—	—	—	—	
IEGR1	Initialized	—	—	—	—	—	Interrupt
IEGR2	Initialized	—	—	—	—	—	
IENR1	Initialized	—	—	—	—	—	
IENR2	Initialized	—	—	—	—	—	
IRR1	Initialized	—	—	—	—	—	
IRR2	Initialized	—	—	—	—	—	
IWPR	Initialized	—	—	—	—	—	
MSTCR1	Initialized	—	—	—	—	—	Low power
MSTCR2	Initialized	—	—	—	—	—	

Appendix C Product Code Lineup

Product Classification			Product Code	Model Marking	Package Code
H8/3687	Flash memory version	Standard product	HD64F3687H	HD64F3687H	QFP-64 (FP-64A)
			HD64F3687FP	HD64F3687FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD64F3687GH	HD64F3687GH	QFP-64 (FP-64A)
			HD64F3687GFP	HD64F3687GFP	LQFP-64 (FP-64E)
	Mask ROM version	Standard product	HD6433687H	HD6433687(***)H	QFP-64 (FP-64A)
			HD6433687FP	HD6433687(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433687GH	HD6433687G(***)H	QFP-64 (FP-64A)
			HD6433687GFP	HD6433687G(***)FP	LQFP-64 (FP-64E)
H8/3686	Mask ROM version	Standard product	HD6433686H	HD6433686(***)H	QFP-64 (FP-64A)
			HD6433686FP	HD6433686(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433686GH	HD6433686G(***)H	QFP-64 (FP-64A)
			HD6433686GFP	HD6433686G(***)FP	LQFP-64 (FP-64E)
H8/3685	Mask ROM version	Standard product	HD6433685H	HD6433685(***)H	QFP-64 (FP-64A)
			HD6433685FP	HD6433685(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433685GH	HD6433685G(***)H	QFP-64 (FP-64A)
			HD6433685GFP	HD6433685G(***)FP	LQFP-64 (FP-64E)
H8/3684	Flash memory version	Standard product	HD64F3684H	HD64F3684H	QFP-64 (FP-64A)
			HD64F3684FP	HD64F3684FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD64F3684GH	HD64F3684GH	QFP-64 (FP-64A)
			HD64F3684GFP	HD64F3684GFP	LQFP-64 (FP-64E)
	Mask ROM version	Standard product	HD6433684H	HD6433684(***)H	QFP-64 (FP-64A)
			HD6433684FP	HD6433684(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433684GH	HD6433684G(***)H	QFP-64 (FP-64A)
			HD6433684GFP	HD6433684G(***)FP	LQFP-64 (FP-64E)
H8/3683	Mask ROM version	Standard product	HD6433683H	HD6433683(***)H	QFP-64 (FP-64A)
			HD6433683FP	HD6433683(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433683GH	HD6433683G(***)H	QFP-64 (FP-64A)
			HD6433683GFP	HD6433683G(***)FP	LQFP-64 (FP-64E)
H8/3682	Mask ROM version	Standard product	HD6433682H	HD6433682(***)H	QFP-64 (FP-64A)
			HD6433682FP	HD6433682(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433682GH	HD6433682G(***)H	QFP-64 (FP-64A)
			HD6433682GFP	HD6433682G(***)FP	LQFP-64 (FP-64E)