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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, SCI
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	32KB (32K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3684fpv

1.2 Internal Block Diagram

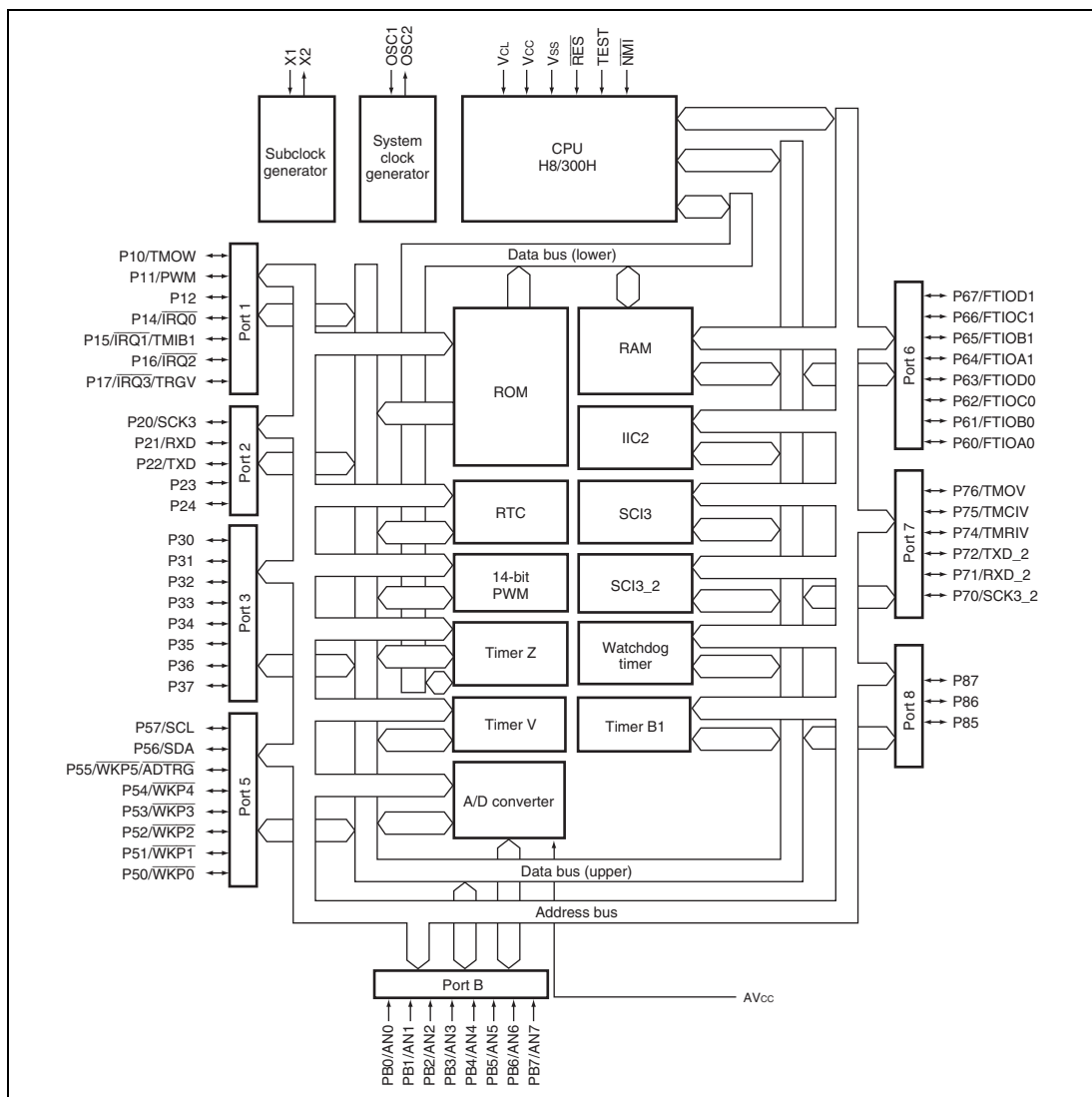


Figure 1.1 Internal Block Diagram of H8/3687 Group of F-ZTAT™ and Mask-ROM Versions

2.6.2 On-Chip Peripheral Modules

On-chip peripheral modules are accessed in two states or three states. The data bus width is 8 bits or 16 bits depending on the register. For description on the data bus width and number of accessing states of each register, refer to section 22.1, Register Addresses (Address Order). Registers with 16-bit data bus width can be accessed by word size only. Registers with 8-bit data bus width can be accessed by byte or word size. When a register with 8-bit data bus width is accessed by word size, a bus cycle occurs twice. In two-state access, the operation timing is the same as that for on-chip memory.

Figure 2.10 shows the operation timing in the case of three-state access to an on-chip peripheral module.

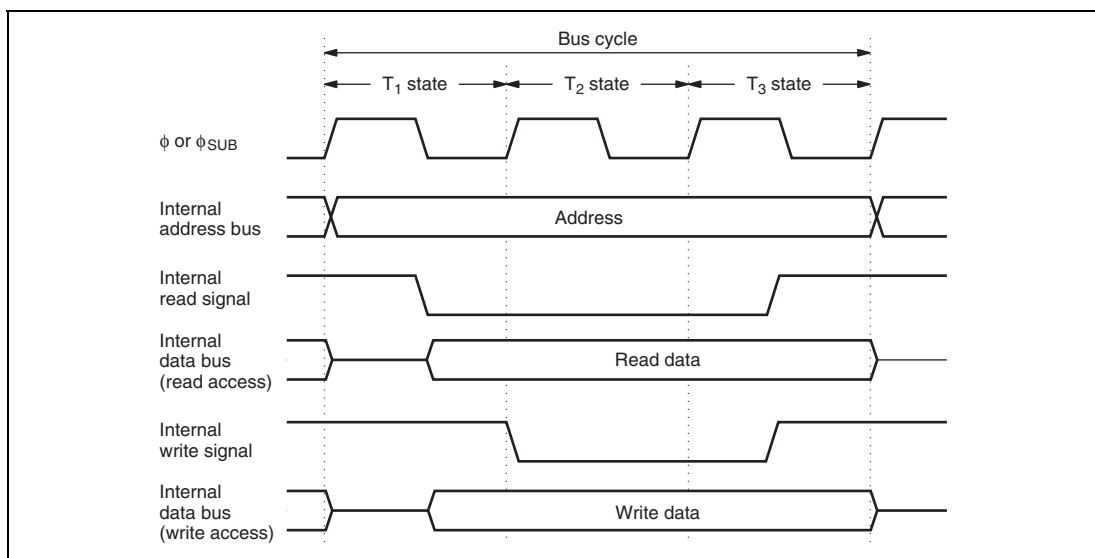
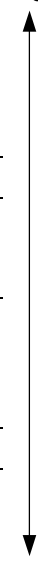


Figure 2.10 On-Chip Peripheral Module Access Cycle (3-State Access)

Relative Module	Exception Sources	Vector Number	Vector Address	Priority
IIC2	Transmit data empty Transmit end Receive data full Arbitration lost/Overrun error NACK detection Stop conditions detected	24	H'0030 to H'0031	 <p>High</p> <p>Low</p>
A/D converter	A/D conversion end	25	H'0032 to H'0033	
Timer Z	Compare match/input capture A0 to D0 Timer Z overflow	26	H'0034 to H'0035	
	Compare match/input capture A1 to D1 Timer Z overflow Timer Z underflow	27	H'0036 to H'0037	
Timer B1	Timer B1 overflow	29	H'003A to H'003B	
SCI3_2	Receive data full Transmit data empty Transmit end Receive error	32	H'0040 to H'0041	

Note: * A low-voltage detection interrupt is enabled only in the product with an on-chip power-on reset and low-voltage detection circuit.

3.2 Register Descriptions

Interrupts are controlled by the following registers.

- Interrupt edge select register 1 (IEGR1)
- Interrupt edge select register 2 (IEGR2)
- Interrupt enable register 1 (IENR1)
- Interrupt enable register 2 (IENR2)
- Interrupt flag register 1 (IRR1)
- Interrupt flag register 2 (IRR2)
- Wakeup interrupt flag register (IWPR)

3.2.2 Interrupt Edge Select Register 2 (IEGR2)

IEGR2 selects the direction of an edge that generates interrupt requests of the pins $\overline{\text{ADTRG}}$ and $\overline{\text{WKP5}}$ to $\overline{\text{WKP0}}$.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 1	—	Reserved These bits are always read as 1.
5	WPEG5	0	R/W	WKP5 Edge Select 0: Falling edge of $\overline{\text{WKP5(ADTRG)}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP5(ADTRG)}}$ pin input is detected
4	WPEG4	0	R/W	WKP4 Edge Select 0: Falling edge of $\overline{\text{WKP4}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP4}}$ pin input is detected
3	WPEG3	0	R/W	WKP3 Edge Select 0: Falling edge of $\overline{\text{WKP3}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP3}}$ pin input is detected
2	WPEG2	0	R/W	WKP2 Edge Select 0: Falling edge of $\overline{\text{WKP2}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP2}}$ pin input is detected
1	WPEG1	0	R/W	WKP1 Edge Select 0: Falling edge of $\overline{\text{WKP1}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP1}}$ pin input is detected
0	WPEG0	0	R/W	WKP0 Edge Select 0: Falling edge of $\overline{\text{WKP0}}$ pin input is detected 1: Rising edge of $\overline{\text{WKP0}}$ pin input is detected

- Break address register (BARH, BARL)
- Break data register (BDRH, BDRL)

4.1.1 Address Break Control Register (ABRKCR)

ABRKCR sets address break conditions.

Bit	Bit Name	Initial Value	R/W	Description
7	RTINTE	1	R/W	RTE Interrupt Enable When this bit is 0, the interrupt immediately after executing RTE is masked and then one instruction must be executed. When this bit is 1, the interrupt is not masked.
6	CSEL1	0	R/W	Condition Select 1 and 0
5	CSEL0	0	R/W	These bits set address break conditions. 00: Instruction execution cycle 01: CPU data read cycle 10: CPU data write cycle 11: CPU data read/write cycle
4	ACMP2	0	R/W	Address Compare Condition Select 2 to 0
3	ACMP1	0	R/W	These bits set the comparison condition between the address set in BAR and the internal address bus.
2	ACMP0	0	R/W	000: Compares 16-bit addresses 001: Compares upper 12-bit addresses 010: Compares upper 8-bit addresses 011: Compares upper 4-bit addresses 1XX: Reserved (setting prohibited)
1	DCMP1	0	R/W	Data Compare Condition Select 1 and 0
0	DCMP0	0	R/W	These bits set the comparison condition between the data set in BDR and the internal data bus. 00: No data comparison 01: Compares lower 8-bit data between BDRL and data bus 10: Compares upper 8-bit data between BDRH and data bus 11: Compares 16-bit data between BDR and data bus

Legend: X: Don't care.

9.2.2 Port Data Register 2 (PDR2)

PDR2 is a general I/O port data register of port 2.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 1	—	Reserved These bits are always read as 1.
4	P24	0	R/W	PDR2 stores output data for port 2 pins.
3	P23	0	R/W	If PDR2 is read while PCR2 bits are set to 1, the value stored in PDR2 is read. If PDR2 is read while PCR2 bits are cleared to 0, the pin states are read regardless of the value stored in PDR2.
2	P22	0	R/W	
1	P21	0	R/W	
0	P20	0	R/W	

9.2.3 Port Mode Register 3 (PMR3)

PMR3 selects the CMOS output or NMOS open-drain output for port 2.

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	—	Reserved These bits are always read as 0.
4	POF24	0	R/W	When the bit is set to 1, the corresponding pin is cut off by PMOS and it functions as the NMOS open-drain output. When cleared to 0, the pin functions as the CMOS output.
3	POF23	0	R/W	
2 to 0	—	All 1	—	Reserved These bits are always read as 1.

10.3.6 RTC Control Register 2 (RTCCR2)

RTCCR2 controls RTC periodic interrupts of weeks, days, hours, minutes, and seconds. Enabling interrupts of weeks, days, hours, minutes, and seconds sets the IRRTA flag to 1 in the interrupt flag register 1 (IRR1) when an interrupt occurs. It also controls an overflow interrupt of a free running counter when RTC operates as a free running counter.

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	—	Reserved These bits are always read as 0.
5	FOIE	—	R/W	Free Running Counter Overflow Interrupt Enable 0: Disables an overflow interrupt 1: Enables an overflow interrupt
4	WKIE	—	R/W	Week Periodic Interrupt Enable 0: Disables a week periodic interrupt 1: Enables a week periodic interrupt
3	DYIE	—	R/W	Day Periodic Interrupt Enable 0: Disables a day periodic interrupt 1: Enables a day periodic interrupt
2	HRIE	—	R/W	Hour Periodic Interrupt Enable 0: Disables an hour periodic interrupt 1: Enables an hour periodic interrupt
1	MNIE	—	R/W	Minute Periodic Interrupt Enable 0: Disables a minute periodic interrupt 1: Enables a minute periodic interrupt
0	SEIE	—	R/W	Second Periodic Interrupt Enable 0: Disables a second periodic interrupt 1: Enables a second periodic interrupt

11.3.3 Timer Load Register B1 (TLB1)

TLB1 is an 8-bit write-only register for setting the reload value of TCB1. When a reload value is set in TLB1, the same value is loaded into TCB1 as well, and TCB1 starts counting up from that value. When TCB1 overflows during operation in auto-reload mode, the TLB1 value is loaded into TCB1. Accordingly, overflow periods can be set within the range of 1 to 256 input clocks. TLB1 is allocated to the same address as TCB1. TLB1 is initialized to H'00.

11.4 Operation

11.4.1 Interval Timer Operation

When bit TMB17 in TMB1 is cleared to 0, timer B1 functions as an 8-bit interval timer. Upon reset, TCB1 is cleared to H'00 and bit TMB17 is cleared to 0, so up-counting and interval timing resume immediately. The operating clock of timer B1 is selected from seven internal clock signals output by prescaler S, or an external clock input at pin TMB1. The selection is made by bits TMB12 to TMB10 in TMB1.

After the count value in TMB1 reaches H'FF, the next clock signal input causes timer B1 to overflow, setting flag IRRTB1 in IRR2 to 1. If IENTB1 in IENR2 is 1, an interrupt is requested to the CPU.

At overflow, TCB1 returns to H'00 and starts counting up again. During interval timer operation (TMB17 = 0), when a value is set in TLB1, the same value is set in TCB1.

11.4.2 Auto-Reload Timer Operation

Setting bit TMB17 in TMB1 to 1 causes timer B1 to function as an 8-bit auto-reload timer. When a reload value is set in TLB1, the same value is loaded into TCB1, becoming the value from which TCB1 starts its count. After the count value in TCB1 reaches H'FF, the next clock signal input causes timer B1 to overflow. The TLB1 value is then loaded into TCB1, and the count continues from that value. The overflow period can be set within a range from 1 to 256 input clocks, depending on the TLB1 value.

The clock sources and interrupts in auto-reload mode are the same as in interval mode. In auto-reload mode (TMB17 = 1), when a new value is set in TLB1, the TLB1 value is also loaded into TCB1.

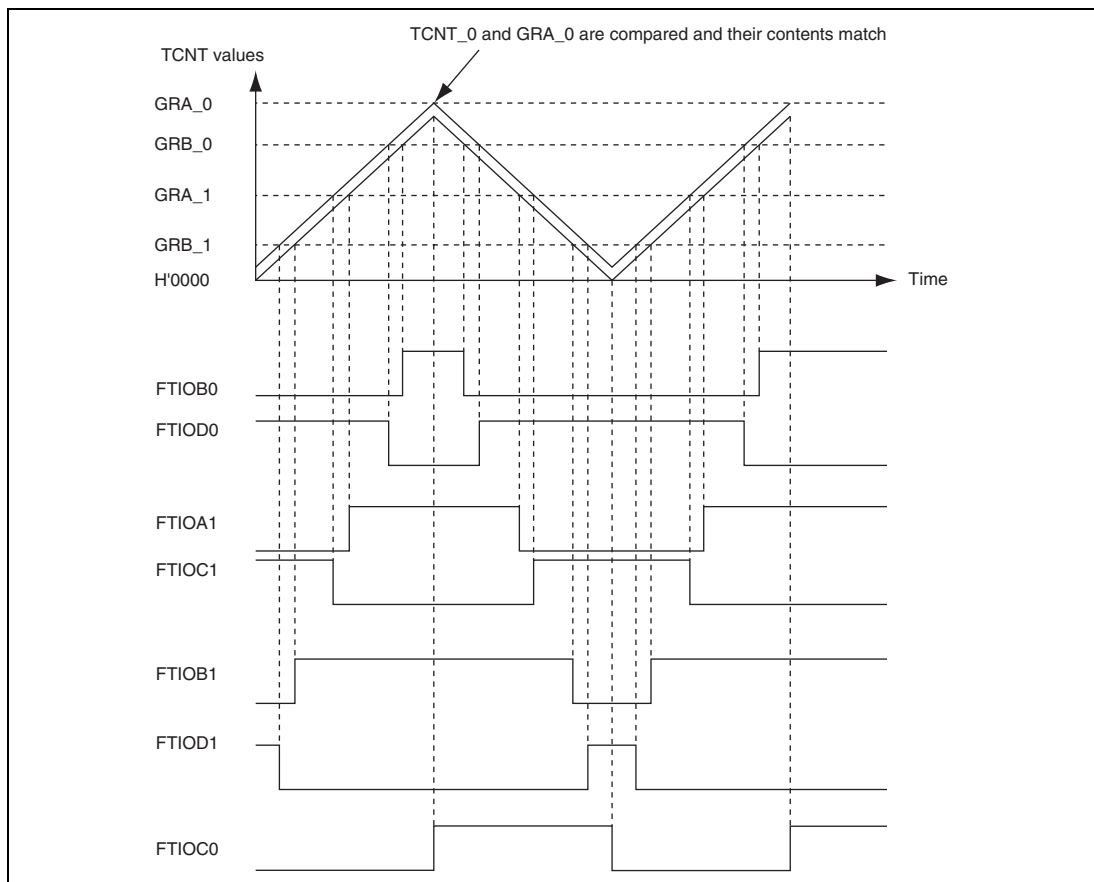


Figure 13.31 Example of Complementary PWM Mode Operation (1)

Figure 13.32 (1) and (2) show examples of PWM waveform output with 0% duty and 100% duty in complementary PWM mode (for one phase).

- $TPSC2 = TPSC1 = TPSC0 = 0$

Set GRB_0 to H'0000 or a value equal to or more than GRA_0. The waveform with a duty cycle of 0% and 100% can be output. When buffer operation is used together, the duty cycles can easily be changed, including the above settings, during operation. For details on buffer operation, refer to section 13.4.8, Buffer Operation.

- Other than $TPSC2 = TPSC1 = TPSC0 = 0$

Set GRB_0 to satisfy the following expression: $GRA_0 + 1 < GRB_0 < H'FFFF$. The waveform with a duty cycle of 0% and 100% can be output. For details on 0%- and 100%-duty cycle waveform output, see 3. C., Outputting a waveform with a duty cycle of 0% and 100% in section 13.4.7.

6. Examples of Buffer Operation

Figure 13.38 shows an operation example in which GRA has been designated as an output compare register, and buffer operation has been designated for GRA and GRC.

This is an example of TCNT operating as a periodic counter cleared by compare match B.

Pins FTIOA and FTIOB are set for toggle output by compare match A and B.

As buffer operation has been set, when compare match A occurs, the FTIOA pin performs toggle outputs and the value in buffer register is simultaneously transferred to the general register. This operation is repeated each time that compare match A occurs.

The timing to transfer data is shown in figure 13.39.

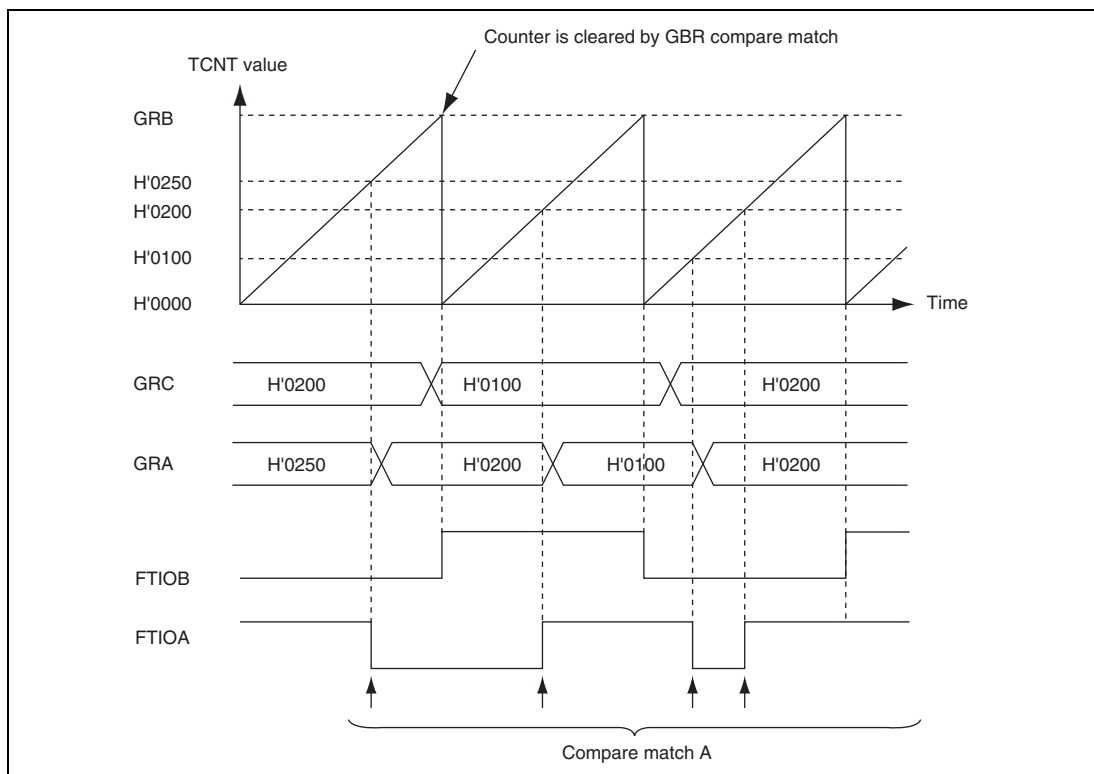


Figure 13.38 Example of Buffer Operation (1)
(Buffer Operation for Output Compare Register)

14.3 Operation

The watchdog timer is provided with an 8-bit counter. If 1 is written to WDON while writing 0 to B2WI when the TCSRWE bit in TCSRWD is set to 1, TCWD begins counting up. (To operate the watchdog timer, two write accesses to TCSRWD are required.) When a clock pulse is input after the TCWD count value has reached H'FF, the watchdog timer overflows and an internal reset signal is generated. The internal reset signal is output for a period of $256 \phi_{osc}$ clock cycles. TCWD is a writable counter, and when a value is set in TCWD, the count-up starts from that value. An overflow period in the range of 1 to 256 input clock cycles can therefore be set, according to the TCWD set value.

Figure 14.2 shows an example of watchdog timer operation.

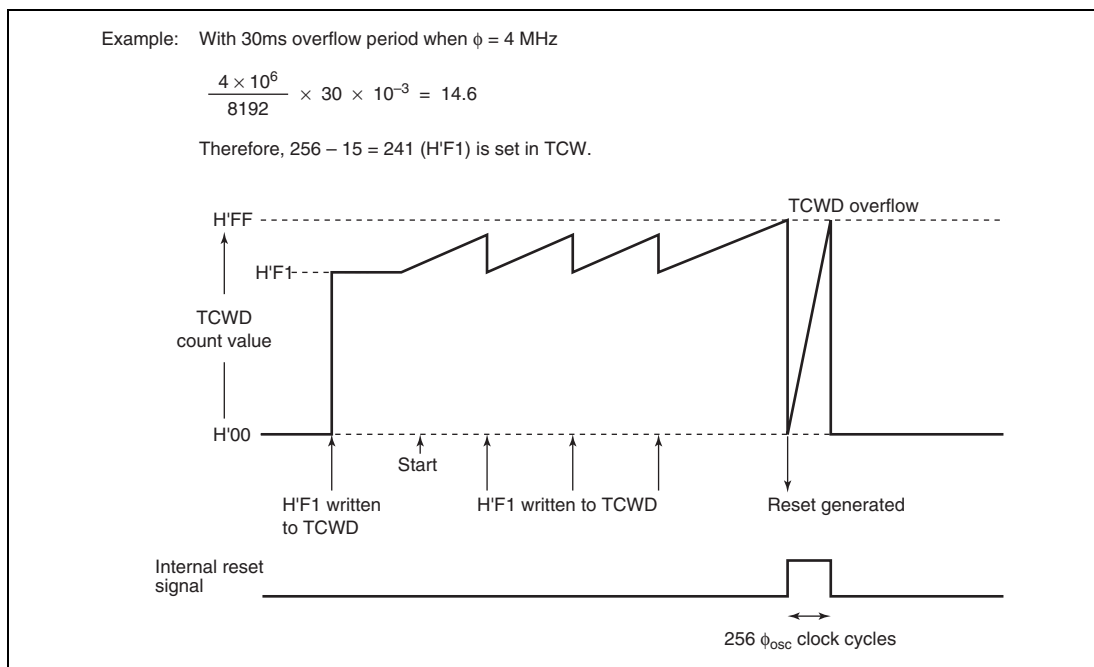


Figure 14.2 Watchdog Timer Operation Example

Table 16.4 Maximum Bit Rate for Each Frequency (Asynchronous Mode)

ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N	ϕ (MHz)	Maximum Bit Rate (bit/s)	n	N
2	62500	0	0	8	250000	0	0
2.097152	65536	0	0	9.8304	307200	0	0
2.4576	76800	0	0	10	312500	0	0
3	93750	0	0	12	375000	0	0
3.6864	115200	0	0	12.288	384000	0	0
4	125000	0	0	14	437500	0	0
4.9152	153600	0	0	14.7456	460800	0	0
5	156250	0	0	16	500000	0	0
6	187500	0	0	17.2032	537600	0	0
6.144	192000	0	0	18	562500	0	0
7.3728	230400	0	0	20	625000	0	0

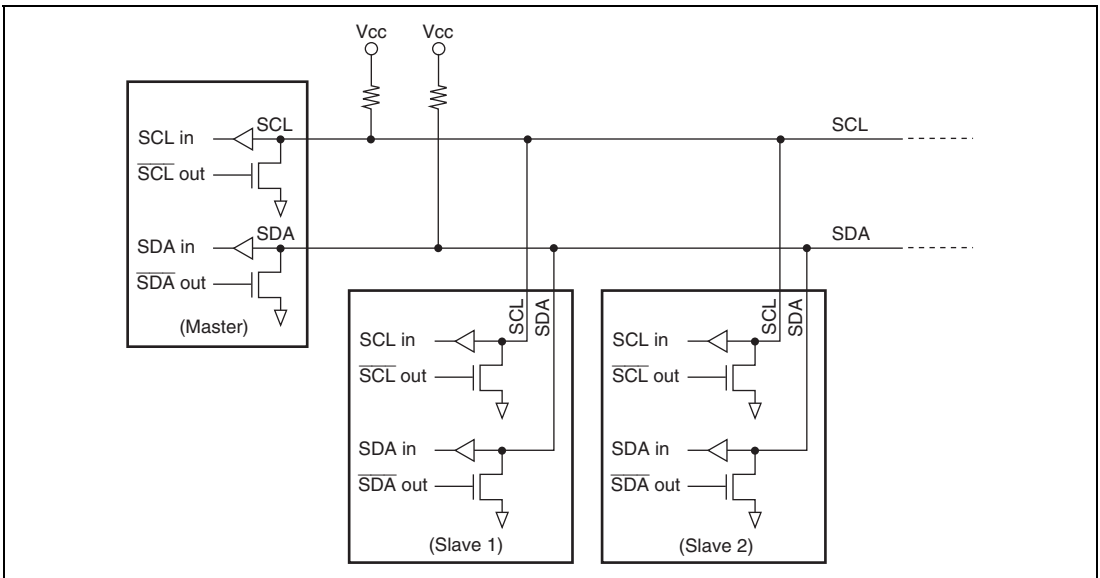


Figure 17.2 External Circuit Connections of I/O Pins

17.2 Input/Output Pins

Table 17.1 summarizes the input/output pins used by the I²C bus interface 2.

Table 17.1 I²C Bus Interface Pins

Name	Abbreviation	I/O	Function
Serial clock	SCL	I/O	IIC serial clock input/output
Serial data	SDA	I/O	IIC serial data input/output

17.3 Register Descriptions

The I²C bus interface 2 has the following registers:

- I²C bus control register 1 (ICCR1)
- I²C bus control register 2 (ICCR2)
- I²C bus mode register (ICMR)
- I²C bus interrupt enable register (ICIER)
- I²C bus status register (ICSR)
- I²C bus slave address register (SAR)
- I²C bus transmit data register (ICDRT)

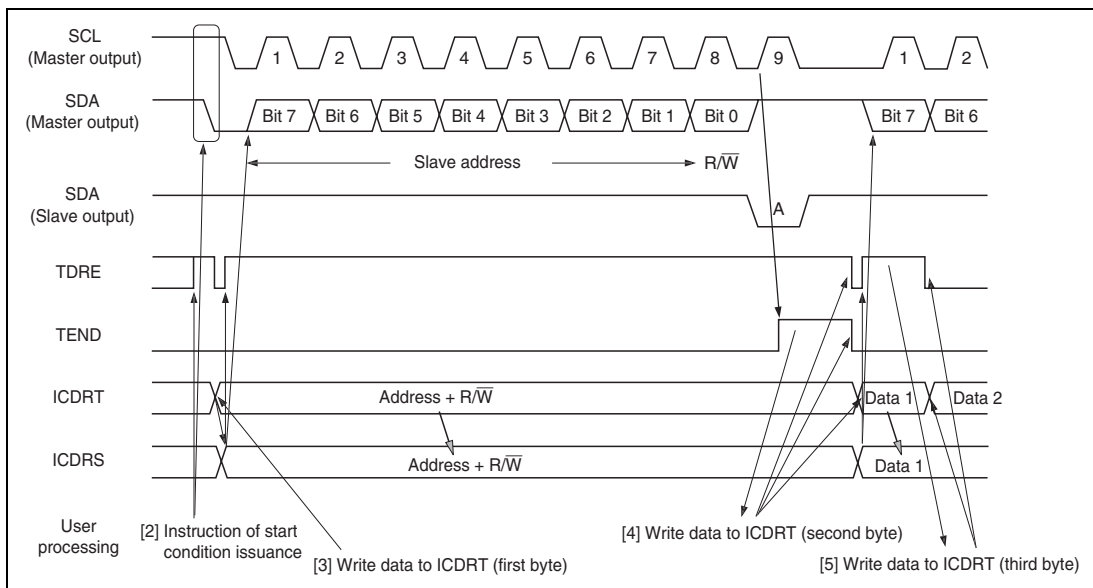


Figure 17.5 Master Transmit Mode Operation Timing (1)

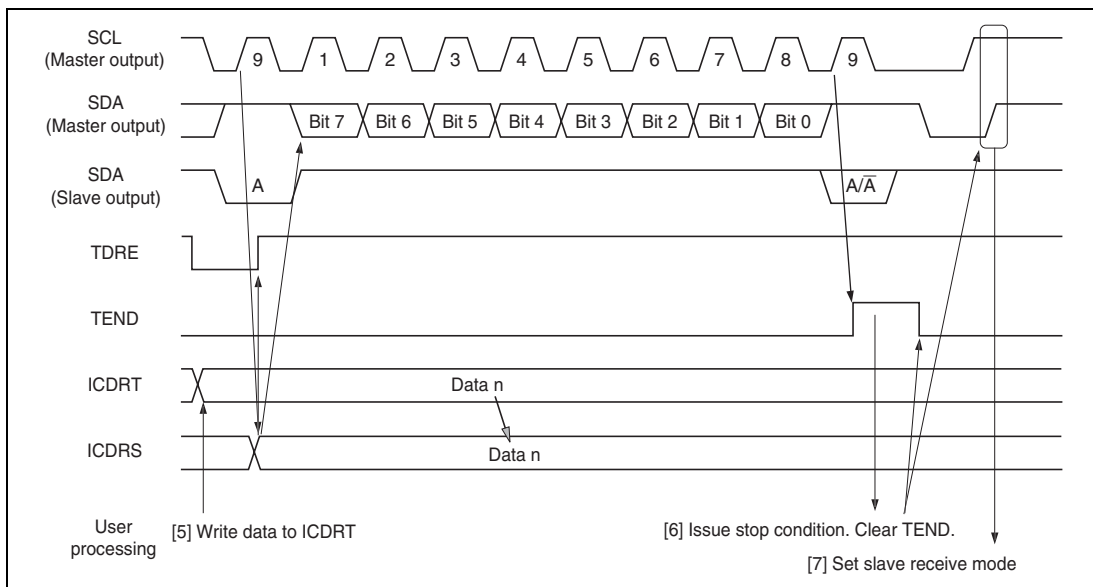


Figure 17.6 Master Transmit Mode Operation Timing (2)

22.3 Registers States in Each Operating Mode

Register Name	Reset	Active	Sleep	Subactive	Subsleep	Standby	Module
TCR_0	Initialized	—	—	—	—	—	Timer Z
TIORA_0	Initialized	—	—	—	—	—	
TIORC_0	Initialized	—	—	—	—	—	
TSR_0	Initialized	—	—	—	—	—	
TIER_0	Initialized	—	—	—	—	—	
POCR_0	Initialized	—	—	—	—	—	
TCNT_0	Initialized	—	—	—	—	—	
GRA_0	Initialized	—	—	—	—	—	
GRB_0	Initialized	—	—	—	—	—	
GRC_0	Initialized	—	—	—	—	—	
GRD_0	Initialized	—	—	—	—	—	
TCR_1	Initialized	—	—	—	—	—	
TIORA_1	Initialized	—	—	—	—	—	
TIORC_1	Initialized	—	—	—	—	—	
TSR_1	Initialized	—	—	—	—	—	
TIER_1	Initialized	—	—	—	—	—	
POCR_1	Initialized	—	—	—	—	—	
TCNT_1	Initialized	—	—	—	—	—	
GRA_1	Initialized	—	—	—	—	—	
GRB_1	Initialized	—	—	—	—	—	
GRC_1	Initialized	—	—	—	—	—	
GRD_1	Initialized	—	—	—	—	—	
TSTR	Initialized	—	—	—	—	—	RTC
TMDR	Initialized	—	—	—	—	—	
TPMR	Initialized	—	—	—	—	—	
TFCR	Initialized	—	—	—	—	—	
TOER	Initialized	—	—	—	—	—	
TOCR	Initialized	—	—	—	—	—	
RSECDR	—	—	—	—	—	—	

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
Input low voltage	V_{IL}	RXD, RXD_2, SCL, SDA, P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87, PB0 to PB7	$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$	-0.3	—	$V_{CC} \times 0.3$	V	
				-0.3	—	$V_{CC} \times 0.2$	V	
		OSC1	$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$	-0.3	—	0.5	V	
				-0.3	—	0.3		
Output high voltage	V_{OH}	P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P55, P60 to P67, P70 to P72, P74 to P76, P85 to P87,	$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$ $-I_{OH} = 1.5 \text{ mA}$	$V_{CC} - 1.0$	—	—	V	
				$V_{CC} - 0.5$	—	—		
		P56, P57	$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$ $-I_{OH} = 0.1 \text{ mA}$	$V_{CC} - 2.5$	—	—	V	
				$V_{CC} - 2.0$	—	—		
Output low voltage	V_{OL}	P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P70 to P72, P74 to P76, P85 to P87	$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$ $I_{OL} = 1.6 \text{ mA}$	—	—	0.6	V	
				—	—	0.4		
		P60 to P67	$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$ $I_{OL} = 20.0 \text{ mA}$	—	—	1.5	V	
				—	—	1.0		
			$V_{CC} = 4.0 \text{ to } 5.5 \text{ V}$ $I_{OL} = 1.6 \text{ mA}$	—	—	0.4		
				—	—	0.4		

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
Output low voltage	V_{OL}	SCL, SDA	$V_{CC} = 4.0$ to 5.5 V	—	—	0.6	V	
			$I_{OL} = 6.0$ mA	—	—	0.4		
			$I_{OL} = 3.0$ mA	—	—	0.4		
Input/output leakage current	$ I_{IL} $	OSC1, TMIB1, RES, NMI, WKP0 to WKP5, IRQ0 to IRQ3, ADTRG, TRGV, TMRIV, TMCIV, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1 RXD, SCK3, RXD_2, SCK3_2, SCL, SDA	$V_{IN} = 0.5$ V to $(V_{CC} - 0.5$ V)	—	—	1.0	μ A	
		P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87,	$V_{IN} = 0.5$ V to $(V_{CC} - 0.5$ V)	—	—	1.0	μ A	
		PB0 to PB7	$V_{IN} = 0.5$ V to $(AV_{CC} - 0.5$ V)	—	—	1.0	μ A	
Pull-up MOS current	$-I_p$	P10 to P12, P14 to P17,	$V_{CC} = 5.0$ V, $V_{IN} = 0.0$ V	50.0	—	300.0	μ A	
		P50 to P55	$V_{CC} = 3.0$ V, $V_{IN} = 0.0$ V	—	60.0	—		Reference value
Input capacitance	C_{in}	All input pins except power supply pins	$f = 1$ MHz, $V_{IN} = 0.0$ V, $T_a = 25^\circ\text{C}$	—	—	15.0	pF	
Active mode current consumption	I_{OPE1}	V_{CC}	Active mode 1 $V_{CC} = 5.0$ V, $f_{OSC} = 20$ MHz	—	21.0	30.0	mA	*
			Active mode 1 $V_{CC} = 3.0$ V, $f_{OSC} = 10$ MHz	—	9.0	—		* Reference value
	I_{OPE2}	V_{CC}	Active mode 2 $V_{CC} = 5.0$ V, $f_{OSC} = 20$ MHz	—	1.8	3.0	mA	*
			Active mode 2 $V_{CC} = 3.0$ V, $f_{OSC} = 10$ MHz	—	1.2	—		* Reference value

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Reference
				Min	Typ	Max		
RES pin low width	t_{REL}	RES	At power-on and in modes other than those below	t_{rc}	—	—	ms	Figure 23.2
			In active mode and sleep mode operation	200	—	—	ns	
Input pin high width	t_{IH}	NMI, TMIB1, IRQ0 to IRQ3, WKP0 to WKP5, TMCIV, TMRIV, TRGV, ADTRG, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1		2	—	—	t_{cyc} t_{subcyc}	Figure 23.3
Input pin low width	t_{IL}	NMI, TMIB1, IRQ0 to IRQ3, WKP0 to WKP5, TMCIV, TMRIV, TRGV, ADTRG, FTIOA0 to FTIOD0, FTIOA1 to FTIOD1		2	—	—	t_{cyc} t_{subcyc}	

- Notes: 1. When an external clock is input, the minimum system clock oscillation frequency is 1.0 MHz.
2. Determined by MA2, MA1, MA0, SA1, and SA0 of system control register 2 (SYSCR2).

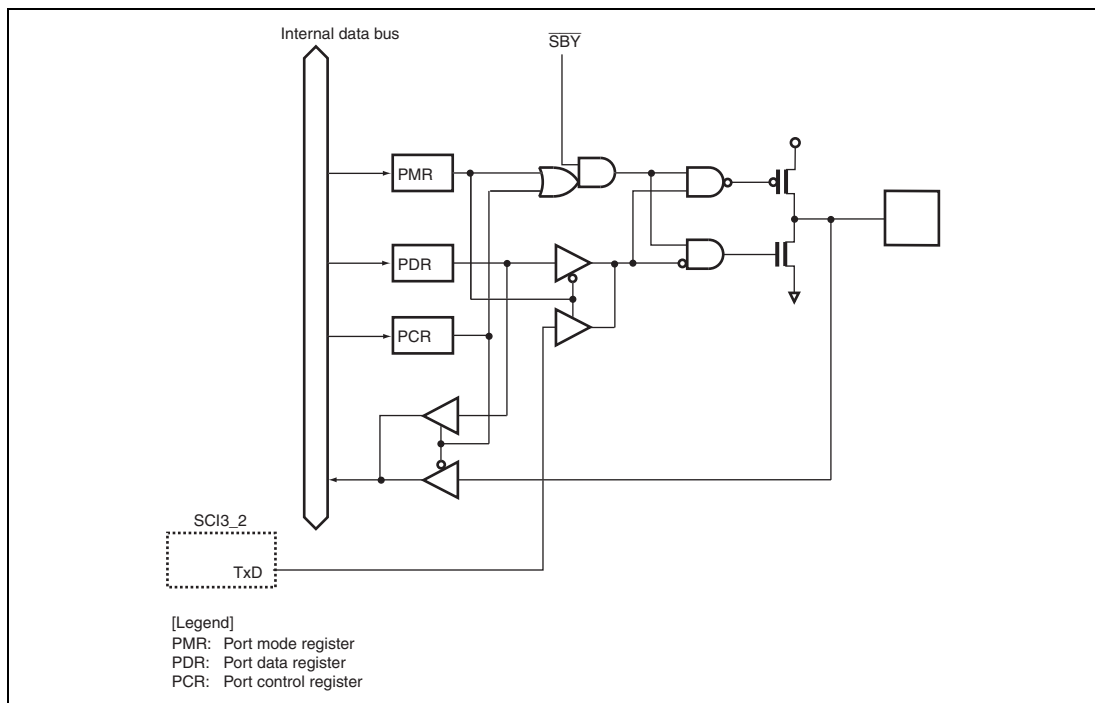


Figure B.19 Port 7 Block Diagram (P72)

