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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	H8/300H
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, SCI
Peripherals	PWM, WDT
Number of I/O	45
Program Memory Size	56KB (56K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 8x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LFQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/hd64f3687fpiv

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2.5 Addressing Modes and Effective Address Calculation

The following describes the H8/300H CPU. In this LSI, the upper eight bits are ignored in the generated 24-bit address, so the effective address is 16 bits.

2.5.1 Addressing Modes

The H8/300H CPU supports the eight addressing modes listed in table 2.10. Each instruction uses a subset of these addressing modes. Addressing modes that can be used differ depending on the instruction. For details, refer to appendix A.4, Combinations of Instructions and Addressing Modes.

Arithmetic and logic instructions can use the register direct and immediate modes. Data transfer instructions can use all addressing modes except program-counter relative and memory indirect. Bit-manipulation instructions use register direct, register indirect, or the absolute addressing mode (@aa:8) to specify an operand, and register direct (BSET, BCLR, BNOT, and BTST instructions) or immediate (3-bit) addressing mode to specify a bit number in the operand.

Table 2.10 Addressing Modes

No.	Addressing Mode	Symbol
1	Register direct	Rn
2	Register indirect	@ERn
3	Register indirect with displacement	@(d:16,ERn)/@(d:24,ERn)
4	Register indirect with post-increment Register indirect with pre-decrement	@ERn+ @-ERn
5	Absolute address	@aa:8/@aa:16/@aa:24
6	Immediate	#xx:8/#xx:16/#xx:32
7	Program-counter relative	@(d:8,PC)/@(d:16,PC)
8	Memory indirect	@@aa:8

Register Direct—Rn

The register field of the instruction specifies an 8-, 16-, or 32-bit general register containing the operand. R0H to R7H and R0L to R7L can be specified as 8-bit registers. R0 to R7 and E0 to E7 can be specified as 16-bit registers. ER0 to ER7 can be specified as 32-bit registers.

5.2.2 Pin Connection when Not Using Subclock

When the subclock is not used, connect pin X_1 to V_{CL} or V_{SS} and leave pin X_2 open, as shown in figure 5.10.

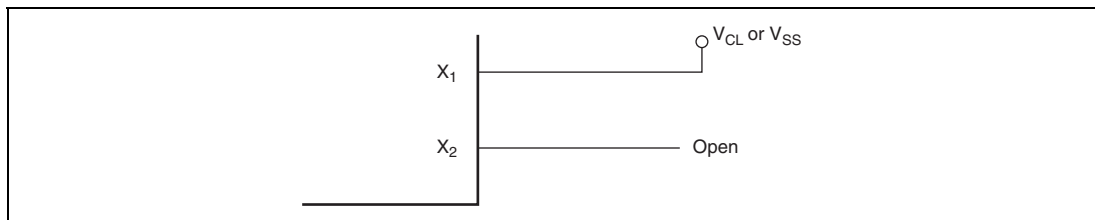


Figure 5.10 Pin Connection when not Using Subclock

5.3 Prescalers

5.3.1 Prescaler S

Prescaler S is a 13-bit counter using the system clock (ϕ) as its input clock. It is incremented once per clock period. Prescaler S is initialized to H'0000 by a reset, and starts counting on exit from the reset state. In standby mode, subactive mode, and subsleep mode, the system clock pulse generator stops. Prescaler S also stops and is initialized to H'0000. The CPU cannot read or write prescaler S. The output from prescaler S is shared by the on-chip peripheral modules. The divider ratio can be set separately for each on-chip peripheral function. In active mode and sleep mode, the clock input to prescaler S is determined by the division factor designated by MA2 to MA0 in SYSCR2.

5.3.2 Prescaler W

Prescaler W is a 5-bit counter using a 32.768 kHz signal divided by 4 ($\phi_w/4$) as its input clock. The divided output is used for clock time base operation of timer A. Prescaler W is initialized to H'00 by a reset, and starts counting on exit from the reset state. Even in standby mode, subactive mode, or subsleep mode, prescaler W continues functioning so long as clock signals are supplied to pins X_1 and X_2 .

9.1.1 Port Mode Register 1 (PMR1)

PMR1 switches the functions of pins in port 1 and port 2.

Bit	Bit Name	Initial Value	R/W	Description
7	IRQ3	0	R/W	This bit selects the function of pin P17/ $\overline{\text{IRQ3}}$ /TRGV. 0: General I/O port 1: $\overline{\text{IRQ3}}$ /TRGV input pin
6	IRQ2	0	R/W	This bit selects the function of pin P16/ $\overline{\text{IRQ2}}$. 0: General I/O port 1: $\overline{\text{IRQ2}}$ input pin
5	IRQ1	0	R/W	This bit selects the function of pin P15/ $\overline{\text{IRQ1}}$ /TMIB1. 0: General I/O port 1: $\overline{\text{IRQ1}}$ /TMIB1 input pin
4	IRQ0	0	R/W	This bit selects the function of pin P14/ $\overline{\text{IRQ0}}$. 0: General I/O port 1: $\overline{\text{IRQ0}}$ input pin
3	TXD2	0	R/W	This bit selects the function of pin P72/TXD_2. 0: General I/O port 1: TXD_2 output pin
2	PWM	0	R/W	This bit selects the function of pin P11/PWM. 0: General I/O port 1: PWM output pin
1	TXD	0	R/W	This bit selects the function of pin P22/TXD. 0: General I/O port 1: TXD output pin
0	TMOW	0	R/W	This bit selects the function of pin P10/TMOW. 0: General I/O port 1: TMOW output pin

11.4.3 Event Counter Operation

Timer B1 can operate as an event counter in which TMIB1 is set to an event input pin. External event counting is selected by setting bits TMB12 to TMB10 in TMB1 to 1. TCB1 counts up at rising or falling edge of an external event signal input at pin TMB1.

When timer B1 is used to count external event input, bit IRQ1 in PMR1 should be set to 1 and IEN1 in IENR1 should be cleared to 0 to disable IRQ1 interrupt requests.

11.5 Timer B1 Operating Modes

Table 11.2 shows the timer B1 operating modes.

Table 11.2 Timer B1 Operating Modes

Operating Mode		Reset	Active	Sleep	Subactive	Subsleep	Standby
TCB1	Interval	Reset	Functions	Functions	Halted	Halted	Halted
	Auto-reload	Reset	Functions	Functions	Halted	Halted	Halted
TMB1		Reset	Functions	Retained	Retained	Retained	Retained

13.3.2 Timer Mode Register (TMDR)

TMDR selects buffer operation settings and synchronized operation.

Bit	Bit Name	Initial Value	R/W	Description
7	BFD1	0	R/W	Buffer Operation D1 0: GRD_1 operates normally 1: GRB_1 and GRD_1 are used together for buffer operation
6	BFC1	0	R/W	Buffer Operation C1 0: GRC_1 operates normally 1: GRA_1 and GRD_1 are used together for buffer operation
5	BFD0	0	R/W	Buffer Operation D0 0: GRD_0 operates normally 1: GRB_0 and GRD_0 are used together for buffer operation
4	BFC0	0	R/W	Buffer Operation C0 0: GRC_0 operates normally 1: GRA_0 and GRC_0 are used together for buffer operation
3 to 1	—	All 1	—	Reserved These bits are always read as 1, and cannot be modified.
0	SYNC	0	R/W	Timer Synchronization 0: TCNT_1 and TCNT_0 operate as a different timer 1: TCNT_1 and TCNT_0 are synchronized TCNT_1 and TCNT_0 can be pre-set or cleared synchronously

13.4.4 Synchronous Operation

In synchronous operation, the values in a number of TCNT counters can be rewritten simultaneously (synchronous presetting). Also, a number of TCNT counters can be cleared simultaneously by making the appropriate setting in TCR (synchronous clearing). Synchronous operation enables GR to be increased with respect to a single time base.

Figure 13.19 shows an example of the synchronous operation setting procedure.

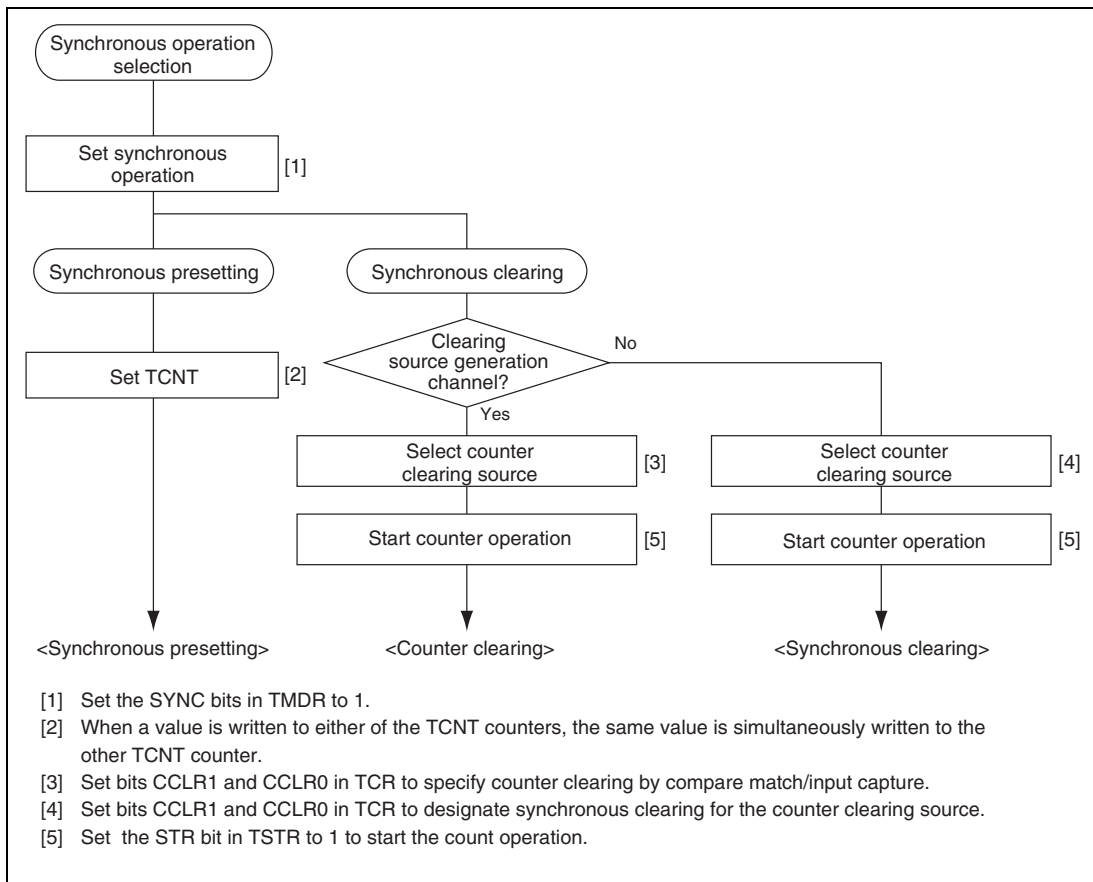


Figure 13.19 Example of Synchronous Operation Setting Procedure

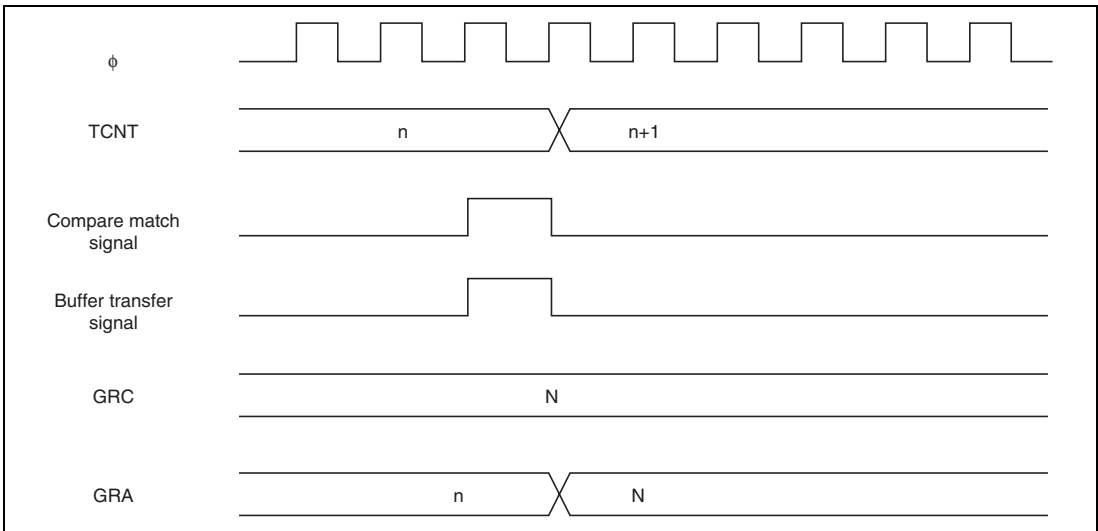


Figure 13.39 Example of Compare Match Timing for Buffer Operation

Figure 13.40 shows an operation example in which GRA has been designated as an input capture register, and buffer operation has been designated for GRA and GRC.

Counter clearing by input capture B has been set for TCNT, and falling edges have been selected as the FIOCB pin input capture input edge. And both rising and falling edges have been selected as the FIOCA pin input capture input edge.

As buffer operation has been set, when the TCNT value is stored in GRA upon the occurrence of input capture A, the value previously stored in GRA is simultaneously transferred to GRC. The transfer timing is shown in figure 13.41.

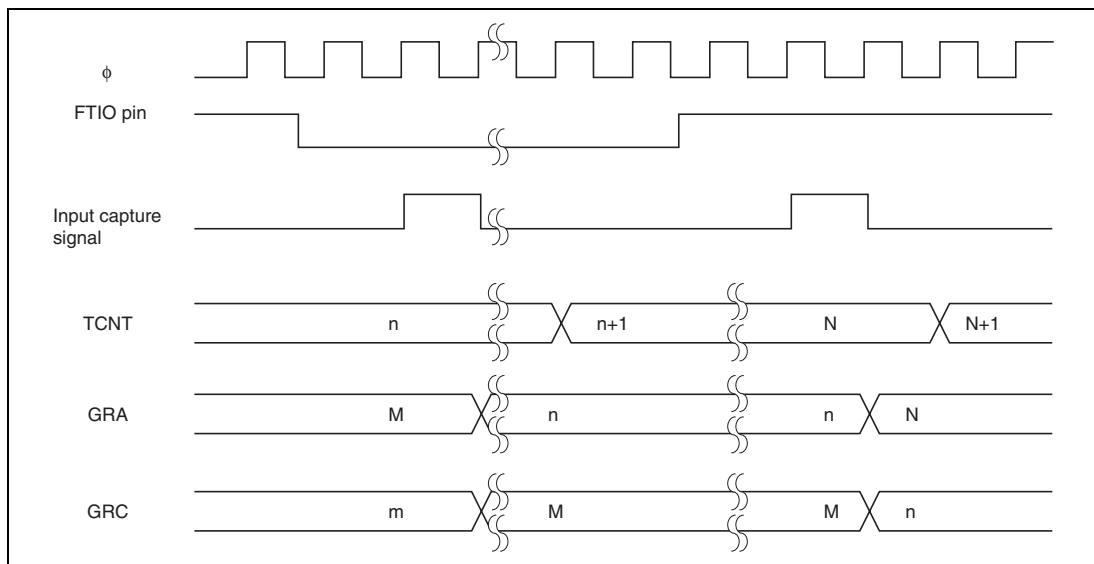


Figure 13.41 Input Capture Timing of Buffer Operation

Figures 13.42 and 13.43 show the operation examples when buffer operation has been designated for GRB_0 and GRD_0 in complementary PWM mode. These are examples when a PWM waveform of 0% duty is created by using the buffer operation and performing $\text{GRD}_0 \geq \text{GRA}_0$. Data is transferred from GRD_0 to GRB_0 according to the settings of CMD_0 and CMD_1 when TCNT_0 and GRA_0 are compared and their contents match or when TCNT_1 underflows. However, when $\text{GRD}_0 \geq \text{GRA}_0$, data is transferred from GRD_0 to GRB_0 when TCNT_1 underflows regardless of the setting of CMD_0 and CMD_1. When $\text{GRD}_0 = \text{H}'0000$, data is transferred from GRD_0 to GRB_0 when TCNT_0 and GRA_0 are compared and their contents match regardless of the settings of CMD_0 and CMD_1.

**Table 16.5 Examples of BRR Settings for Various Bit Rates (Clocked Synchronous Mode)
(2)**

Bit Rate (bit/s)	Operating Frequency ϕ (MHz)			
	18		20	
	n	N	n	N
110	—	—	—	—
250	—	—	—	—
500	3	140	3	155
1k	3	69	3	77
2.5k	2	112	2	124
5k	1	224	1	249
10k	1	112	1	124
25k	0	179	0	199
50k	0	89	0	99
100k	0	44	0	49
250k	0	17	0	19
500k	0	8	0	9
1M	0	4	0	4
2M	—	—	—	—
2.5M	—	—	0	1
4M	—	—	—	—

Legend:

Blank : No setting is available.

— : A setting is available but error occurs.

* : Continuous transfer is not possible.

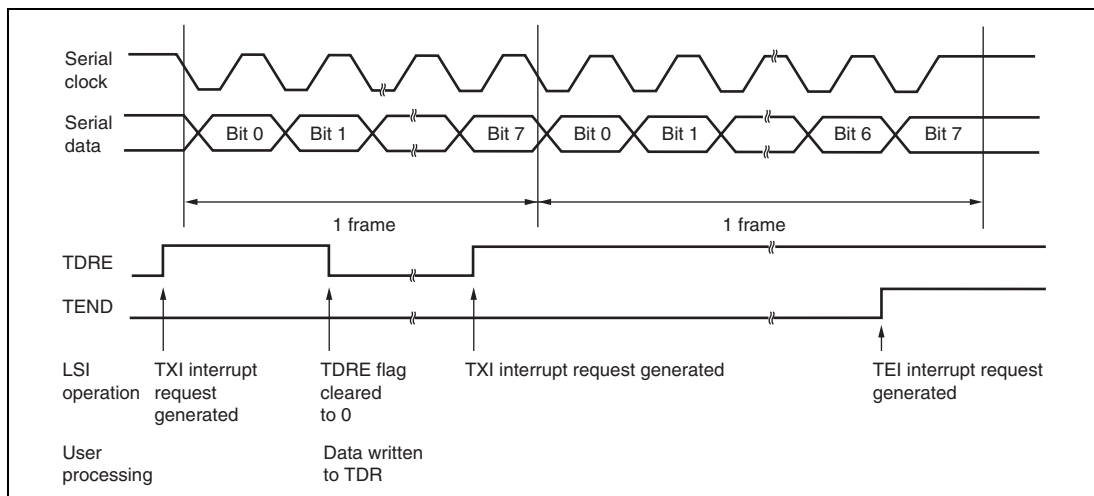


Figure 16.10 Example of SCI3 Transmission in Clocked Synchronous Mode

16.5.5 Simultaneous Serial Data Transmission and Reception

Figure 16.14 shows a sample flowchart for simultaneous serial transmit and receive operations. The following procedure should be used for simultaneous serial data transmit and receive operations. To switch from transmit mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished transmission and the TDRE and TEND flags are set to 1, clear TE to 0. Then simultaneously set TE and RE to 1 with a single instruction. To switch from receive mode to simultaneous transmit and receive mode, after checking that the SCI3 has finished reception, clear RE to 0. Then after checking that the RDRF and receive error flags (OER, FER, and PER) are cleared to 0, simultaneously set TE and RE to 1 with a single instruction.

17.3.7 I²C Bus Transmit Data Register (ICDRT)

ICDRT is an 8-bit readable/writable register that stores the transmit data. When ICDRT detects the space in the shift register (ICDRS), it transfers the transmit data which is written in ICDRT to ICDRS and starts transferring data. If the next transfer data is written to ICDRT during transferring data of ICDRS, continuous transfer is possible. If the MLS bit of ICMR is set to 1 and when the data is written to ICDRT, the MSB/LSB inverted data is read. The initial value of ICDRT is H'FF.

17.3.8 I²C Bus Receive Data Register (ICDRR)

ICDRR is an 8-bit register that stores the receive data. When data of one byte is received, ICDRR transfers the receive data from ICDRS to ICDRR and the next data can be received. ICDRR is a receive-only register, therefore the CPU cannot write to this register. The initial value of ICDRR is H'FF.

17.3.9 I²C Bus Shift Register (ICDRS)

ICDRS is a register that is used to transfer/receive data. In transmission, data is transferred from ICDRT to ICDRS and the data is sent from the SDA pin. In reception, data is transferred from ICDRS to ICDRR after data of one byte is received. This register cannot be read directly from the CPU.

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
GRB_1	GRB1H7	GRB1H6	GRB1H5	GRB1H4	GRB1H3	GRB1H2	GRB1H1	GRB1H0	Timer Z
	GRB1L7	GRB1L6	GRB1L5	GRB1L4	GRB1L3	GRB1L2	GRB1L1	GRB1L0	
GRC_1	GRC1H7	GRC1H6	GRC1H5	GRC1H4	GRC1H3	GRC1H2	GRC1H1	GRC1H0	
	GRC1L7	GRC1L6	GRC1L5	GRC1L4	GRC1L3	GRC1L2	GRC1L1	GRC1L0	
GRD_1	GRD1H7	GRD1H6	GRD1H5	GRD1H4	GRD1H3	GRD1H2	GRD1H1	GRD1H0	
	GRD1L7	GRD1L6	GRD1L5	GRD1L4	GRD1L3	GRD1L2	GRD1L1	GRD1L0	
TSTR	—	—	—	—	—	—	STR1	STR0	
TMDR	BFD1	BFC1	BFD0	BFC0	—	—	—	SYNC	
TPMR	—	PWMD1	PWMC1	PWMB1	—	PWMD0	PWMC0	PWMB0	
TFCR	—	STCLK	ADEG	ADTRG	OLS1	OLS0	CMD1	CMD0	
TOER	ED1	EC1	EB1	EA1	ED0	EC0	EB0	EA0	
TOCR	TOD1	TOC1	TOB1	TOA1	TOD0	TOC0	TOB0	TOA0	
RSECDR	BSY	SC12	SC11	SC10	SC03	SC02	SC01	SC00	RTC
RMINDR	BSY	MN12	MN11	MN10	MN03	MN02	MN01	MN00	
RHRDR	BSY	—	HR11	HR10	HR03	HR02	HR01	HR00	
RWKDR	BSY	—	—	—	—	WK2	WK1	WK0	
RTCCR1	RUN	12/24	PM	RST	—	—	—	—	
RTCCR2	—	—	FOIE	WKIE	DYIE	HRIE	MNIE	SEIE	
RTCCSR	—	RCS6	RCS5	—	RCS3	RCS2	RCS1	RCS0	
LVDCR	LVDE	—	—	—	LVDSEL	LVDRE	LVDDE	LVDUE	LVDC (optional)* ¹
LVDSR	—	—	—	—	—	—	LVDDF	LVDUF	
—	—	—	—	—	—	—	—	—	—
SMR_2	COM	CHR	PE	PM	STOP	MP	CKS1	CKS0	SCI3_2
BRR_2	BRR7	BRR6	BRR5	BRR4	BRR3	BRR2	BRR1	BRR0	
SCR3_2	TIE	RIE	TE	RE	MPIE	TEIE	CKE1	CKE0	
TDR_2	TDR7	TDR6	TDR5	TDR4	TDR3	TDR2	TDR1	TDR0	
SSR_2	TDRE	RDRF	OER	FER	PER	TEND	MPBR	MPBT	
RDR_2	RDR7	RDR6	RDR5	RDR4	RDR3	RDR2	RDR1	RDR0	
ICCR1	ICE	RCVD	MST	TRS	CKS3	CKS2	CKS1	CKS0	IIC2
ICCR2	BBSY	SCP	SDAO	SDAOP	SCLO	—	IICRST	—	
ICMR	MLS	WAIT	—	—	BCWP	BC2	BC1	BC0	

Register Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module Name
ADDRB	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	A/D converter
	AD1	AD0	—	—	—	—	—	—	
ADDRC	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADDRD	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	
	AD1	AD0	—	—	—	—	—	—	
ADCSR	ADF	ADIE	ADST	SCAN	CKS	CH2	CH1	CH0	
ADCR	TRGE	—	—	—	—	—	—	—	
—	—	—	—	—	—	—	—	—	—
PWDRL	PWDRL7	PWDRL6	PWDRL5	PWDRL4	PWDRL3	PWDRL2	PWDRL1	PWDRL0	14-bit PWM
PWDRU	—	—	PWDRU5	PWDRU4	PWDRU3	PWDRU2	PWDRU1	PWDRU0	
PWCR	—	—	—	—	—	—	—	PWCR0	
TCSRWD	B6WI	TCWE	B4WI	TCSRWE	B2WI	WDON	B0WI	WRST	WDT* ²
TCWD	TCWD7	TCWD6	TCWD5	TCWD4	TCWD3	TCWD2	TCWD1	TCWD0	
TMWD	—	—	—	—	CKS3	CKS2	CKS1	CKS0	
—	—	—	—	—	—	—	—	—	—
ABRKCR	RTINTE	CSEL1	CSEL0	ACMP2	ACMP1	ACMP0	DCMP1	DCMP0	Address break
ABRSR	ABIF	ABIE	—	—	—	—	—	—	
BARH	BARH7	BARH6	BARH5	BARH4	BARH3	BARH2	BARH1	BARH0	
BARL	BARL7	BARL6	BARL5	BARL4	BARL3	BARL2	BARL1	BARL0	
BDRH	BDRH7	BDRH6	BDRH5	BDRH4	BDRH3	BDRH2	BDRH1	BDRH0	
BDRL	BDRL7	BDRL6	BDRL5	BDRL4	BDRL3	BDRL2	BDRL1	BDRL0	
—	—	—	—	—	—	—	—	—	—
PUCR1	PUCR17	PUCR16	PUCR15	PUCR14	—	PUCR12	PUCR11	PUCR10	I/O port
PUCR5	—	—	PUCR55	PUCR54	PUCR53	PUCR52	PUCR51	PUCR50	
PDR1	P17	P16	P15	P14	—	P12	P11	P10	
PDR2	—	—	—	P24	P23	P22	P21	P20	
PDR3	P37	P36	P35	P34	P33	P32	P31	P30	
PDR5	P57* ³	P56* ³	P55	P54	P53	P52	P51	P50	
PDR6	P67	P66	P65	P64	P63	P62	P61	P60	
PDR7	—	P76	P75	P74	—	P72	P71	P70	

Item	Symbol	Applicable Pins	Test Condition	Values			Unit	Notes
				Min	Typ	Max		
Input low voltage	V_{IL}	RXD, RXD _{_2} , SCL, SDA, P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P60 to P67, P70 to P72, P74 to P76, P85 to P87, PB0 to PB7	$V_{CC} = 4.0$ to 5.5 V	-0.3	—	$V_{CC} \times 0.3$	V	
				-0.3	—	$V_{CC} \times 0.2$	V	
		OSC1	$V_{CC} = 4.0$ to 5.5 V	-0.3	—	0.5	V	
				-0.3	—	0.3		
Output high voltage	V_{OH}	P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P55, P60 to P67, P70 to P72, P74 to P76, P85 to P87,	$V_{CC} = 4.0$ to 5.5 V $-I_{OH} = 1.5$ mA	$V_{CC} - 1.0$	—	—	V	
				$V_{CC} - 0.5$	—	—		
		P56, P57	$V_{CC} = 4.0$ to 5.5 V $-I_{OH} = 0.1$ mA	$V_{CC} - 2.5$	—	—	V	
				$V_{CC} - 2.0$	—	—		
Output low voltage	V_{OL}	P10 to P12, P14 to P17, P20 to P24, P30 to P37, P50 to P57, P70 to P72, P74 to P76, P85 to P87	$V_{CC} = 4.0$ to 5.5 V $I_{OL} = 1.6$ mA	—	—	0.6	V	
				—	—	0.4		
		P60 to P67	$V_{CC} = 4.0$ to 5.5 V $I_{OL} = 20.0$ mA	—	—	1.5	V	
				—	—	1.0		
			$V_{CC} = 4.0$ to 5.5 V $I_{OL} = 1.6$ mA	—	—	0.4		
				—	—	0.4		

A.4 Combinations of Instructions and Addressing Modes

Table A.5 Combinations of Instructions and Addressing Modes

Functions	Instructions	Addressing Mode											
		#xx	Rn	@ERn	@(d:16.ERn)	@(d:24.ERn)	@ERn+/@ERn	@aa:8	@aa:16	@aa:24	@(d:8.PC)	@(d:16.PC)	@@aa:8
Data transfer instructions	MOV	BWL	BWL	BWL	BWL	BWL	BWL	B	BWL	BWL	—	—	—
	POP, PUSH	—	—	—	—	—	—	—	—	—	—	—	WL
	MOVFP, MOVTPE	—	—	—	—	—	—	—	—	—	—	—	—
Arithmetic operations	ADD, CMP	BWL	BWL	—	—	—	—	—	—	—	—	—	—
	SUB	WL	BWL	—	—	—	—	—	—	—	—	—	—
	ADDX, SUBX	B	B	—	—	—	—	—	—	—	—	—	—
	ADDS, SUBS	—	L	—	—	—	—	—	—	—	—	—	—
	INC, DEC	—	BWL	—	—	—	—	—	—	—	—	—	—
	DAA, DAS	—	B	—	—	—	—	—	—	—	—	—	—
	MULXU, MULXS, DIVXU, DIVXS	—	BW	—	—	—	—	—	—	—	—	—	—
	NEG	—	BWL	—	—	—	—	—	—	—	—	—	—
	EXTU, EXTS	—	WL	—	—	—	—	—	—	—	—	—	—
Logical operations	AND, OR, XOR	—	BWL	—	—	—	—	—	—	—	—	—	—
	NOT	—	BWL	—	—	—	—	—	—	—	—	—	—
Shift operations		—	BWL	—	—	—	—	—	—	—	—	—	—
Bit manipulations		—	B	B	—	—	—	B	—	—	—	—	—
Branching instructions	BCC, BSR	—	—	—	—	—	—	—	—	—	—	—	—
	JMP, JSR	—	—	○	—	—	—	—	—	—	○	○	—
	RTS	—	—	—	—	—	—	—	—	○	—	—	○
System control instructions	TRAPA	—	—	—	—	—	—	—	—	—	—	—	○
	RTE	—	—	—	—	—	—	—	—	—	—	—	○
	SLEEP	—	—	—	—	—	—	—	—	—	—	—	○
	LDC	B	B	W	W	W	W	—	W	W	—	—	○
	STC	—	B	W	W	W	W	—	W	W	—	—	—
	ANDC, ORC, XORC	B	—	—	—	—	—	—	—	—	—	—	—
	NOP	—	—	—	—	—	—	—	—	—	—	—	○
Block data transfer instructions		—	—	—	—	—	—	—	—	—	—	—	BW

Appendix C Product Code Lineup

Product Classification			Product Code	Model Marking	Package Code
H8/3687	Flash memory version	Standard product	HD64F3687H	HD64F3687H	QFP-64 (FP-64A)
			HD64F3687FP	HD64F3687FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD64F3687GH	HD64F3687GH	QFP-64 (FP-64A)
			HD64F3687GFP	HD64F3687GFP	LQFP-64 (FP-64E)
	Mask ROM version	Standard product	HD6433687H	HD6433687(***)H	QFP-64 (FP-64A)
			HD6433687FP	HD6433687(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433687GH	HD6433687G(***)H	QFP-64 (FP-64A)
			HD6433687GFP	HD6433687G(***)FP	LQFP-64 (FP-64E)
H8/3686	Mask ROM version	Standard product	HD6433686H	HD6433686(***)H	QFP-64 (FP-64A)
			HD6433686FP	HD6433686(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433686GH	HD6433686G(***)H	QFP-64 (FP-64A)
			HD6433686GFP	HD6433686G(***)FP	LQFP-64 (FP-64E)
H8/3685	Mask ROM version	Standard product	HD6433685H	HD6433685(***)H	QFP-64 (FP-64A)
			HD6433685FP	HD6433685(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433685GH	HD6433685G(***)H	QFP-64 (FP-64A)
			HD6433685GFP	HD6433685G(***)FP	LQFP-64 (FP-64E)
H8/3684	Flash memory version	Standard product	HD64F3684H	HD64F3684H	QFP-64 (FP-64A)
			HD64F3684FP	HD64F3684FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD64F3684GH	HD64F3684GH	QFP-64 (FP-64A)
			HD64F3684GFP	HD64F3684GFP	LQFP-64 (FP-64E)
	Mask ROM version	Standard product	HD6433684H	HD6433684(***)H	QFP-64 (FP-64A)
			HD6433684FP	HD6433684(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433684GH	HD6433684G(***)H	QFP-64 (FP-64A)
			HD6433684GFP	HD6433684G(***)FP	LQFP-64 (FP-64E)
H8/3683	Mask ROM version	Standard product	HD6433683H	HD6433683(***)H	QFP-64 (FP-64A)
			HD6433683FP	HD6433683(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433683GH	HD6433683G(***)H	QFP-64 (FP-64A)
			HD6433683GFP	HD6433683G(***)FP	LQFP-64 (FP-64E)
H8/3682	Mask ROM version	Standard product	HD6433682H	HD6433682(***)H	QFP-64 (FP-64A)
			HD6433682FP	HD6433682(***)FP	LQFP-64 (FP-64E)
		Product with POR & LVDC	HD6433682GH	HD6433682G(***)H	QFP-64 (FP-64A)
			HD6433682GFP	HD6433682G(***)FP	LQFP-64 (FP-64E)

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