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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2371rvfq34v

Bit	Bit Name	Initial Value	R/W	Description
1	V	Undefined	R/W	Overflow Flag Set to 1 when an arithmetic overflow occurs, and cleared to 0 otherwise.
0	C	Undefined	R/W	Carry Flag Set to 1 when a carry occurs, and cleared to 0 otherwise. Used by: • Add instructions, to indicate a carry • Subtract instructions, to indicate a borrow • Shift and rotate instructions, to indicate a carry The carry flag is also used as a bit accumulator by bit manipulation instructions.

2.4.5 Initial Register Values

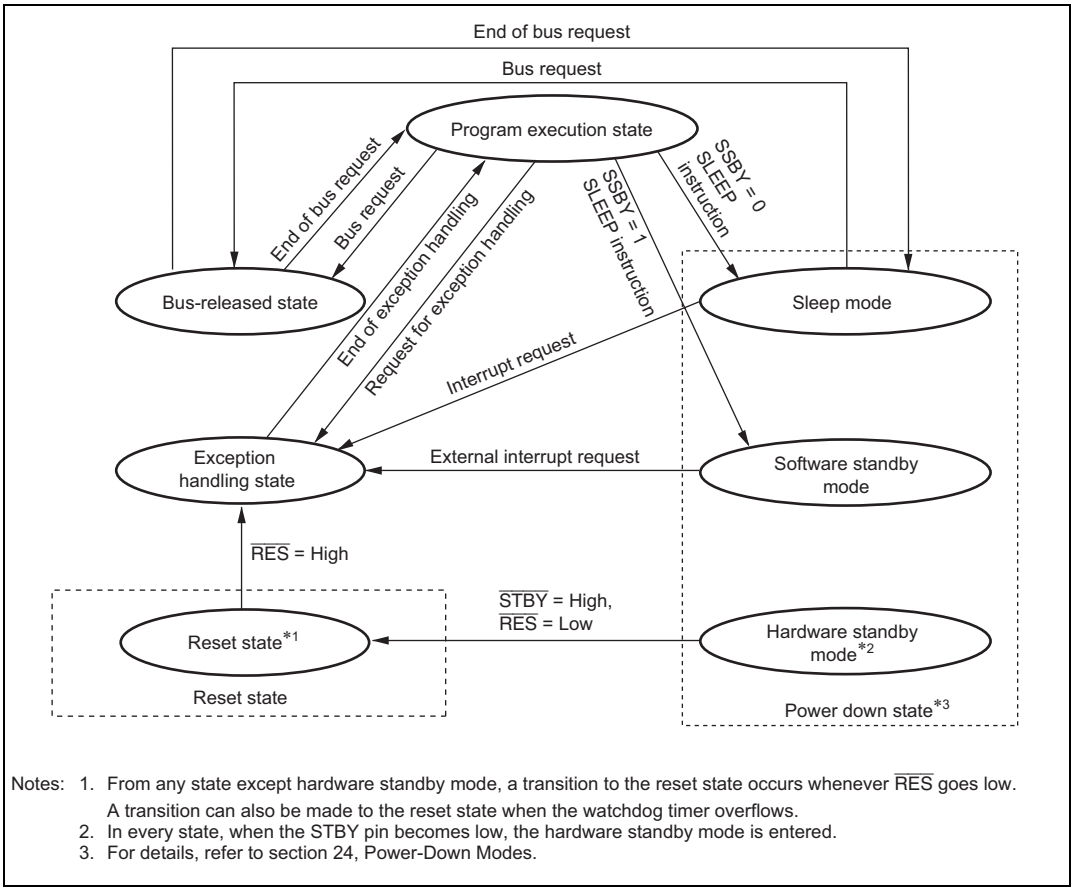
Reset exception handling loads the CPU's program counter (PC) from the vector table, clears the trace (T) bit in EXR to 0, and sets the interrupt mask (I) bits in CCR and EXR to 1. The other CCR bits and the general registers are not initialized. Note that the stack pointer (ER7) is undefined. The stack pointer should therefore be initialized by an MOV.L instruction executed immediately after a reset.

2.5 Data Formats

The H8S/2000 CPU can process 1-bit, 4-bit BCD, 8-bit (byte), 16-bit (word), and 32-bit (longword) data. Bit-manipulation instructions operate on 1-bit data by accessing bit n (n = 0, 1, 2, …, 7) of byte operand data. The DAA and DAS decimal-adjust instructions treat byte data as two digits of 4-bit BCD data.

No	Addressing Mode and Instruction Format	Effective Address Calculation	Effective Address (EA)
5	Absolute address @aa:8 op abs @aa:16 op abs @aa:24 op abs @aa:32 op abs		31 24 23 8 7 0 Don't care H'FFFF 31 24 23 16 15 0 Don't care Sign extension 31 24 23 0 Don't care 31 24 23 0 Don't care
6	Immediate #xx:8/#xx:16/#xx:32 op IMM		Operand is immediate data.
7	Program-counter relative @(d:8,PC)/@(d:16,PC) op disp	23 0 PC contents 23 0 Sign extension disp	31 24 23 0 Don't care
8	Memory indirect @@aa:8 • Normal mode* op abs • Advanced mode op abs	31 8 7 0 H'000000 abs 15 0 Memory contents 31 8 7 0 H'000000 abs 31 0 Memory contents	31 24 23 16 15 0 Don't care H'00 31 24 23 0 Don't care

Note: * For this LSI, normal mode is not available.



Notes: 1. From any state except hardware standby mode, a transition to the reset state occurs whenever $\overline{RES}$ goes low.
A transition can also be made to the reset state when the watchdog timer overflows.
2. In every state, when the STBY pin becomes low, the hardware standby mode is entered.
3. For details, refer to section 24, Power-Down Modes.

Figure 2.13 State Transitions

2.9 Usage Note

2.9.1 Note on Bit Manipulation Instructions

Bit manipulation instructions such as BSET, BCLR, BNOT, BST, and BIST read data in byte units, perform bit manipulation, and write data in byte units. Thus, care must be taken when these bit manipulation instructions are executed for a register or port including write-only bits.

In addition, the BCLR instruction can be used to clear the flag of an internal I/O register. In this case, if the flag to be cleared has been set by an interrupt processing routine, the flag need not be read before executing the BCLR instruction.

- WTCRBH

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0 and cannot be modified.
14 13 12	W32 W31 W30	1 1 1	R/W R/W R/W	Area 3 Wait Control 2 to 0 These bits select the number of program wait states when accessing area 3 while AST3 bit in ASTCR = 1. 000: Program wait not inserted 001: 1 program wait state inserted 010: 2 program wait states inserted 011: 3 program wait states inserted 100: 4 program wait states inserted 101: 5 program wait states inserted 110: 6 program wait states inserted 111: 7 program wait states inserted
11	—	0	R	Reserved This bit is always read as 0 and cannot be modified.

6.5.2 Valid Strobes

Table 6.3 shows the data buses used and valid strobes for the access spaces.

In a read, the $\overline{RD}$ signal is valid for both the upper and the lower half of the data bus. In a write, the $\overline{HWR}$ signal is valid for the upper half of the data bus, and the $\overline{LWR}$ signal for the lower half.

Table 6.3 Data Buses Used and Valid Strobes

Area	Access Size	Read/ Write	Address	Valid Strobe	Upper Data Bus (D15 to D8)	Lower Data Bus (D7 to D0)
8-bit access space	Byte	Read	—	$\overline{RD}$	Valid	Invalid
		Write	—	$\overline{HWR}$		Hi-Z
16-bit access space	Byte	Read	Even	$\overline{RD}$	Valid	Invalid
			Odd		Invalid	Valid
		Write	Even	$\overline{HWR}$	Valid	Hi-Z
			Odd	$\overline{LWR}$	Hi-Z	Valid
	Word	Read	—	$\overline{RD}$	Valid	Valid
		Write	—	$\overline{HWR}$, $\overline{LWR}$	Valid	Valid

Note: Hi-Z: High-impedance state
Invalid: Input state; input value is ignored.

6.5.3 Basic Timing

8-Bit, 2-State Access Space: Figure 6.10 shows the bus timing for an 8-bit, 2-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used. The $\overline{LWR}$ pin is always fixed high. Wait states can be inserted.

8-Bit, 3-State Access Space: Figure 6.11 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used. The $\overline{\text{LWR}}$ pin is always fixed high. Wait states can be inserted.

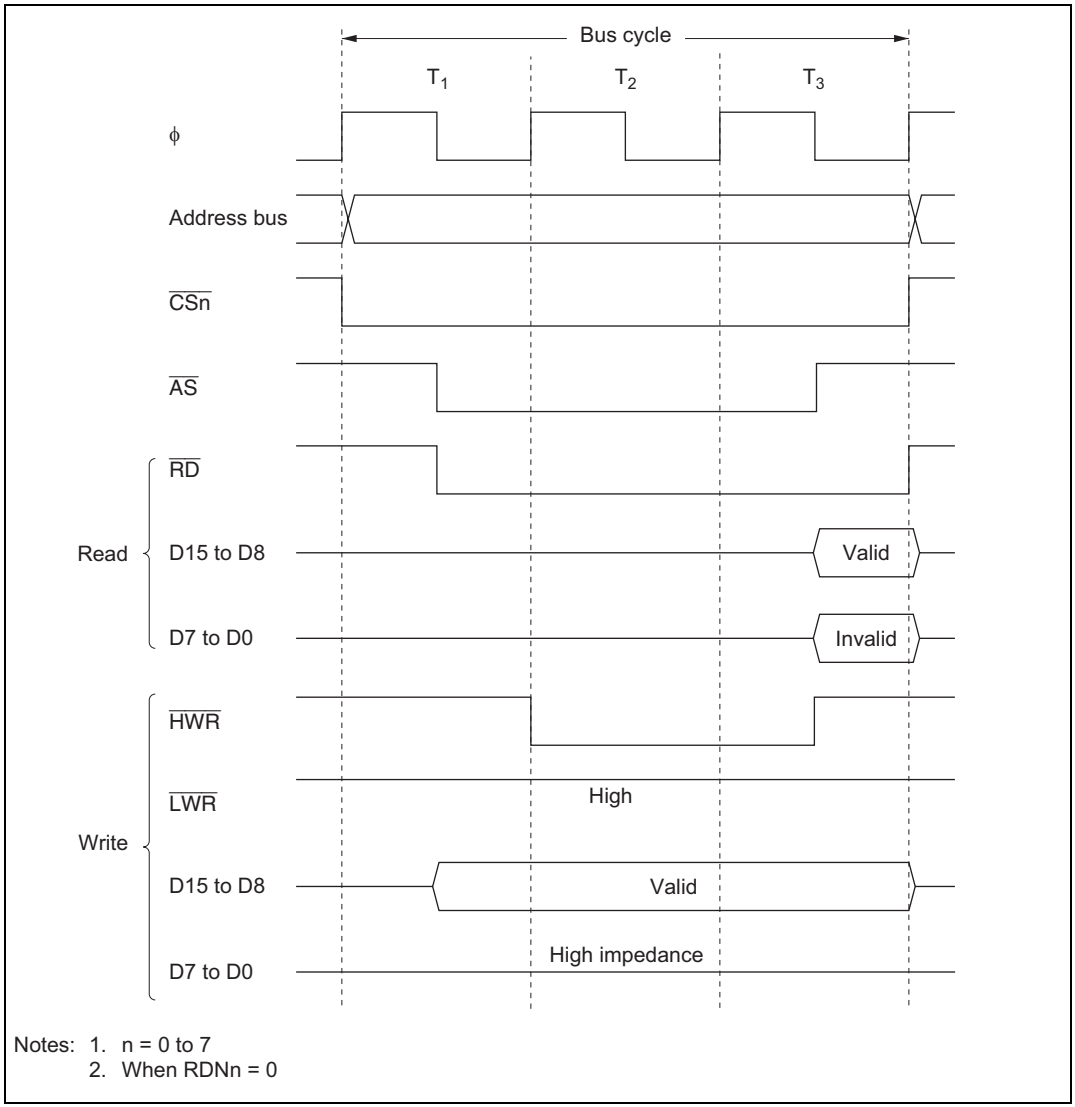


Figure 6.11 Bus Timing for 8-Bit, 3-State Access Space

16-Bit, 2-State Access Space: Figures 6.12 to 6.14 show bus timings for a 16-bit, 2-state access space. When a 16-bit access space is accessed, the upper half (D15 to D8) of the data bus is used

6.7.7 CAS Latency Control

CAS latency is controlled by settings of the W22 to W20 bits of WTCRB. Set the CAS latency count, as shown in table 6.10, by the setting of synchronous DRAM. Depending on the setting, the CAS latency control cycle (T_{c1}) is inserted. WTCRB can be set regardless of the setting of the AST2 bit of ASTCR. Figure 6.45 shows the CAS latency control timing when synchronous DRAM of CAS latency 3 is connected.

The initial value of W22 to W20 is H'7. Set the register according to the CAS latency of synchronous DRAM to be connected.

Table 6.10 Setting CAS Latency

W22	W21	W20	Description	CAS Latency Control Cycle Inserted
0	0	0	Connect synchronous DRAM of CAS latency 1	0 state
		1	Connect synchronous DRAM of CAS latency 2	1 state
	1	0	Connect synchronous DRAM of CAS latency 3	2 states
		1	Connect synchronous DRAM of CAS latency 4	3 states
1	0	0	Reserved (must not used)	—
		1	Reserved (must not used)	—
	1	0	Reserved (must not used)	—
		1	Reserved (must not used)	—

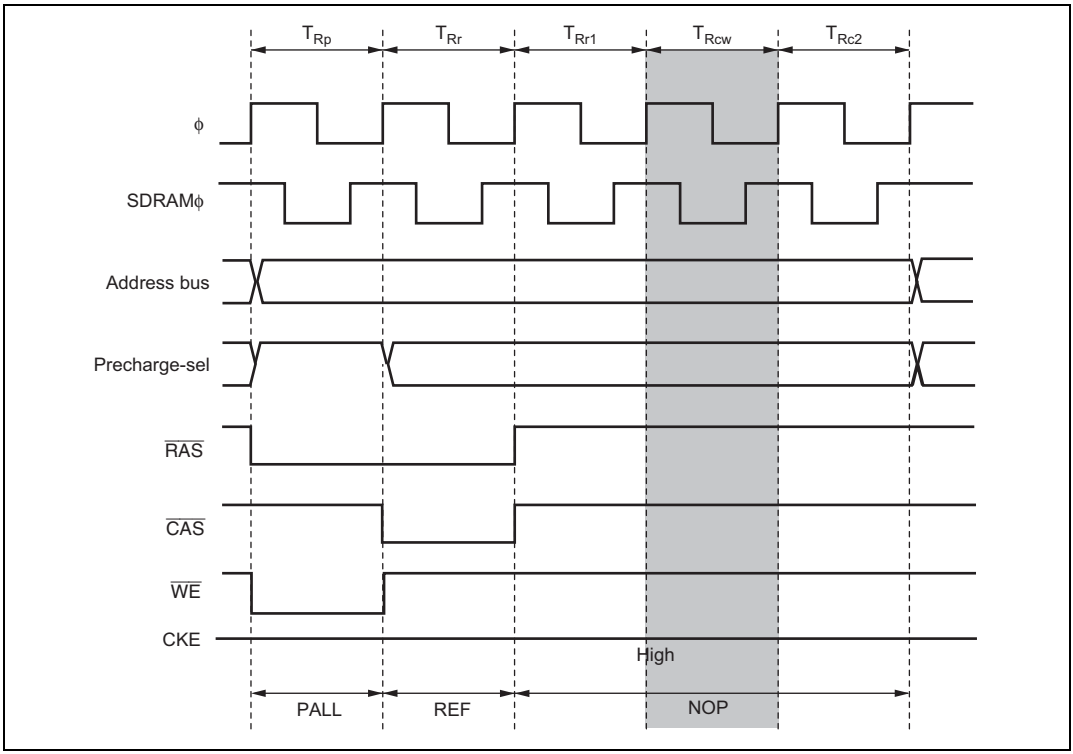


Figure 6.56 Auto Refresh Timing
(TPC = 0, TPC0 = 0, RLW1 = 0, RLW0 = 1)

Self-Refreshing: A self-refresh mode (battery backup mode) is provided for synchronous DRAM as a kind of standby mode. In this mode, refresh timing and refresh addresses are generated within the synchronous DRAM.

To select self-refreshing, set the RFSHE bit to 1 in REFCR. When a SLEEP instruction is executed to enter software standby mode, the SELF command is issued, as shown in figure 6.57.

When software standby mode is exited, the SLFRF bit in REFCR is cleared to 0 and self-refresh mode is exited automatically. If an auto refresh request occurs when making a transition to software standby mode, auto refreshing is executed, then self-refresh mode is entered.

When using self-refresh mode, the OPE bit must not be cleared to 0 in SBYCR.

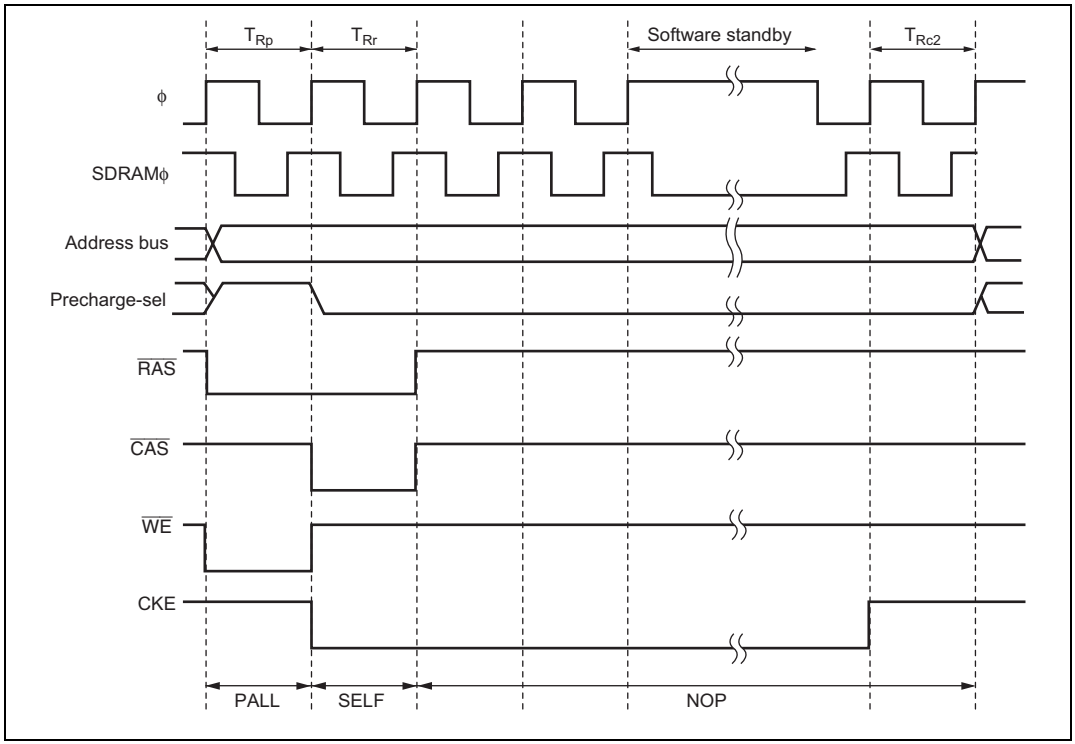


Figure 6.57 Self-Refresh Timing
(TPC1 = 1, TPC0 = 0, RCW1 = 0, RCW0 = 0, RLW1 = 0, RLW0 = 0)

In some synchronous DRAMs provided with a self-refresh mode, the interval between clearing self-refreshing and the next command is specified. A setting can be made in bits TPCS2 to TPCS0 in REFCR to make the precharge time after self-refreshing from 1 to 7 states longer than the normal precharge time. In this case, too, normal precharging is performed according to the setting of bits TPC1 and TPC0 in DRACCR, and therefore a setting should be made to give the optimum post-self-refresh precharge time, including this time. Figure 6.58 shows an example of the timing when the precharge time after self-refreshing is extended by 2 states.

Write after Read: If an external write occurs after an external read while the ICIS0 bit is set to 1 in BCR, an idle cycle is inserted at the start of the write cycle.

Figure 6.66 shows an example of the operation in this case. In this example, bus cycle A is a read cycle for ROM with a long output floating time, and bus cycle B is a CPU write cycle. In (a), an idle cycle is not inserted, and a collision occurs in bus cycle B between the read data from ROM and the CPU write data. In (b), an idle cycle is inserted, and a data collision is prevented.

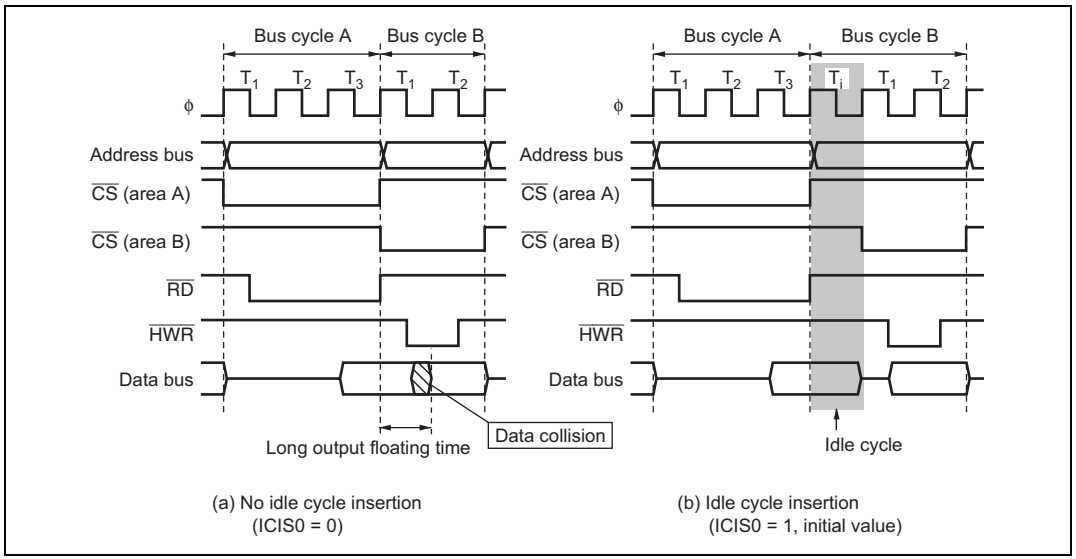


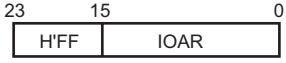
Figure 6.66 Example of Idle Cycle Operation (Write after Read)

7.5.2 Sequential Mode

Sequential mode can be specified by clearing the RPE bit in DMACR to 0. In sequential mode, MAR is updated after each byte or word transfer in response to a single transfer request, and this is executed the number of times specified in ETCR. One address is specified by MAR, and the other by IOAR. The transfer direction can be specified by the DTDIR bit in DMACR.

Table 7.5 summarizes register functions in sequential mode.

Table 7.5 Register Functions in Sequential Mode

	Function			
Register	**DTDIR = 0**	**DTDIR = 1**	**Initial Setting**	**Operation**
	Source address register	Destination address register	Start address of transfer destination or transfer source	Incremented/ decremented every transfer
	Destination address register	Source address register	Start address of transfer source or transfer destination	Fixed
	Transfer counter		Number of transfers	Decremented every transfer; transfer ends when count reaches H'0000

MAR specifies the start address of the transfer source or transfer destination as 24 bits. MAR is incremented or decremented by 1 or 2 each time a byte or word is transferred. IOAR specifies the lower 16 bits of the other address. The 8 bits above IOAR have a value of H'FF.

Figure 7.3 illustrates operation in sequential mode.

8.4.10 EXDMAC Bus Cycles (Single Address Mode)

Single Address Mode (Read): Figure 8.22 shows an example of transfer when $\overline{\text{ETEND}}$ output is enabled, and byte-size, single address mode transfer (read) is performed from external 8-bit, 2-state access space to an external device.

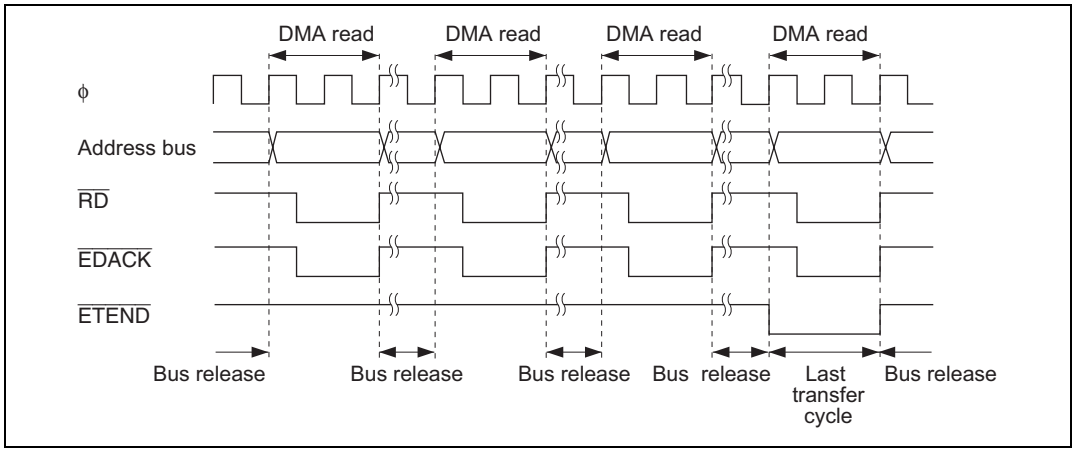


Figure 8.22 Example of Single Address Mode (Byte Read) Transfer

Figure 8.23 shows an example of transfer when $\overline{\text{ETEND}}$ output is enabled, and word-size, single address mode transfer (read) is performed from external 8-bit, 2-state access space to an external device.

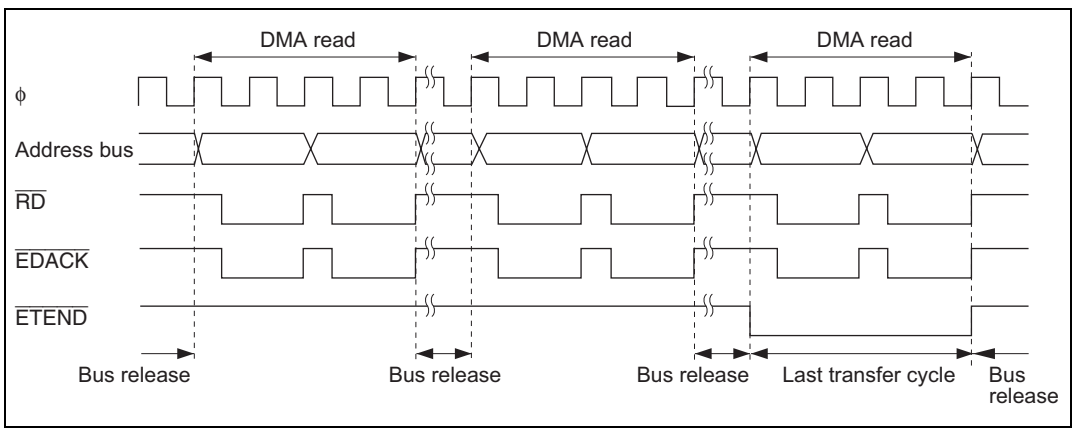


Figure 8.23 Example of Single Address Mode (Word Read) Transfer

- P14/PO12/TIOCA1

  The pin function is switched as shown below according to the combination of the TPU channel 1 settings (by bits MD3 to MD0 in TMDR_1, bits IOA3 to IOA0 in TIOR_1, and bits CCLR1 and CCLR0 in TCR_1), bit NDER12 in NDERH, and bit P14DDR.

TPU channel 1 settings	(1) in table below	(2) in table below		
P14DDR	—	0	1	1
NDER12	—	—	0	1
Pin function	TIOCA1 output	P14 input	P14 output	PO12 output
		TIOCA1 input*1		

TPU channel 1 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01××		B'001×	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	B'××00	Other than B'××00	Other than B'××00	
CCLR1, CCLR0	—	—	—	—	Other than B'01	B'01
Output function	—	Output compare output	—	PWM*2 mode 1 output	PWM mode 2 output	—

Legend:

×: Don't care

Notes: 1. TIOCA1 input when MD3 to MD0 = B'0000 or B'01×× and IOA3 to IOA0 = B'10××.

2. TIOCB1 output disabled.

- P33/RxD1/SCL1

  The pin function is switched as shown below according to the combination of bit ICE in ICCRA of I^2C_0, bit RE in SCR of SCI_1 and bit P33DDR.

ICE	0			1
RE	0		1	—
P33DDR	0	1	—	—
Pin function	P33 input	P33 output*1	RxD1 input	SCL1 I/O*2

Notes: 1. NMOS open-drain output when P33ODR = 1.
2. NMOS open-drain output regardless of P33ODR.

- P32/RxD0/IrRxD/SDA1

  The pin function is switched as shown below according to the combination of bit ICE in ICCRA of I^2C_0, bit RE in SCR of SCI_0 and bit P32DDR.

ICE	0			1
RE	0		1	—
P32DDR	0	1	—	—
Pin function	P32 input	P32 output*1	RxD0/IrRxD input	SDA1 I/O*2

Notes: 1. NMOS open-drain output when P32ODR = 1.
2. NMOS open-drain output regardless of P32ODR.

- P31/TxD1

  The pin function is switched as shown below according to the combination of bit TE in SCR of SCI_1 and bit P31DDR.

TE	0		1
P31DDR	0	1	—
Pin function	P31 input	P31 output*	TxD1 output*

Note: * NMOS open-drain output when P31ODR = 1.

Table 11.17 TIORL_3

				Description	
Bit 7 IOD3	**Bit 6 IOD2**	**Bit 5 IOD1**	**Bit 4 IOD0**	**TGRD_3 Function**	**TIOCD3 Pin Function**
0	0	0	0	Output compare register*2	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	0	0	0	Input capture register*2	Capture input source is TIOCD3 pin Input capture at rising edge
			1		Capture input source is TIOCD3 pin Input capture at falling edge
		1	×		Capture input source is TIOCD3 pin Input capture at both edges
	1	×	×		Capture input source is channel 4/count clock Input capture at TCNT_4 count-up/count-down*1

Legend: ×: Don’t care

Notes: 1. When bits TPSC2 to TPSC0 in TCR_4 are set to B'000 and φ/1 is used as the TCNT_4 count clock, this setting is invalid and input capture is not generated.

2. When the BFB bit in TMDR_3 is set to 1 and TGRD_3 is used as a buffer register, this setting is invalid and input capture/output compare is not generated.

Table 15.6 BRR Settings for Various Bit Rates (Clocked Synchronous Mode)

Bit Rate	Operating Frequency ϕ (MHz)																	
	8		10		16		20		25		30		33		34*1		35*2	
(bit/s)	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																		
250	3	124	—	—	3	249												
500	2	249	—	—	3	124	—	—			3	233						
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	132	3	136
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	212	2	218
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	105	2	108
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	212	1	218
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	84	1	87
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	0	169	0	174
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	84	0	87
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	33	0	34
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	16	—	—
1 M	0	1			0	3	0	4	—	—	—	—	—	—			—	—
2.5 M			0	0*			0	1	—	—	0	2	—	—			—	—
5 M							0	0*	—	—	—	—	—	—			—	—

Legend:

Blank: Cannot be set.

—: Can be set, but there will be a degree of error.

*: Continuous transfer is not possible.

Notes: 1. Supported on the H8S/2378 0.18μm F-ZTAT Group and H8S/2378R 0.18μm F-ZTAT Group only.

2. Supported on the H8S/2378 only.

Table 15.12 Settings of Bits IrCKS2 to IrCKS0

Operating Frequency ϕ (MHz)	Bit Rate (bps) (Above)/Bit Period × 3/16 (µs) (Below)					
	2400	9600	19200	38400	57600	115200
	78.13	19.53	9.77	4.88	3.26	1.63
8	100	100	100	100	100	100
9.8304	100	100	100	100	100	100
10	100	100	100	100	100	100
12	101	101	101	101	101	101
12.288	101	101	101	101	101	101
14	101	101	101	101	101	101
14.7456	101	101	101	101	101	101
16	101	101	101	101	101	101
16.9344	101	101	101	101	101	101
17.2032	101	101	101	101	101	101
18	101	101	101	101	101	101
19.6608	101	101	101	101	101	101
20	101	101	101	101	101	101
25	110	110	110	110	110	—
30	110	110	110	110	110	—
33	110	110	110	110	110	—
34*1	110	110	110	110	110	—
35*2	110	110	110	110	110	—

Legend:

—: A bit rate setting cannot be made on the SCI side.

Notes: 1. Supported on the H8S/2378 0.18µm F-ZTAT Group and H8S/2378R 0.18µm F-ZTAT Group only.

2. Supported on the H8S/2378 only.

18.4 Operation

The D/A converter includes D/A conversion circuits for six channels*1, each of which can operate independently.

When DAOE bit in DACR01*2, DACR23, or DACR45*3 is set to 1, D/A conversion is enabled and the conversion result is output.

The operation example concerns D/A conversion on channel 2. Figure 18.4 shows the timing of this operation.

[1] Write the conversion data to DADR2.

[2] Set the DAOE2 bit in DACR23 to 1. D/A conversion is started. The conversion result is output from the analog output pin DA2 after the conversion time t_{DCONV} has elapsed. The conversion result is continued to output until DADR2 is written to again or the DAOE2 bit is cleared to 0. The output value is expressed by the following formula:

$$\frac{\text{DADR contents}}{256} \times \text{Vref}$$

[3] If DADR2 is written to again, the conversion is immediately started. The conversion result is output after the conversion time t_{DCONV} has elapsed.

[4] If the DAOE2 bit is cleared to 0, analog output is disabled.

Notes: 1. Two channels are available for the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.
2. Not supported by the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.
3. Not supported by the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.

(3) Erasing Procedure in User Program Mode

The procedures for download, initialization, and erasing are shown in figure 21.12.

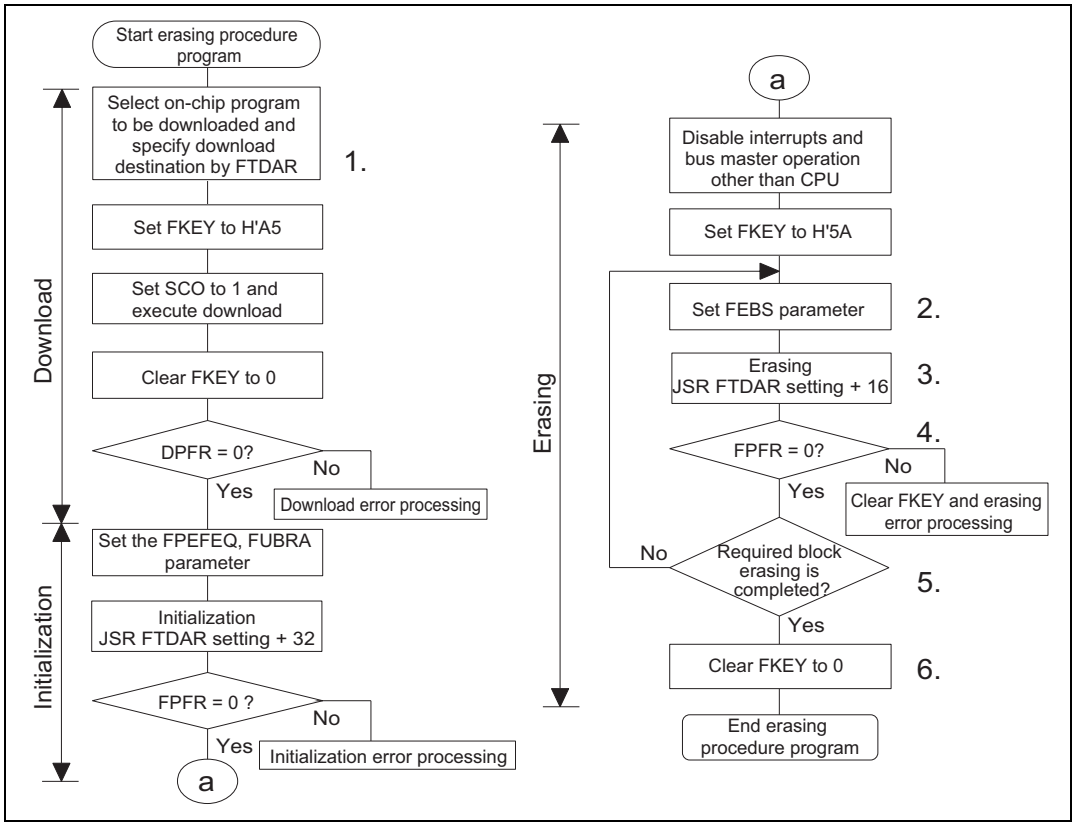


Figure 21.12 Erasing Procedure

The procedure program must be executed in an area other than the user MAT to be erased. Especially the part where the SCO bit in FCCS is set to 1 for downloading must be executed in the on-chip RAM.

The area that can be executed in the steps of the user procedure program (on-chip RAM, user MAT, and external space) is shown in section 21.4.4, Procedure Program and Storable Area for Programming Data.

For the downloaded on-chip program area, refer to figure 21.10.

Instruction	1	2	3	4	5	6	7	8	9
BLD #xx:3,@aa:8	R:W 2nd	R:B EA	R:W NEXT						
BLD #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W NEXT					
BLD #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W NEXT				
BNOT #xx:3,Rd	R:W NEXT								
BNOT #xx:3,@ERd	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BNOT #xx:3,@aa:8	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BNOT #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B:M EA	R:W:M NEXT	W:B EA				
BNOT #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B:M EA	R:W:M NEXT	W:B EA			
BNOT Rn,Rd	R:W NEXT								
BNOT Rn,@ERd	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BNOT Rn,@aa:8	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					
BNOT Rn,@aa:16	R:W 2nd	R:W 3rd	R:B:M EA	R:W:M NEXT	W:B EA				
BNOT Rn,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B:M EA	R:W:M NEXT	W:B EA			
BOR #xx:3,Rd	R:W NEXT								
BOR #xx:3,@ERd	R:W 2nd	R:B EA	R:W NEXT						
BOR #xx:3,@aa:8	R:W 2nd	R:B EA	R:W NEXT						
BOR #xx:3,@aa:16	R:W 2nd	R:W 3rd	R:B EA	R:W NEXT					
BOR #xx:3,@aa:32	R:W 2nd	R:W 3rd	R:W 4th	R:B EA	R:W NEXT				
BSET #xx:3,Rd	R:W NEXT								
BSET #xx:3,@ERd	R:W 2nd	R:B:M EA	R:W:M NEXT	W:B EA					