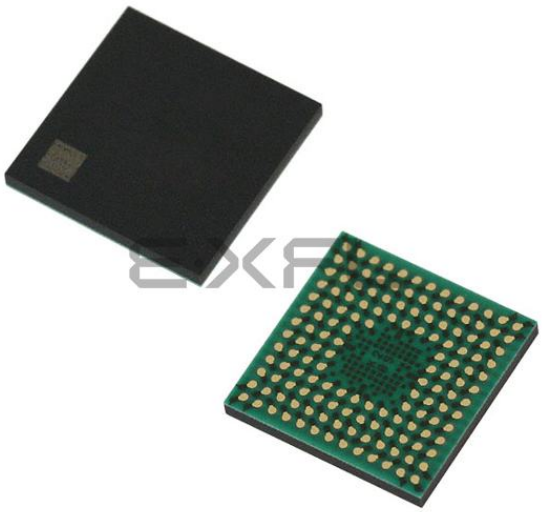

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2371rvlp34v

Item	Page	Revision (See Manual for Details)
15.4.4 SCI Initialization (Asynchronous Mode)	727	Description added Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as shown in figure 15.5. Do not write to SMR, SCMR, IrCR, or SEMR while the SCI is operating. This also applies to writing the same data as the current register contents. …
15.6.2 SCI Initialization (Clocked Synchronous Mode)	741	Description added Before transmitting and receiving data, you should first clear the TE and RE bits in SCR to 0, then initialize the SCI as described in a sample flowchart in figure 15.15. Do not write to SMR, SCMR, IrCR, or SEMR while the SCI is operating. This also applies to writing the same data as the current register contents. …
Section 16 I^2C Bus Interface 2 (IIC2) (Option)	771	Description amended The I^2C bus interface conforms to and provides a subset of the NXP Semiconductors I^2C bus (inter-IC bus) interface (Rev. 3) standard and fast mode functions. The register configuration that controls the I^2C bus differs partly from the NXP Semiconductors configuration, however.
16.3.1 I^2C Bus Control Register A (ICCRA) Table 16.2 Transfer Rate	776	Table amended

Bit 3	Bit 2	Bit 1	Bit 0		Transfer Rate						
CKS3	CKS2	CKS1	CKS0	Clock	φ = 8 MHz	φ = 10 MHz	φ = 20 MHz	φ = 25 MHz	φ = 33 MHz	φ = 34 MHz*1	φ = 35 MHz*2
0*4	0*4	0	0	φ/28	286 kHz	357 kHz	714 kHz*3	893 kHz*3	1179 kHz*3	1214 kHz*3	1250 kHz*3
			1	φ/40	200 kHz	250 kHz	500 kHz*3	625 kHz*3	825 kHz*3	850 kHz*3	875 kHz*3
		1	0	φ/48	167 kHz	208 kHz	417 kHz*3	521 kHz*3	688 kHz*3	708 kHz*3	729 kHz*3
			1	φ/64	125 kHz	156 kHz	313 kHz	391 kHz	516 kHz*3	531 kHz*3	547 kHz*3

Notes 3 and 4 added

3. I^2C bus interface specification (standard mode: max. 100 kHz, fast mode: max. 400 kHz).
4. Due to load conditions, etc., it may not be possible to attain the specified transfer rate when CKS3 and CKS2 are both cleared to 0 (bit period: 7.5 tcyc) and the operating frequency is 20 MHz or higher. Use a bit period other than 7.5 tcyc when the operating frequency exceeds 20 MHz.

8-Bit, 3-State Access Space: Figure 6.11 shows the bus timing for an 8-bit, 3-state access space. When an 8-bit access space is accessed, the upper half (D15 to D8) of the data bus is used. The $\overline{\text{LWR}}$ pin is always fixed high. Wait states can be inserted.

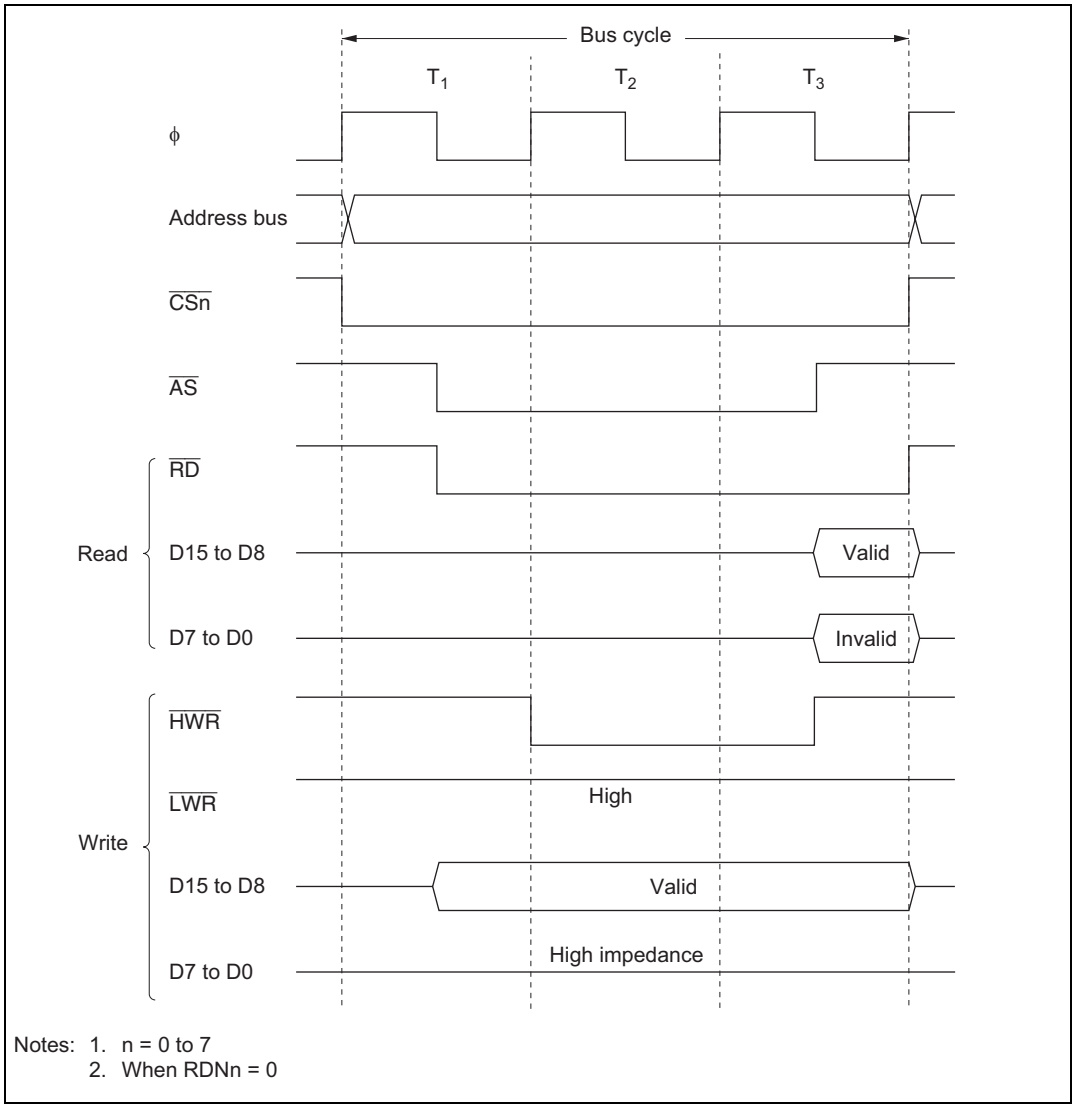


Figure 6.11 Bus Timing for 8-Bit, 3-State Access Space

16-Bit, 2-State Access Space: Figures 6.12 to 6.14 show bus timings for a 16-bit, 2-state access space. When a 16-bit access space is accessed, the upper half (D15 to D8) of the data bus is used

6.7.5 Synchronous DRAM Clock

When the DCTL pin is fixed to 1, synchronous clock (SDRAMϕ) is output from the $\overline{CS5}$ pin. When the frequency multiplication factor of the PLL circuit of this LSI is set to ×1 or ×2, SDRAMϕ is 90° phase shift from ϕ. Therefore, a stable margin is ensured for the synchronous DRAM that operates at the rising edge of clocks. Figure 6.43 shows the relationship between ϕ and SDRAMϕ. When the frequency multiplication factor of the PLL circuit is ×4, the phase of SDRAMϕ and that of ϕ are the same.

When the CLK pin of the synchronous DRAM is directly connected to SDRAMϕ of this LSI, it is recommended to set the frequency multiplication factor of the PLL circuit to ×1 or ×2.

Note: SDRAMϕ output timing is shown when the frequency multiplication factor of the PLL circuit is ×1 or ×2.

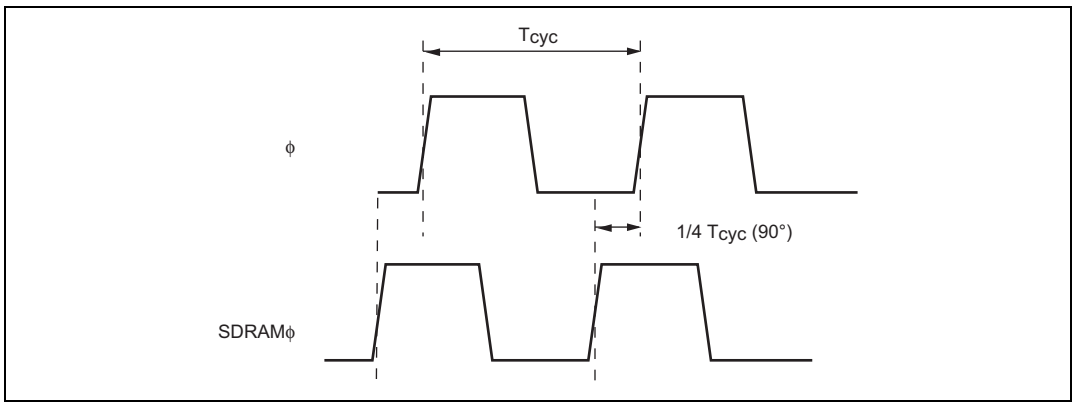


Figure 6.43 Relationship between ϕ and SDRAMϕ (when PLL Frequency Multiplication Factor Is ×1 or ×2)

6.7.6 Basic Timing

The four states of the basic timing consist of one T_p (precharge cycle) state, one T_r (row address output cycle) state, and the T_{c1} and two T_{c2} (column address output cycle) states.

When areas 2 to 5 are set for the continuous synchronous DRAM space, settings of the WAITE bit of BCR, RAST, CAST, RCDM bits of DRAMCR, and the CBRM bit of REFCR are ignored.

Figure 6.44 shows the basic timing for synchronous DRAM.

Bit	Bit Name	Initial Value	R/W	Description
3	DTF3	0	R/W	• Channel B
2	DTF2	0	R/W	0000: Setting prohibited
1	DTF1	0	R/W	0001: Activated by A/D converter conversion end interrupt
0	DTF0	0	R/W	0010: Activated by $\overline{\text{DREQ}}$ pin falling edge input (detected as a low level in the first transfer after transfer is enabled)
				0011: Activated by $\overline{\text{DREQ}}$ pin low-level input
				0100: Activated by SCI channel 0 transmission complete interrupt
				0101: Activated by SCI channel 0 reception complete interrupt
				0110: Activated by SCI channel 1 transmission complete interrupt
				0111: Activated by SCI channel 1 reception complete interrupt
				1000: Activated by TPU channel 0 compare match/input capture A interrupt
				1001: Activated by TPU channel 1 compare match/input capture A interrupt
				1010: Activated by TPU channel 2 compare match/input capture A interrupt
				1011: Activated by TPU channel 3 compare match/input capture A interrupt
				1100: Activated by TPU channel 4 compare match/input capture A interrupt
				1101: Activated by TPU channel 5 compare match/input capture A interrupt
				1110: Setting prohibited
				1111: Setting prohibited
				The same factor can be selected for more than one channel. In this case, activation starts with the highest-priority channel according to the relative channel priorities. For relative channel priorities, see section 7.5.12, Multi-Channel Operation.

- P52/SCK2/$\overline{\text{IRQ2}}$

  The pin function is switched as shown below according to the combination of bit C/A in SMR of SCI_2, bits CKE0 and CKE1 in SCR, bit ITS2 in ITSR, and bit P52DDR.

CKE1	0				1
C/$\overline{\text{A}}$	0			1	—
CKE0	0		1	—	—
P52DDR	0	1	—	—	—
Pin function	P52 input	P52 output	SCK2 output	SCK2 output	SCK2 input
	$\overline{\text{IRQ2}}$ interrupt input*				

Note: * $\overline{\text{IRQ2}}$ input when ITS2 = 0.

- P51/RxD2/$\overline{\text{IRQ1}}$

  The pin function is switched as shown below according to the combination of bit RE in SCR of SCI_2, bit ITS1 in ITSR, and bit P51DDR.

RE	0		1
P51DDR	0	1	—
Pin function	P51 input	P51 output	RxD2 input
	$\overline{\text{IRQ1}}$ interrupt input*		

Note: * $\overline{\text{IRQ1}}$ input when ITS1 = 0.

- P50/TxD2/$\overline{\text{IRQ0}}$

  The pin function is switched as shown below according to the combination of bit TE in SCR of SCI_2, bit ITS0 in ITSR, and bit P50DDR.

TE	0		1
P50DDR	0	1	—
Pin function	P50 input	P50 output	TxD2 input
	$\overline{\text{IRQ0}}$ interrupt input*		

Note: * $\overline{\text{IRQ0}}$ input when ITS0 = 0.

10.8.2 Pin Functions

Port 9 also functions as the pins for A/D converter analog input and D/A converter analog output. The correspondence between pins are as follows.

- P97/AN15/DA5*

Pin function	AN15 input
	DA5 output

Note: * Not available for the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.

- P96/AN14/DA4*

Pin function	AN14 input
	DA4 output

Note: * Not available for the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.

- P95/AN13/DA3

Pin function	AN13 input
	DA3 output

- P94/AN12/DA2

Pin function	AN12 input
	DA2 output

- P93/AN11

Pin function	AN11 input

- P92/AN10

Pin function	AN10 input

- P91/AN9

Pin function	AN9 input

- P90/AN8

Pin function	AN8 input

10.10 Port B

Port B is an 8-bit I/O port that also has other functions. The port B has the following registers.

- Port B data direction register (PBDDR)
- Port B data register (PBDR)
- Port B register (PORTB)
- Port B pull-up MOS control register (PBPCR)

10.10.1 Port B Data Direction Register (PBDDR)

The individual bits of PBDDR specify input or output for the pins of port B.

PBDDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	PB7DDR	0	W	• Modes 1 and 2 Port B pins are address outputs regardless of the PBDDR settings. • Modes 7 (when EXPE = 1) and 4 Setting a PBDDR bit to 1 makes the corresponding port B pin an address output, while clearing the bit to 0 makes the pin an input port. • Modes 7 (when EXPE = 0) Port B is an I/O port, and its pin functions can be switched with PBDDR.
6	PB6DDR	0	W	
5	PB5DDR	0	W	
4	PB4DDR	0	W	
3	PB3DDR	0	W	
2	PB2DDR	0	W	
1	PB1DDR	0	W	
0	PB0DDR	0	W	

- PF2/$\overline{\text{LCAS}}$/$\overline{\text{IRQ15}}$/DQML*2

  The pin function is switched as shown below according to the combination of the operating mode, bit EXPE, bits RMTS2 to RMTS0 in DRAMCR, bits ABW5 to ABW2 in ABWCR, and bit PF2DDR.

Operating mode	1, 2, 4			3*2, 7				
EXPE	—			0		1		
Areas 2 to 5	Any DRAM / synchronous DRAM*2 space area is 16-bit bus space	All DRAM/ synchronous DRAM*2 space areas are 8-bit bus space, or areas 2 to 5 are all normal space		—		Any DRAM/ synchronous DRAM*2 space area is 16-bit bus space	All DRAM/ synchronous DRAM*2 space areas are 8-bit bus space, or areas 2 to 5 are all normal space	
PF2DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{\text{LCAS}}$/ $\overline{\text{DQML}}$*2 output	PF2 input	PF2 output	PF2 input	PF2 output	$\overline{\text{LCAS}}$/ $\overline{\text{DQML}}$*2 output	PF2 input	PF2 output
	$\overline{\text{IRQ15}}$ interrupt input*1							

Notes: 1. $\overline{\text{IRQ15}}$ interrupt input when bit ITS15 is cleared to 0 in ITSR.
2. Not used in the H8S/2378 0.18μm F-ZTAT Group, H8S/2377, H8S/2375, and H8S/2373.

Bit	Bit Name	Initial Value	R/W	Description
3	PER	0	R/(W)*[1]	Parity Error Indicates that a parity error occurred while receiving in asynchronous mode and the reception has ended abnormally. [Setting condition] • When a parity error is detected during reception If a parity error occurs, the receive data is transferred to RDR but the RDRF flag is not set. Also, subsequent serial reception cannot be continued while the PER flag is set to 1. In clocked synchronous mode, serial transmission cannot be continued, either. [Clearing condition] • When 0 is written to PER after reading PER = 1 • The PER flag is not affected and retains its previous state when the RE bit in SCR is cleared to 0.

Table 15.5 Maximum Bit Rate with External Clock Input (Asynchronous Mode)

ϕ (MHz)	External Input Clock (MHz)	Maximum Bit Rate (bit/s)
8	2.0000	125000
9.8304	2.4576	153600
10	2.5000	156250
12	3.0000	187500
12.288	3.0720	192000
14	3.5000	218750
14.7456	3.6864	230400
16	4.0000	250000
17.2032	4.3008	268800
18	4.5000	281250
19.6608	4.9152	307200
20	5.0000	312500
25	6.2500	390625
30	7.5000	468750
33	8.2500	515625
34*1	8.5000	531250
35*2	8.7500	546875

Notes: 1. Supported on the H8S/2378 0.18μm F-ZTAT Group and H8S/2378R 0.18μm F-ZTAT Group only.
2. Supported on the H8S/2378 only.

15.4 Operation in Asynchronous Mode

Figure 15.2 shows the general format for asynchronous serial communication. One frame consists of a start bit (low level), followed by transfer data, a parity bit, and finally stop bits (high level). In asynchronous serial communication, the transmission line is usually held in the mark state (high level). The SCI monitors the transmission line, and when it goes to the space state (low level), recognizes a start bit and starts serial communication. In asynchronous serial communication, the communication line is usually held in the mark state (high level). The SCI monitors the communication line, and when it goes to the space state (low level), recognizes a start bit and starts serial communication. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

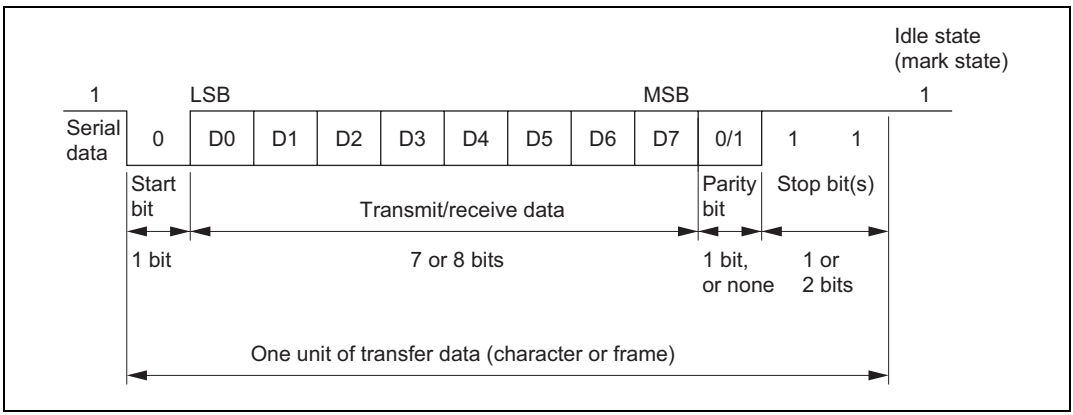


Figure 15.2 Data Format in Asynchronous Communication (Example with 8-Bit Data, Parity, Two Stop Bits)

15.4.1 Data Transfer Format

Table 15.10 shows the data transfer formats that can be used in asynchronous mode. Any of 12 transfer formats can be selected according to the SMR setting. For details on the multiprocessor bit, refer to section 15.5, Multiprocessor Communication Function.

15.6 Operation in Clocked Synchronous Mode

Figure 15.14 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received in synchronization with clock pulses. One character of communication data consists of 8-bit data. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI receives data in synchronization with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

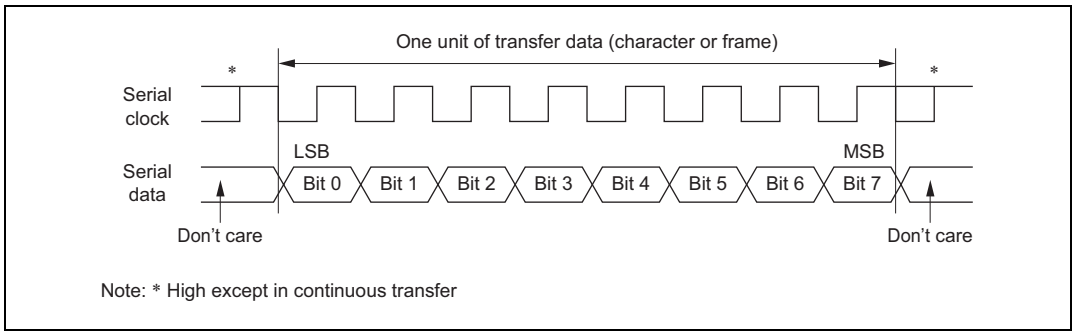


Figure 15.14 Data Format in Clocked Synchronous Communication (For LSB-First)

15.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of CKE1 and CKE0 bits in SCR. When the SCI is operated on an internal clock, the serial clock is output from the SCK pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

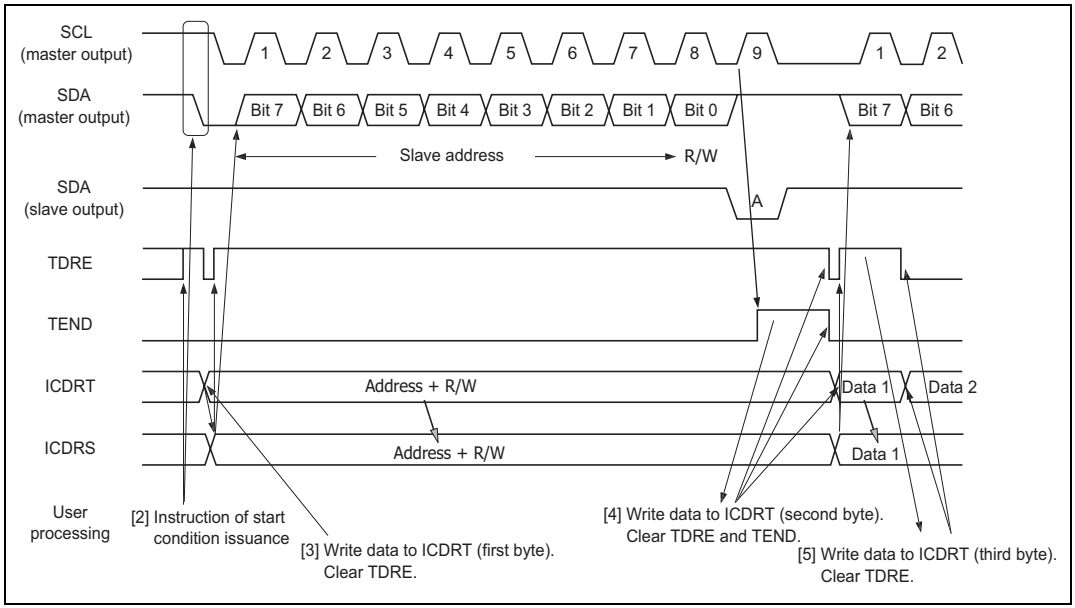


Figure 16.5 Master Transmit Mode Operation Timing 1

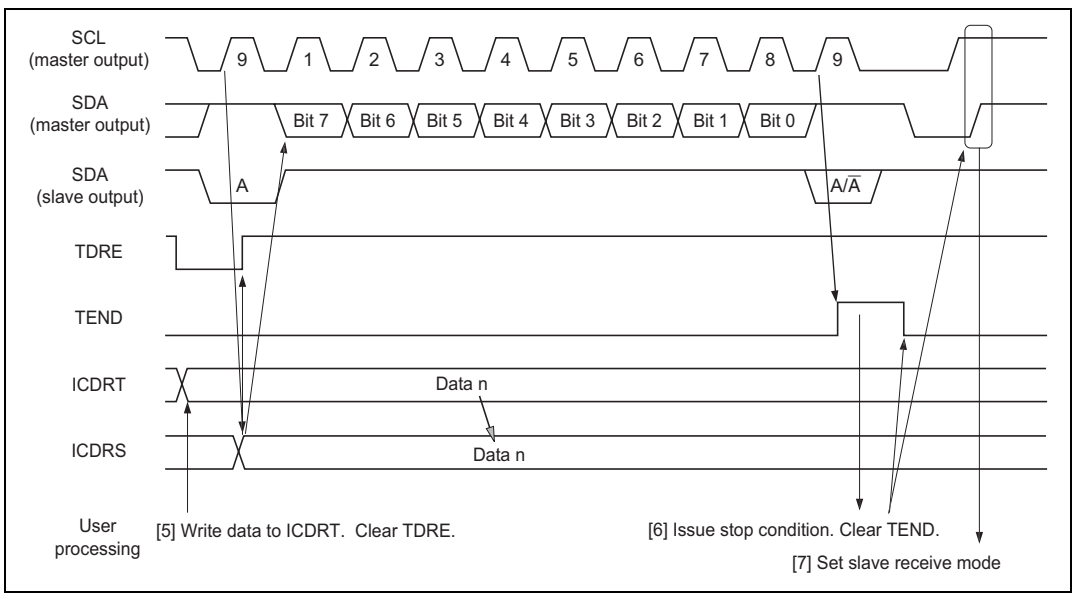


Figure 16.6 Master Transmit Mode Operation Timing 2

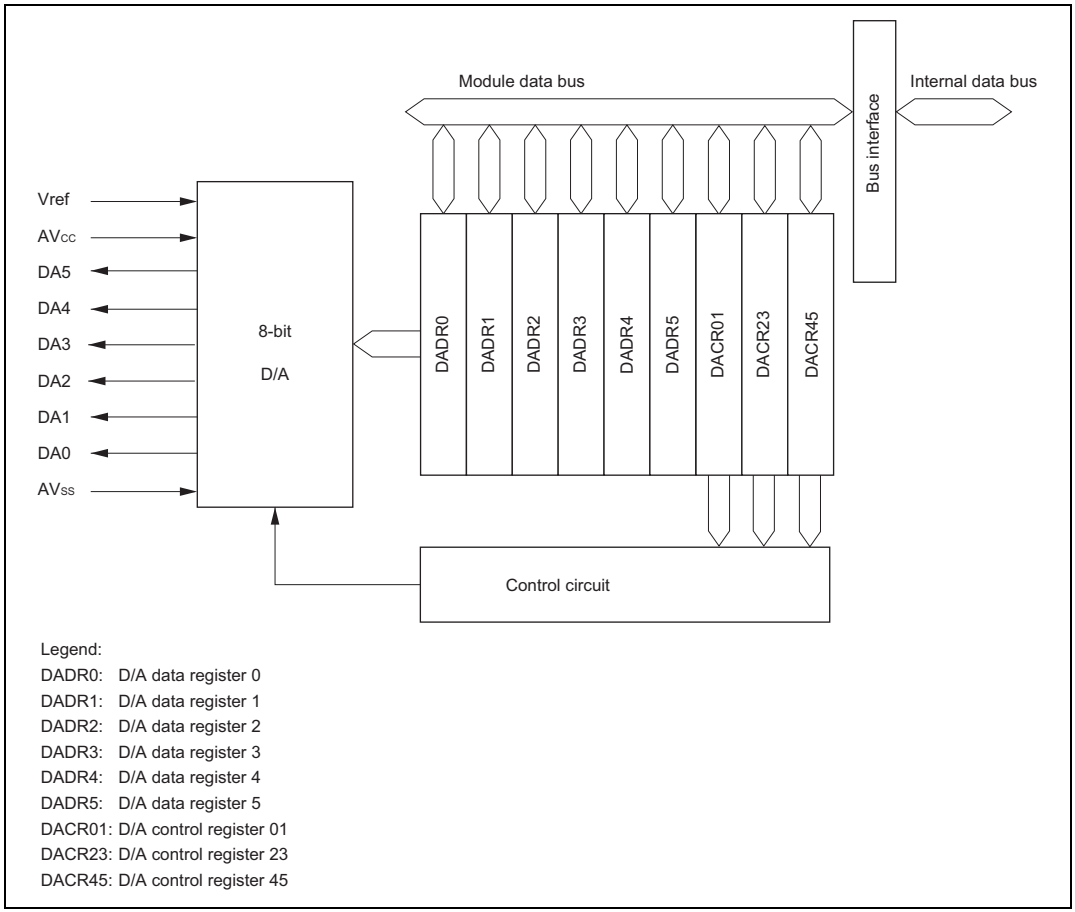


Figure 18.1 Block Diagram of D/A Converter for H8S/2378 0.18µm F-ZTAT Group, H8S/2378R 0.18µm F-ZTAT Group, H8S/2377, and H8S/2377R

Command	H'58	Size	Block number	SUM

- Command, H'58, (one byte): Erasure
- Size, (one byte): The number of bytes that represents the block number
  This is fixed to 1.
- Block number (one byte): H'FF
  Stop code for erasure
- SUM (one byte): Checksum

Response	H'06

- Response, H'06, (one byte): Response to end of erasure (ACK)
  When erasure is to be performed after the block number H'FF has been sent, the procedure should be executed from the erasure selection command.

(11) Memory read

The boot program will return the data in the specified address.

Command	H'52	Size	Area	Read address	
	Read size				SUM

- Command: H'52 (1 byte): Memory read
- Size (1 byte): Amount of data that represents the area, read address, and read size (fixed at 9)
- Area (1 byte)
  H'00: User boot MAT
  H'01: User MAT
  An address error occurs when the area setting is incorrect.
- Read address (4 bytes): Start address to be read from
- Read size (4 bytes): Size of data to be read
- SUM (1 byte): Checksum

Response	H'52	Read size						
	Data	…						
	SUM							

- Response: H'52 (1 byte): Response to memory read
- Read size (4 bytes): Size of data to be read
- Data (n bytes): Data for the read size from the read address
- SUM (1 byte): Checksum

Section 23 Clock Pulse Generator

This LSI has an on-chip clock pulse generator (CPG) that generates the system clock (ϕ) and internal clocks.

The clock pulse generator consists of an oscillator circuit, PLL circuit, and divider.

Figure 23.1 shows a block diagram of the clock pulse generator.

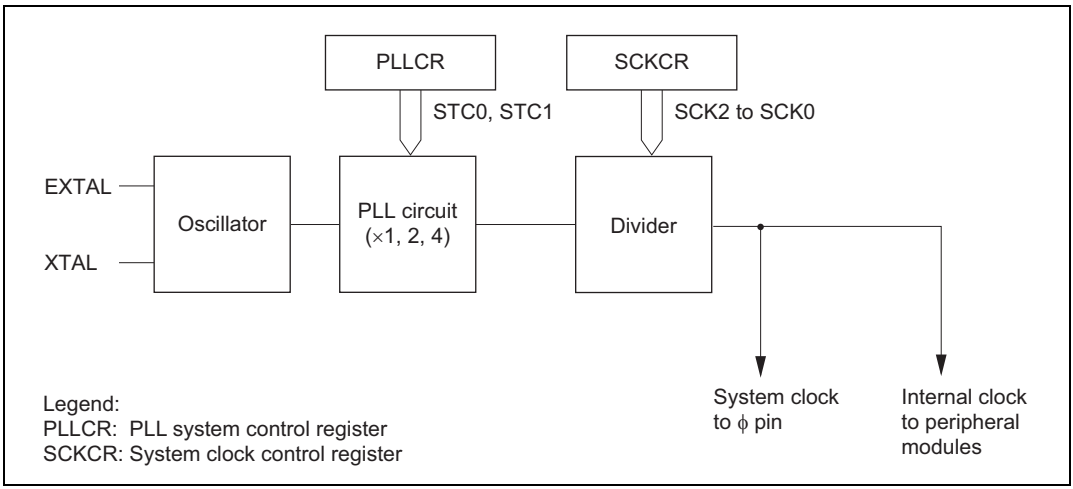


Figure 23.1 Block Diagram of Clock Pulse Generator

The frequency can be changed by means of the PLL circuit. Frequency changes are made by software by means of settings in the PLL control register (PLLCR) and the system clock control register (SCKCR).

23.1 Register Descriptions

The clock pulse generator has the following registers.

- System clock control register (SCKCR)
- PLL control register (PLLCR)

23.1.1 System Clock Control Register (SCKCR)

SCKCR controls ϕ clock output and selects operation when the frequency multiplication factor used by the PLL circuit is changed, and the division ratio used by the divider.

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
RAM standby voltage	V_{RAM}	2.5	—	—	V	
V_{CC} start voltage*5	$V_{CCstart}$	—	—	0.8	V	
V_{CC} rise slope*5	SV_{CC}	—	—	20	ms/V	

Notes: 1. When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current consumption values are for $V_{IH}min = V_{CC} - 0.2$ V and $V_{IL}max = 0.2$ V with all output pins unloaded and all input pull-up MOSs in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, $V_{IH}min = V_{CC} \times 0.9$, and $V_{IL}max = 0.3$ V.

4. I_{CC} depends on V_{CC} and f as follows:

   $I_{CC}max = 15\ (mA) + 0.37\ (mA/(MHz \times V)) \times V_{CC} \times f$ (normal operation)

   $I_{CC}max = 15\ (mA) + 0.20\ (mA/(MHz \times V)) \times V_{CC} \times f$ (sleep mode)

5. Applies when $\overline{RES}$ pin is low level at power-on.

Table 26.17 Permissible Output Currents

Conditions: $V_{CC} = 3.0$ V to 3.6 V, $AV_{CC} = 3.0$ V to 3.6 V, $V_{ref} = 3.0$ V to AV_{CC},
$V_{SS} = AV_{SS} = 0$ V*, $T_a = -20$°C to +75°C (regular specifications),
$T_a = -40$°C to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	SCL0, 1, SDA0, 1	I_{OL}	—	—	8.0	mA
	Output pins other than the above		—	—	2.0	
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in table 26.17.

Note: * When the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

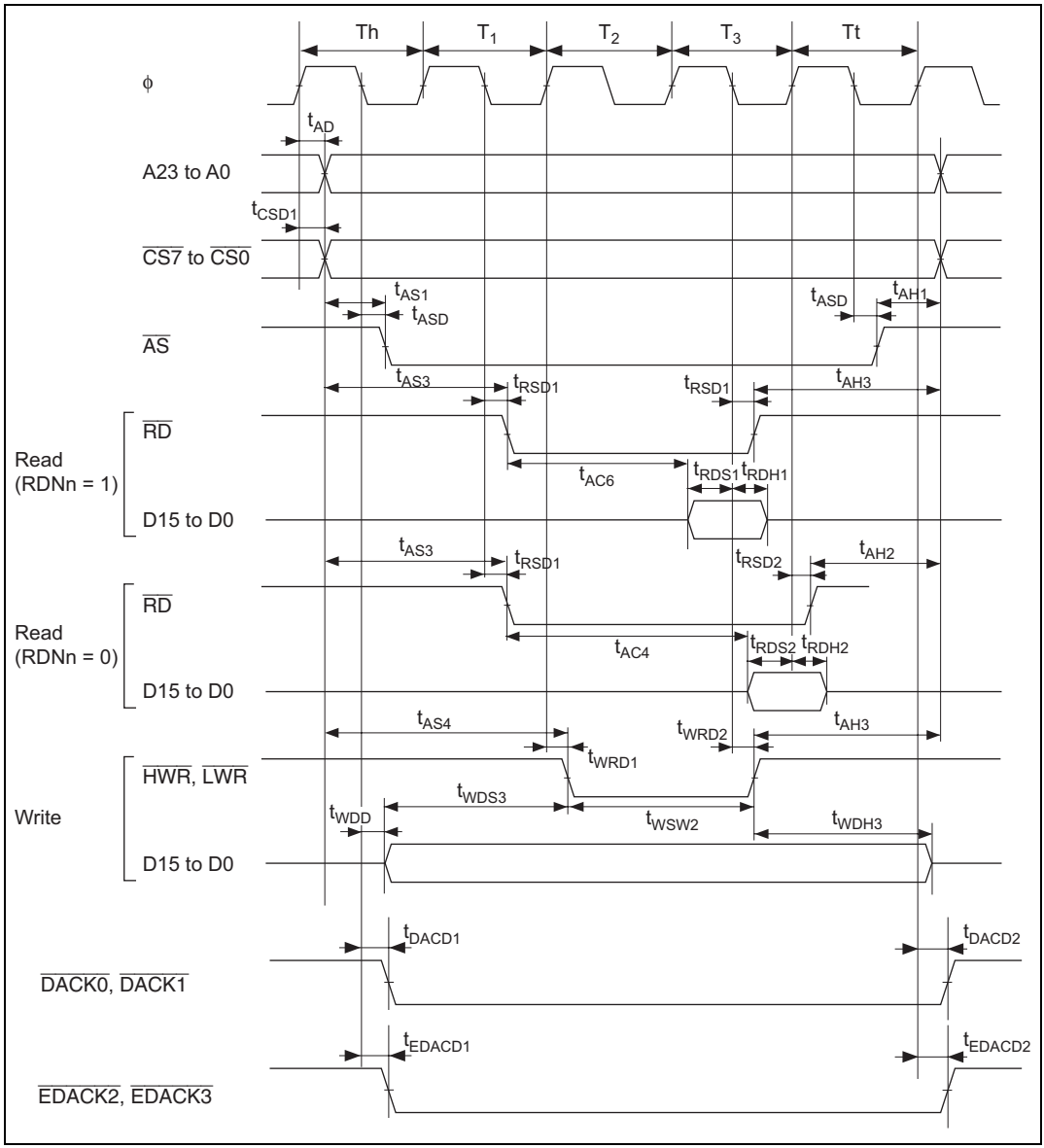
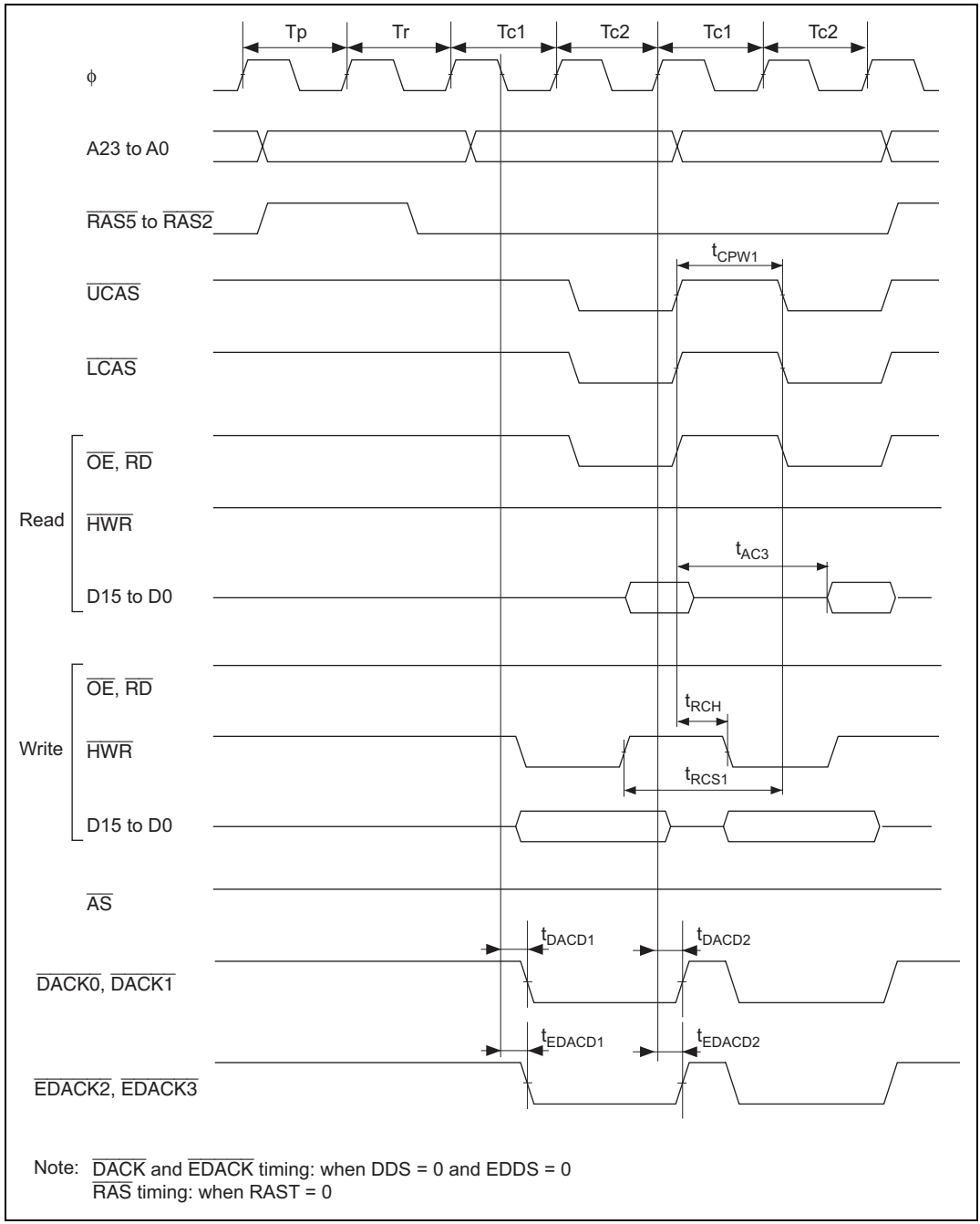


Figure 26.11 Basic Bus Timing: Three-State Access ($\overline{CS}$ Assertion Period Extended)



Note: DACK and EDACK timing: when DDS = 0 and EDDS = 0
RAS timing: when RAST = 0

Figure 26.16 DRAM Access Timing: Two-State Burst Access

Appendix

A. I/O Port States in Each Pin State

Port Name	MCU Operating Mode	Reset	Hardware Standby Mode	Software Standby Mode	Bus Release State	Program Execution State Sleep Mode
Port 1	1, 2, 4, 7	T	T	keep	keep	I/O port
Port 2	1, 2, 4, 7	T	T	keep	keep	I/O port
P34 to P30	1, 2, 4, 7	T	T	keep	keep	I/O port
P35/$\overline{OE}$/ CKE*1	1, 2, 4, 7	T	T	[OPE = 0, $\overline{OE}$, CKE output]	[OPE = 0, $\overline{OE}$, CKE output]	[OPE = 0, $\overline{OE}$, CKE output]
				T	T	$\overline{OE}$, CKE
				[OPE = 1, $\overline{OE}$ output]	[Other than the above]	[Other than the above]
				H	keep	I/O port
				[OPE = 1, CKE output]		
				L		
				[Other than the above]		
				keep		
P47/DA1	1, 2, 4, 7	T	T	[DAOE1 = 1]	keep	Input port
				keep		
				[DAOE1 = 0]		
				T		
P46/DA0	1, 2, 4, 7	T	T	[DAOE0 = 1]	keep	Input port
				keep		
				[DAOE0 = 0]		
				T		
P45 to P40	1, 2, 4, 7	T	T	T	T	Input port
P53 to P50	1, 2, 4, 7	T	T	keep	keep	I/O port
Port 6	1, 2, 4, 7	T	T	keep	keep	I/O port
Port 8	1, 2, 4, 7	T	T	keep	keep	I/O port