Renesas Electronics America Inc - DF2372RVFQ34V Datasheet

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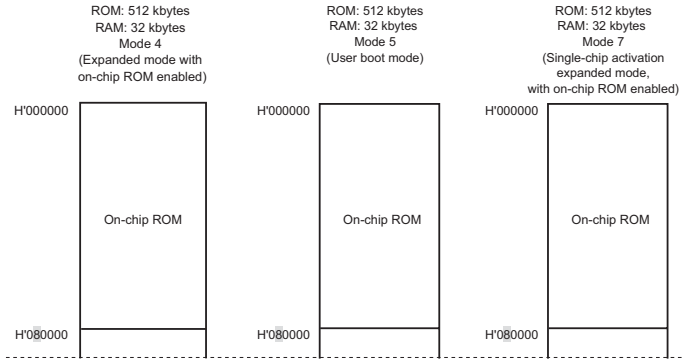
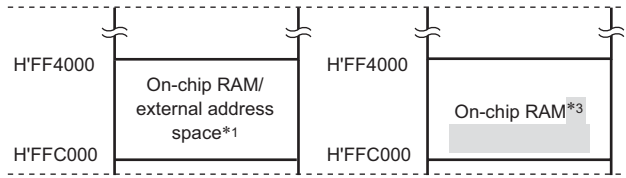
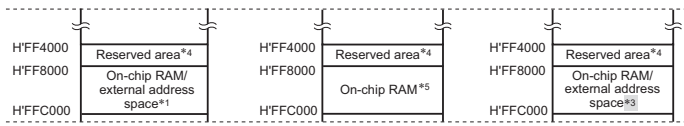
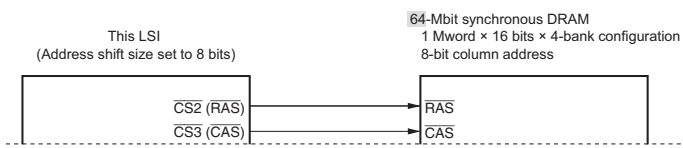
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2372rvfq34v

Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)
3.4 Memory Map in Each Operating Mode Figure 3.2 Memory Map for H8S/2378 and H8S/2378R (2)	79	Figure amended 
Figure 3.7 Memory Map for H8S/2374 and H8S/2374R (1)	84	Figure amended 
Figure 3.15 Memory Map for H8S/2370 and H8S/2370R (2)	92	Figure amended 
6.7.11 Byte Access Control Figure 6.51 Example of DQMU and DQML Byte Control	230	Figure amended 
6.9.2 Pin States in Idle Cycle Table 6.12 Pin States in Idle Cycle	268	Table amended **Pins** — **Pin State** EDACKn (n = 3, 2) — High
7.3.7 DMA Terminal Control Register (DMATCR)	306	Description amended … The TEND pin is available only for channel B in short address mode.

Contents

2.7.7 Program-Counter Relative—@(d:8, PC) or @(d:16, PC)

This mode can be used by the Bcc and BSR instructions. An 8-bit or 16-bit displacement contained in the instruction code is sign-extended to 24 bits and added to the 24-bit address indicated by the PC value to generate a 24-bit branch address. Only the lower 24 bits of this branch address are valid; the upper 8 bits are all assumed to be 0 (H'00). The PC value to which the displacement is added is the address of the first byte of the next instruction, so the possible branching range is –126 to +128 bytes (–63 to +64 words) or –32766 to +32768 bytes (–16383 to +16384 words) from the branch instruction. The resulting value should be an even number.

2.7.8 Memory Indirect—@@aa:8

This mode can be used by the JMP and JSR instructions. The instruction code contains an 8-bit absolute address specifying a memory operand which contains a branch address. The upper bits of the 8-bit absolute address are all assumed to be 0, so the address range is 0 to 255 (H'0000 to H'00FF in normal mode, H'000000 to H'0000FF in advanced mode).

In normal mode, the memory operand is a word operand and the branch address is 16 bits long. In advanced mode, the memory operand is a longword operand, the first byte of which is assumed to be 0 (H'00).

Note that the top area of the address range in which the branch address is stored is also used for the exception vector area. For further details, refer to section 4, Exception Handling.

If an odd address is specified in word or longword memory access, or as a branch address, the least significant bit is regarded as 0, causing data to be accessed or the instruction code to be fetched at the address preceding the specified address. (For further information, see section 2.5.2, Memory Data Formats.)

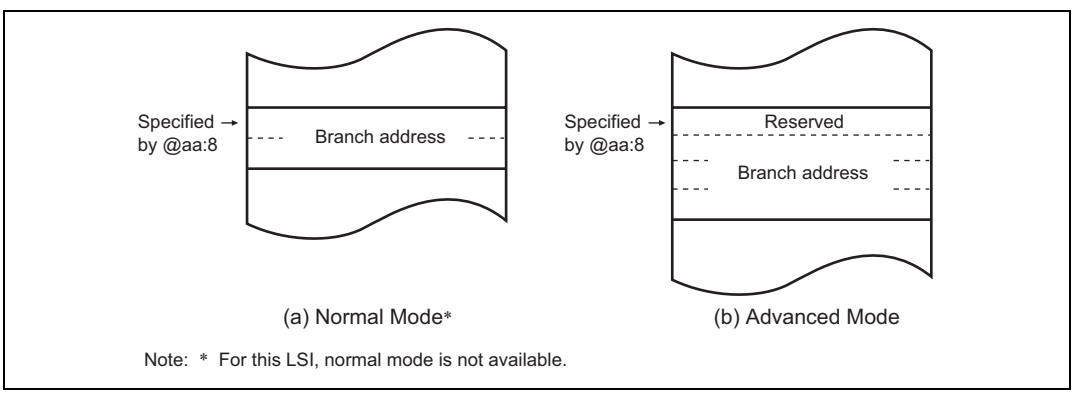


Figure 2.12 Branch Address Specification in Memory Indirect Addressing Mode

6.3.6 Area 0 Burst ROM Interface Control Register (BROMCRH)
Area 1 Burst ROM Interface Control Register (BROMCRL)

BROMCRH and BROMCRL are used to make burst ROM interface settings. Area 0 and area 1 burst ROM interface settings can be made independently in BROMCRH and BROMCRL, respectively.

Bit	Bit Name	Initial Value	R/W	Description
7	BSRMn	0	R/W	Burst ROM Interface Select Selects the basic bus interface or burst ROM interface. 0: Basic bus interface space 1: Burst ROM interface space
6 5 4	BSTSn2 BSTSn1 BSTSn0	0 0 0	R/W R/W R/W	Burst Cycle Select These bits select the number of burst cycle states. 000: 1 state 001: 2 states 010: 3 states 011: 4 states 100: 5 states 101: 6 states 110: 7 states 111: 8 states
3, 2	—	All 0	R/W	Reserved These bits are always read as 0. The initial value should not be changed.
1 0	BSWDn1 BSWDn0	0 0	R/W R/W	Burst Word Number Select These bits select the number of words that can be burst-accessed on the burst ROM interface. 00: Maximum 4 words 01: Maximum 8 words 10: Maximum 16 words 11: Maximum 32 words

(n = 1 or 0)

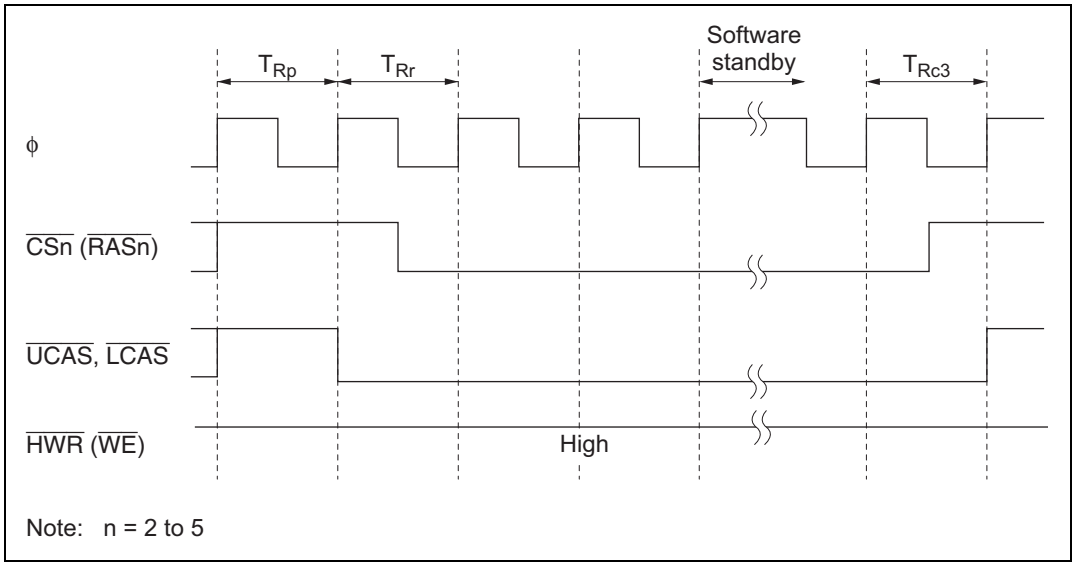


Figure 6.39 Self-Refresh Timing

In some DRAMs provided with a self-refresh mode, the $\overline{RAS}$ signal precharge time immediately after self-refreshing is longer than the normal precharge time. A setting can be made in bits TPCS2 to TPCS0 in REFCR to make the precharge time immediately after self-refreshing from 1 to 7 states longer than the normal precharge time. In this case, too, normal precharging is performed according to the setting of bits TPC1 and TPC0 in DRACCR, and therefore a setting should be made to give the optimum post-self-refresh precharge time, including this time. Figure 6.40 shows an example of the timing when the precharge time immediately after self-refreshing is extended by 2 states.

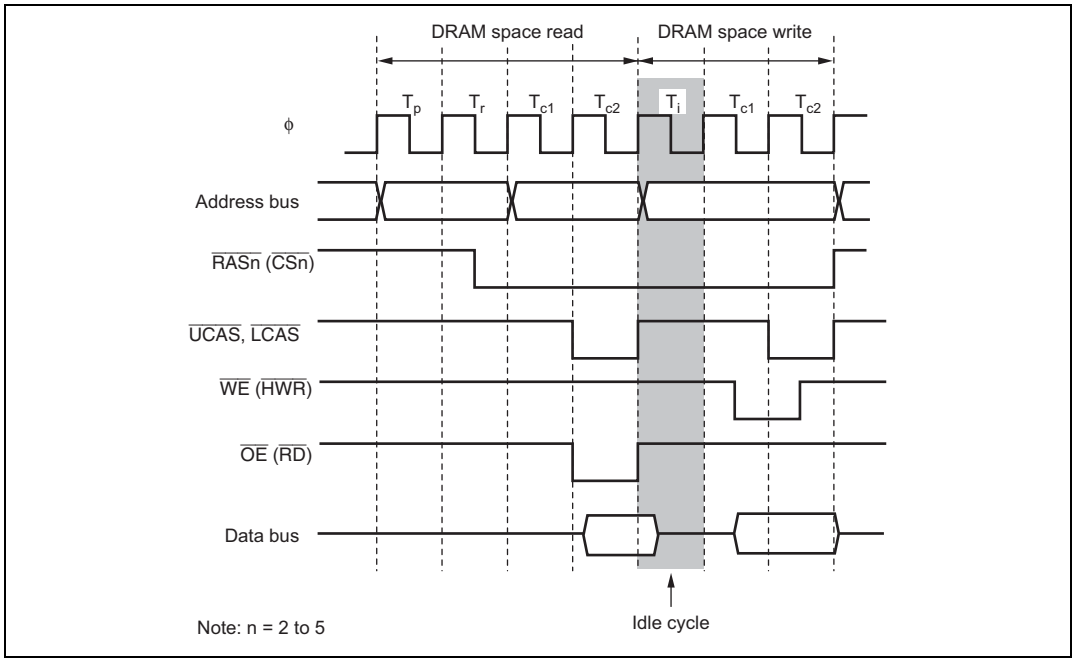


Figure 6.81 Example of Timing for Idle Cycle Insertion in Case of Consecutive Read and Write Accesses to DRAM Space in RAS Down Mode

Bit	Bit Name	Initial Value	R/W	Description
5	DTME0	0	R/W	Data Transfer Master Enable 0 Together with the DTE0 bit, this bit controls enabling or disabling of data transfer on channel 0. When both the DTME0 bit and DTE0 bit are set to 1, transfer is enabled for channel 0. If channel 0 is in the middle of a burst mode transfer when an NMI interrupt is generated, the DTME0 bit is cleared, the transfer is interrupted, and bus mastership passes to the CPU. When the DTME0 bit is subsequently set to 1 again, the interrupted transfer is resumed. In block transfer mode, however, the DTME0 bit is not cleared by an NMI interrupt, and transfer is not interrupted. [Clearing conditions] • When initialization is performed • When NMI is input in burst mode • When 0 is written to the DTME0 bit [Setting condition] When 1 is written to DTME0 after reading DTME0 = 0

Port	Description	Mode 1*3	Mode 2*3	Mode 4	Mode 7		Input/ Output Type
					EXPE = 1	EXPE = 0	
Port A	General I/O port also functioning as address outputs	PA7/A23/$\overline{\text{IRQ7}}$		PA7/A23/$\overline{\text{IRQ7}}$		PA7/$\overline{\text{IRQ7}}$	Only PA4 to PA7 are Schmitt-triggered input when used as IRQ input. Built-in input pull-up MOS Open-drain output capability
		PA6/A22/$\overline{\text{IRQ6}}$		PA6/A22/$\overline{\text{IRQ6}}$		PA6/$\overline{\text{IRQ6}}$	
		PA5/A21/$\overline{\text{IRQ5}}$		PA5/A21/$\overline{\text{IRQ5}}$		PA5/$\overline{\text{IRQ5}}$	
		A20/$\overline{\text{IRQ4}}$		PA4/A20/$\overline{\text{IRQ4}}$		PA4/$\overline{\text{IRQ4}}$	
		A19		PA3/A19		PA3	
		A18		PA2/A18		PA2	
		A17		PA1/A17		PA1	
		A16		PA0/A16		PA0	
Port B	General I/O port also functioning as address outputs	A15		PB7/A15		PB7	Built-in input pull-up MOS
		A14		PB6/A14		PB6	
		A13		PB5/A13		PB5	
		A12		PB4/A12		PB4	
		A11		PB3/A11		PB3	
		A10		PB2/A10		PB2	
		A9		PB1/A9		PB1	
		A8		PB0/A8		PB0	
Port C	General I/O port also functioning as address outputs	A7		PC7/A7		PC7	Built-in input pull-up MOS
		A6		PC6/A6		PC6	
		A5		PC5/A5		PC5	
		A4		PC4/A4		PC4	
		A3		PC3/A3		PC3	
		A2		PC2/A2		PC2	
		A1		PC1/A1		PC1	
		A0		PC0/A0		PC0	

10.11.6 Port C Input Pull-Up MOS States

Port C has a built-in input pull-up MOS function that can be controlled by software. This input pull-up MOS function can be used in modes 4 and 7. Input pull-up MOS can be specified as on or off on a bit-by-bit basis.

In modes 4 and 7, when a PCDDR bit is cleared to 0, setting the corresponding PCPCR bit to 1 turns on the input pull-up MOS for that pin.

Table 10.4 summarizes the input pull-up MOS states.

Table 10.4 Input Pull-Up MOS States (Port C)

Mode	Reset	Hardware Standby Mode	Software Standby Mode	In Other Operations
1, 2	Off	Off	Off	Off
4, 7			On/Off	On/Off

Legend:
Off: Input pull-up MOS is always off.
On/Off: On when PCDDR = 0 and PCPCR = 1; otherwise off.

10.14.2 Port F Data Register (PFDR)

PFDR stores output data for the port F pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PF7DR	0	R/W	Output data for a pin is stored when the pin function is specified to a general purpose I/O.
6	PF6DR	0	R/W	
5	PF5DR	0	R/W	
4	PF4DR	0	R/W	
3	PF3DR	0	R/W	
2	PF2DR	0	R/W	
1	PF1DR	0	R/W	
0	PF0DR	0	R/W	

10.14.3 Port F Register (PORTF)

PORTF shows port F pin states.

PORTF cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	PF7	—*	R	If a port F read is performed while PFDDR bits are set to 1, the PFDR values are read. If a port F read is performed while PFDDR bits are cleared to 0, the pin states are read.
6	PF6	—*	R	
5	PF5	—*	R	
4	PF4	—*	R	
3	PF3	—*	R	
2	PF2	—*	R	
1	PF1	—*	R	
0	PF0	—*	R	

Note: * Determined by the states of pins PF7 to PF0.

- PG5/$\overline{\text{BACK}}$

  The pin function is switched as shown below according to the operating mode, bit EXPE, bit BRLE, and bit PG5DDR.

Operating mode	1, 2, 4			7				
EXPE	—			0		1		
BRLE	0		1	—		0		1
PG5DDR	0	1	—	0	1	0	1	—
Pin function	PG5 input	PG5 output	$\overline{\text{BACK}}$ output	PG5 input	PG5 output	PG5 input	PG5 output	$\overline{\text{BACK}}$ output

- PG4/$\overline{\text{BREQO}}$

  The pin function is switched as shown below according to the operating mode, bit EXPE, bit BRLE, bit BREQO, and bit PG4DDR.

Operating mode	1, 2, 4					7						
EXPE	—					0		1				
BRLE	0		1			—		0		1		
BREQO	—		0		1	—		—		0		1
PG4DDR	0	1	0	1	—	0	1	0	1	0	1	—
Pin function	PG4 input	PG4 output	PG4 input	PG4 output	$\overline{\text{BREQO}}$ output	PG4 input	PG4 output	PG4 input	PG4 output	PG4 input	PG4 output	$\overline{\text{BREQO}}$ output

Table 11.15 TIOR_2

				Description	
Bit 7 IOB3	**Bit 6 IOB2**	**Bit 5 IOB1**	**Bit 4 IOB0**	**TGRB_2 Function**	**TIOCB2 Pin Function**
0	0	0	0	Output compare register	Output disabled
			1		Initial output is 0 output 0 output at compare match
		1	0		Initial output is 0 output 1 output at compare match
			1		Initial output is 0 output Toggle output at compare match
	1	0	0		Output disabled
			1		Initial output is 1 output 0 output at compare match
		1	0		Initial output is 1 output 1 output at compare match
			1		Initial output is 1 output Toggle output at compare match
1	×	0	0	Input capture register	Capture input source is TIOCB2 pin Input capture at rising edge
			1		Capture input source is TIOCB2 pin Input capture at falling edge
		1	×		Capture input source is TIOCB2 pin Input capture at both edges

Legend: ×: Don't care

11.4.4 Cascaded Operation

In cascaded operation, two 16-bit counters for different channels are used together as a 32-bit counter.

This function works by counting the channel 1 (channel 4) counter clock at overflow/underflow of TCNT_2 (TCNT_5) as set in bits TPSC2 to TPSC0 in TCR.

Underflow occurs only when the lower 16-bit TCNT is in phase-counting mode.

Table 11.29 shows the register combinations used in cascaded operation.

Note: When phase counting mode is set for channel 1 or 4, the counter clock setting is invalid and the counter operates independently in phase counting mode.

Table 11.29 Cascaded Combinations

Combination	Upper 16 Bits	Lower 16 Bits
Channels 1 and 2	TCNT_1	TCNT_2
Channels 4 and 5	TCNT_4	TCNT_5

Example of Cascaded Operation Setting Procedure: Figure 11.17 shows an example of the setting procedure for cascaded operation.

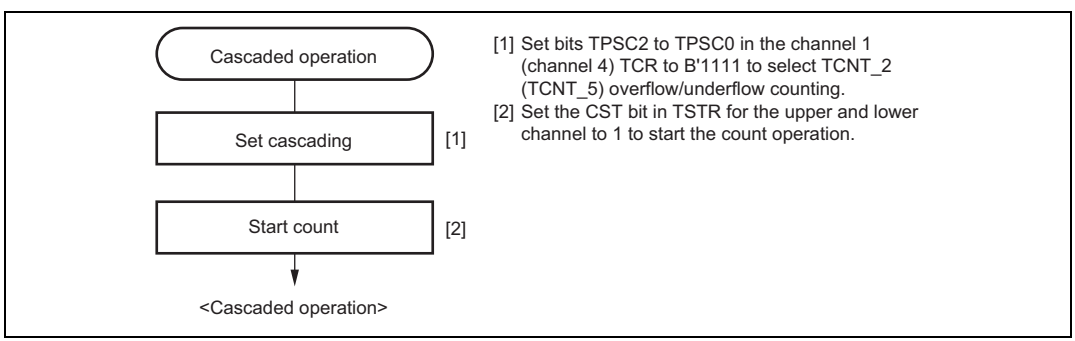


Figure 11.17 Cascaded Operation Setting Procedure

12.3.4 PPG Output Control Register (PCR)

PCR selects output trigger signals on a group-by-group basis. For details on output trigger selection, refer to section 12.3.5, PPG Output Mode Register (PMR).

Bit	Bit Name	Initial Value	R/W	Description
7	G3CMS1	1	R/W	Group 3 Compare Match Select 1 and 0
6	G3CMS0	1	R/W	Select output trigger of pulse output group 3. 00: Compare match in TPU channel 0 01: Compare match in TPU channel 1 10: Compare match in TPU channel 2 11: Compare match in TPU channel 3
5	G2CMS1	1	R/W	Group 2 Compare Match Select 1 and 0
4	G2CMS0	1	R/W	Select output trigger of pulse output group 2. 00: Compare match in TPU channel 0 01: Compare match in TPU channel 1 10: Compare match in TPU channel 2 11: Compare match in TPU channel 3
3	G1CMS1	1	R/W	Group 1 Compare Match Select 1 and 0
2	G1CMS0	1	R/W	Select output trigger of pulse output group 1. 00: Compare match in TPU channel 0 01: Compare match in TPU channel 1 10: Compare match in TPU channel 2 11: Compare match in TPU channel 3
1	G0CMS1	1	R/W	Group 0 Compare Match Select 1 and 0
0	G0CMS0	1	R/W	Select output trigger of pulse output group 0. 00: Compare match in TPU channel 0 01: Compare match in TPU channel 1 10: Compare match in TPU channel 2 11: Compare match in TPU channel 3

15.6 Operation in Clocked Synchronous Mode

Figure 15.14 shows the general format for clocked synchronous communication. In clocked synchronous mode, data is transmitted or received in synchronization with clock pulses. One character of communication data consists of 8-bit data. In clocked synchronous serial communication, data on the transmission line is output from one falling edge of the serial clock to the next. In clocked synchronous mode, the SCI receives data in synchronization with the rising edge of the serial clock. After 8-bit data is output, the transmission line holds the MSB state. In clocked synchronous mode, no parity or multiprocessor bit is added. Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communication by use of a common clock. Both the transmitter and the receiver also have a double-buffered structure, so that data can be read or written during transmission or reception, enabling continuous data transfer.

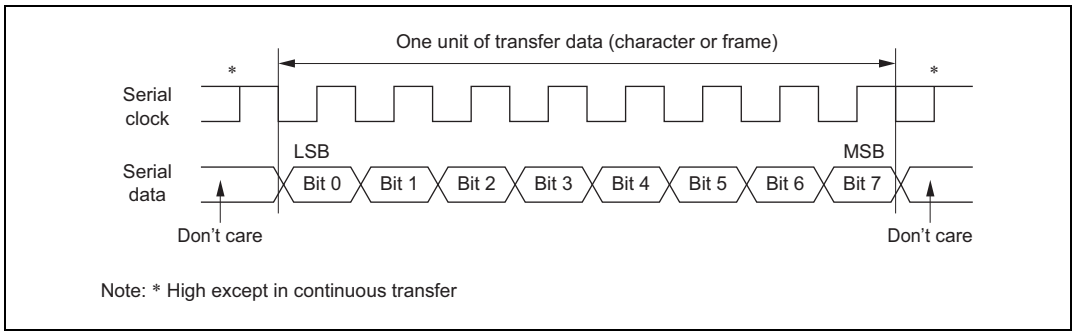


Figure 15.14 Data Format in Clocked Synchronous Communication (For LSB-First)

15.6.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCK pin can be selected, according to the setting of CKE1 and CKE0 bits in SCR. When the SCI is operated on an internal clock, the serial clock is output from the SCK pin. Eight serial clock pulses are output in the transfer of one character, and when no transfer is performed the clock is fixed high.

16.3.2 I²C Bus Control Register B (ICCRB)

ICCRB is an 8-bit readable/writable register that issues start/stop conditions, manipulates the SDA pin, monitors the SCL pin, and controls reset in I²C control.

Bit	Bit Name	Initial Value	R/W	Description
7	BBSY	0	R/W	Bus Busy This bit enables to confirm whether the I²C bus is occupied or released and to issue start and stop conditions in master mode. This bit is set to 1 when the SDA level changes from high to low under the condition of SCL = high, assuming that the start condition has been issued. This bit is cleared to 0 when the SDA level changes from low to high under the condition of SCL = high, assuming that the stop condition has been issued. Write 1 to BBSY and 0 to SCP to issue a start condition. Follow this procedure when also re-transmitting a start condition. Write 0 to BBSY and 0 to SCP to issue a stop condition. To issue a start/stop condition, use the MOV instruction.
6	SCP	1	W	Start Condition/Stop Condition Prohibit The SCP bit controls the issue of start/stop conditions in master mode. To issue a start condition, write 1 in BBSY and 0 in SCP. A retransmit start condition is issued in the same way. To issue a stop condition, write 0 in BBSY and 0 in SCP. This bit is always read as 1. If 1 is written, the data is not stored.
5	SDAO	1	R/W	Monitors the output level of SDA. 0: When reading, SDA pin outputs low. 1: When reading, SDA pin outputs high. The write value must always be 1.
4	—	1	R/W	Reserved The write value must always be 1.
3	SCLO	1	R	This bit monitors SCL output level. When reading and SCLO is 1, SCL pin outputs high. When reading and SCLO is 0, SCL pin outputs low.
2	—	1	—	Reserved This bit is always read as 1.

Bit	Bit Name	Initial Value	R/W	Description
2	WD	—	R/W	Write Data Address Detect When the address in the flash memory area is specified as the start address of the storage destination of the program data, an error occurs. 0: Setting of write data address is normal 1: Setting of write data address is abnormal
1	WA	—	R/W	Write Address Error Detect When the following items are specified as the start address of the programming destination, an error occurs. • When the programming destination address in the area other than flash memory is specified • When the specified address is not a 128-byte boundary (the value of A6 to A0 is not H'0). 0: Setting of programming destination address is normal 1: Setting of programming destination address is abnormal
0	SF	—	R/W	Success/Fail Indicates whether the program processing is ended normally or not. 0: Programming is ended normally (no error) 1: Programming is ended abnormally (error occurs)

(4) Erasure Execution

When flash memory is erased, the erase-block number on the user MAT must be passed to the erasing program which is downloaded. This is set to the FEBS parameter (general register ER0).

One block is specified from the block number 0 to 15.

For details on the erasing processing procedure, see section 21.4.2, User Program Mode.

Register Abbreviation	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Module
BCR	BRLE	BREQ0E	—	IDLC	ICIS1	ICIS0	WDBE	WAITE	BSC
	—	—	—	—	—	ICIS2	—	—	
DRAMCR	OEE	RAST	—	CAST	—	RMTS2	RMTS1	RMTS0	
	BE	RCDM	DDS	EDDS	—	MXC2	MXC1	MXC0	
DRACCRH	DRMI	—	TPC1	TPC0	SDWCD	—	RCD1	RCD0	
DRACCRL	—	—	—	—	CKSPE	—	RDXC1	RDXC0	
REFCR	CMF	CMIE	RCW1	RCW0	—	RTCK2	RTCK1	RTCK0	
	RFSHE	CBRM	RLW1	RLW0	SLFRF	TPCS2	TPCS1	TPCS0	
RTCNT	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
RTCOR	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_0AH	—	—	—	—	—	—	—	—	DMAC
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_0AL	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
IOAR_0A	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
ETCR_0A	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_0BH	—	—	—	—	—	—	—	—	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_0BL	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
IOAR_0B	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
ETCR_0B	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_1AH	—	—	—	—	—	—	—	—	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
MAR_1AL	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	
IOAR_1A	Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	
	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	

26.3.3 AC Characteristics

The clock, control signal, bus, DMAC, EXDMAC, and on-chip peripheral function timings are shown below. The measurement conditions of the AC characteristics are shown in figure 26.1.

(1) Clock Timing

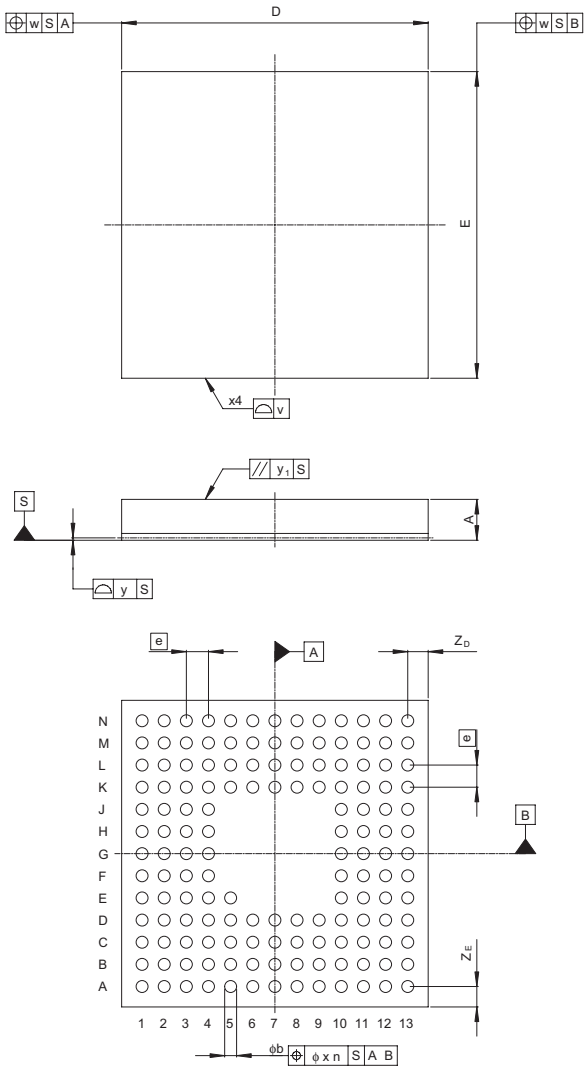
Table 26.31 Clock Timing

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 34 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
Clock cycle time	t_{cyc}	29.4	125	ns	Figure 26.2
Clock pulse high width	t_{CH}	9	—	ns	Figure 26.2
Clock pulse low width	t_{CL}	9	—	ns	
Clock rising time	t_{Cr}	—	5	ns	
Clock falling time	t_{Cf}	—	5	ns	
Reset oscillation settling time (crystal)	t_{OSC1}	10	—	ms	Figure 26.4(1)
Software standby oscillation settling time (crystal)	t_{OSC2}	10	—	ms	Figure 26.4(2)
External clock output delay settling time	t_{DEXT}	1	—	ms	Figure 26.4(1)
Clock phase difference*	t_{cdif}	$1/4 \times t_{cyc} - 3$	$1/4 \times t_{cyc} + 3$	ns	Figure 26.3
Clock pulse high width (SDRAMϕ)*	t_{SDCH}	9	—	ns	Figure 26.3
Clock pulse low width (SDRAMϕ)*	t_{SDCL}	9	—	ns	Figure 26.3
Clock rising time (SDRAMϕ)*	t_{sdcr}	—	5	ns	Figure 26.3
Clock falling time (SDRAMϕ)*	t_{sdcf}	—	5	ns	Figure 26.3

Note: * Supported by the H8S/2378R, H8S/2374R, H8S/2372R, H8S/2371R, and H8S/2370R only.

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-9x9-0.65	PTLG0145JB-A	-	0.15g



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	9.0	—
E	—	9.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.2
A_1	—	—	—
e	—	0.65	—
b	0.30	0.35	0.40
x	—	—	0.08
y	—	—	0.1
y_1	—	—	0.20
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.6	—
Z_E	—	0.6	—

Figure C.2 Package Dimensions (TLP-145V)