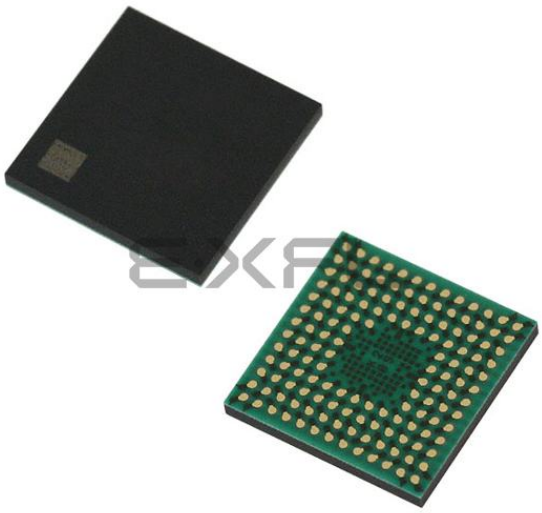

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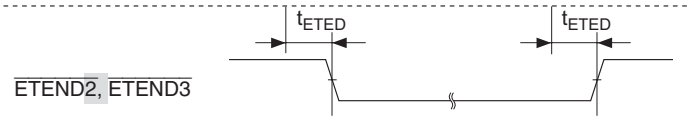
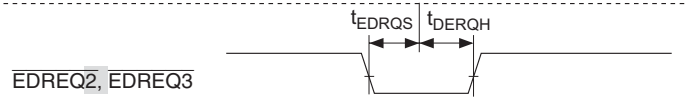
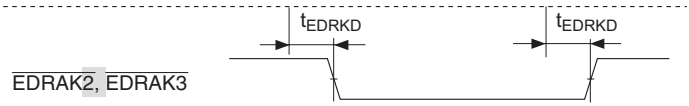
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2372vlp34v

Item	Page	Revision (See Manual for Details)
26.4.4 DMAC and EXDMAC Timing Figure 26.30 DMAC and EXDMAC $\overline{\text{TEND}}$/$\overline{\text{ETEND}}$ Output Timing	1090	Figure amended 
Figure 26.31 DMAC and EXDMAC $\overline{\text{DREQ}}$/$\overline{\text{EDREQ}}$ Input Timing	1090	Figure amended 
Figure 26.32 EXDMAC $\overline{\text{EDRAK}}$ Output Timing	1090	Figure amended 
C. Package Dimensions Figure C.2 Package Dimensions (TLP-145V)	1107	Figure replaced

- H8S/2377, H8S/2377R, H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R

Bit	Bit Name	Initial Value	R/W	Descriptions
7, 6	—	All 1	R/W	Reserved The initial value should not be modified.
5, 4	—	All 0	R/W	Reserved The initial value should not be modified.
3	FLSHE	0	R/W	Flash Memory Control Register Enable Controls CPU access to the flash memory control registers (FLMCR1, FLMCR2, EBR1, and EBR2). If this bit is set to 1, the flash memory control registers can be read from and written to. If this bit is cleared to 0, the flash memory control registers are not selected. At this time, the contents of the flash memory control registers are maintained. This bit should be written to 0 in other than flash memory version. 0: Flash memory control registers are not selected for area H'FFFFC8 to H'FFFFCB 1: Flash memory control registers are selected for area H'FFFFC8 to H'FFFFCB
2	—	0	—	Reserved This bit is always read as 0 and cannot be modified.
1	EXPE	—	R/W	External Bus Mode Enable Sets external bus mode. In modes 1, 2, and 4, this bit is fixed at 1 and cannot be modified. In modes 3 and 7, this bit can be read from and written to. Writing of 0 to this bit when its value is 1 should only be carried out when an external bus cycle is not being executed. 0: External bus disabled 1: External bus enabled
0	RAME	1	R/W	RAM Enable Enables or disables the on-chip RAM. The RAME bit is initialized when the reset state is released. 0: On-chip RAM is disabled 1: On-chip RAM is enabled

3.3.7 Pin Functions

Table 3.2 shows the pin functions in each operating mode.

Table 3.2 Pin Functions in Each Operating Mode

Port		Mode 1	Mode 2	Mode 3	Mode 4	Mode 5	Mode 7
Port A	PA7 to PA5	P*/A	P*/A	P*/A	P*/A	P*/A	P*/A
	PA4 to PA0	A	A				
Port B		A	A	P*/A	P*/A	P*/A	P*/A
Port C		A	A	P*/A	P*/A	P*/A	P*/A
Port D		D	D	P*/D	D	P*/D	P*/D
Port E		P/D*	P*/D	P*/D	P*/D	P*/D	P*/D
Port F	PF7, PF6	P/C*	P/C*	P*/C	P/C*	P*/C	P*/C
	PF5, PF4	C	C		C		
	PF3	P/C*	P/C*		P/C*		
	PF2 to PF0	P*/C	P*/C		P*/C		
Port G	PG6 to PG1	P*/C	P*/C	P*/C	P*/C	P*/C	P*/C
	PG0	P/C*	P/C*		P*/C		

Legend: P: I/O port
A: Address bus output
D: Data bus input/output
C: Control signals, clock input/output
*: After reset

Note: Mode 5 is available only for the H8S/2378 0.18μm F-ZTAT Group and H8S/2378R 0.18μm F-ZTAT Group.
Only modes 1 and 2 may be used on ROM-less versions.

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	—	Reserved This bit is always read as 0 and the initial value should not be changed.
14 13 12	IPR14 IPR13 IPR12	1 1 1	R/W R/W R/W	Sets the priority of the corresponding interrupt source. 000: Priority level 0 (Lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (Highest)
11	—	0	—	Reserved This bit is always read as 0 and the initial value should not be changed.
10 9 8	IPR10 IPR9 IPR8	1 1 1	R/W R/W R/W	Sets the priority of the corresponding interrupt source. 000: Priority level 0 (Lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (Highest)
7	—	0	—	Reserved This bit is always read as 0 and the initial value should not be changed.
6 5 4	IPR6 IPR5 IPR4	1 1 1	R/W R/W R/W	Sets the priority of the corresponding interrupt source. 000: Priority level 0 (Lowest) 001: Priority level 1 010: Priority level 2 011: Priority level 3 100: Priority level 4 101: Priority level 5 110: Priority level 6 111: Priority level 7 (Highest)

6.3.8 DRAM Control Register (DRAMCR)

DRAMCR is used to make DRAM/synchronous DRAM interface settings.

Note: The synchronous DRAM interface is not supported by the H8S/2378 Group.

Bit	Bit Name	Initial Value	R/W	Description
15	OEE	0	R/W	$\overline{OE}$ Output Enable The OE signal used when EDO page mode DRAM is connected can be output from the (OE) pin. The $\overline{OE}$ signal is common to all areas designated as DRAM space. When the synchronous DRAM is connected, the CKE signal can be output from the (OE) pin. The CKE signal is common to the continuous synchronous DRAM space. 0: $\overline{OE}$/CKE signal output disabled ($\overline{OE}$)/(CKE) pin can be used as I/O port 1: $\overline{OE}$/CKE signal output enabled
14	RAST	0	R/W	$\overline{RAS}$ Assertion Timing Select Selects whether, in DRAM access, the $\overline{RAS}$ signal is asserted from the start of the T_r cycle (rising edge of ϕ) or from the falling edge of ϕ. Figure 6.4 shows the relationship between the RAST bit setting and the $\overline{RAS}$ assertion timing. The setting of this bit applies to all areas designated as DRAM space. 0: $\overline{RAS}$ is asserted from ϕ falling edge in T_r cycle 1: $\overline{RAS}$ is asserted from start of T_r cycle
13	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.

6.14 Usage Notes

6.14.1 External Bus Release Function and All-Module-Clocks-Stopped Mode

In this LSI, if the ACSE bit is set to 1 in MSTPCR, and then a SLEEP instruction is executed with the setting for all peripheral module clocks to be stopped (MSTPCR = H'FFFF, EXMSTPCR = H'FFFF) or for operation of the 8-bit timer module alone (MSTPCR = H'FFFE, EXMSTPCR = H'FFFF), and a transition is made to the sleep state, the all-module-clocks-stopped mode is entered in which the clock is also stopped for the bus controller and I/O ports. In this state, the external bus release function is halted. To use the external bus release function in sleep mode, the ACSE bit in MSTPCR must be cleared to 0. Conversely, if a SLEEP instruction to place the chip in all-module-clocks-stopped mode is executed in the external bus released state, the transition to all-module-clocks-stopped mode is deferred and performed until after the bus is recovered.

6.14.2 External Bus Release Function and Software Standby

In this LSI, internal bus master operation does not stop even while the bus is released, as long as the program is running in on-chip ROM, etc., and no external access occurs. If a SLEEP instruction to place the chip in software standby mode is executed while the external bus is released, the transition to software standby mode is deferred and performed after the bus is recovered.

Also, since clock oscillation halts in software standby mode, if $\overline{\text{BREQ}}$ goes low in this mode, indicating an external bus release request, the request cannot be answered until the chip has recovered from the software standby state.

6.14.3 External Bus Release Function and CBR Refreshing/Auto Refreshing

CBR refreshing/auto refreshing cannot be executed while the external bus is released. Setting the BREQOE bit to 1 in BCR beforehand enables the $\overline{\text{BREQO}}$ signal to be output when a CBR refresh/auto refresh request is issued.

Note: The auto refresh control is not supported by the H8S/2378 Group.

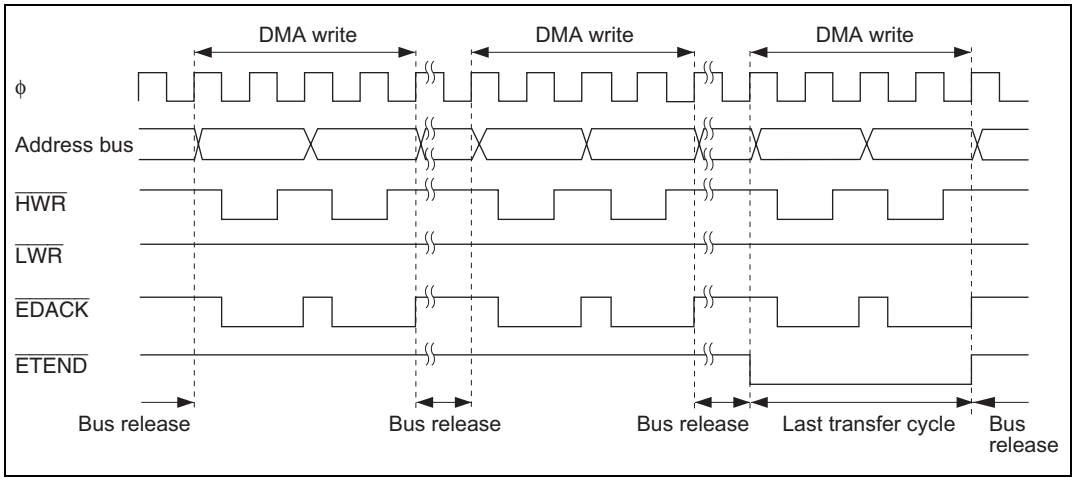


Figure 8.25 Example of Single Address Mode (Word Write) Transfer

After one byte or word has been transferred in response to one transfer request, the bus is released. While the bus is released, one or more CPU, DMAC, or DTC bus cycles are initiated.

9.5.2 Repeat Mode

In repeat mode, one operation transfers one byte or one word of data. Table 9.5 lists the register function in repeat mode. From 1 to 256 transfers can be specified. Once the specified number of transfers has ended, the initial state of the transfer counter and the address register specified as the repeat area is restored, and transfer is repeated. In repeat mode the transfer counter value does not reach H'00, and therefore CPU interrupts cannot be requested when DISEL = 0.

Table 9.5 Register Function in Repeat Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register AH	CRAH	Holds number of transfers
DTC transfer count register AL	CRAL	Designates transfer count
DTC transfer count register B	CRB	Not used

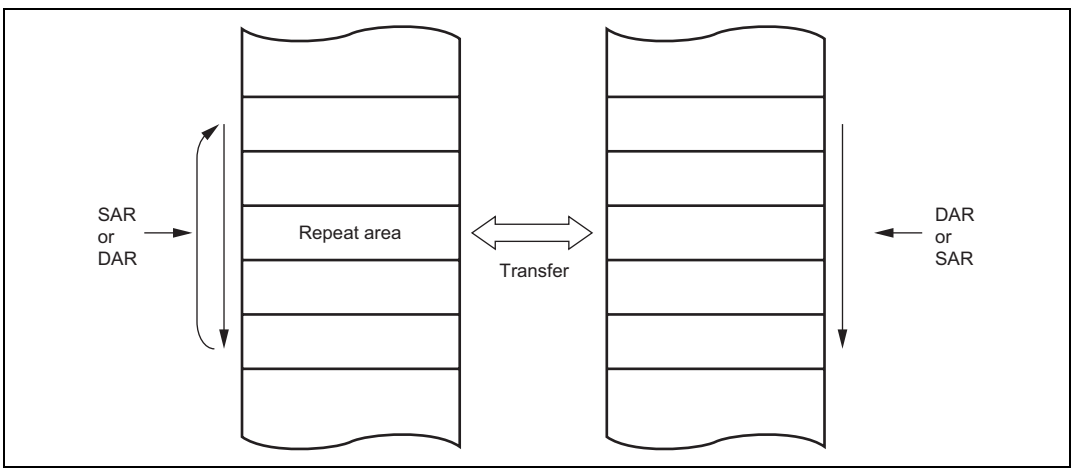


Figure 9.7 Memory Mapping in Repeat Mode

10.2 Port 2

Port 2 is an 8-bit I/O port that also has other functions. The port 2 has the following registers.

- Port 2 data direction register (P2DDR)
- Port 2 data register (P2DR)
- Port 2 register (PORT2)

10.2.1 Port 2 Data Direction Register (P2DDR)

The individual bits of P2DDR specify input or output for the pins of port 2.

P2DDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	P27DDR	0	W	When a pin function is specified to a general purpose I/O, setting this bit to 1 makes the corresponding port 1 pin an output pin, while clearing this bit to 0 makes the pin an input pin.
6	P26DDR	0	W	
5	P25DDR	0	W	
4	P24DDR	0	W	
3	P23DDR	0	W	
2	P22DDR	0	W	
1	P21DDR	0	W	
0	P20DDR	0	W	

- P23/PO3/TIOCD3/TxD4/($\overline{\text{IRQ11}}$)

  The pin function is switched as shown below according to the combination of the TPU channel 3 settings (by bits MD3 to MD0 in TMDR_3, bits IOD3 to IOD0 in TIORL_3, and bits CCLR2 to CCLR0 in TCR_3), bit NDER3 in NDERL, bit TE in SCR of SCI_4, bit P23DDR, and bit ITS11 in ITSR.

TE	0				1
TPU channel 3 settings	(1) in table below	(2) in table below			—
P23DDR	—	0	1	1	—
NDER3	—	—	0	1	—
Pin function	TIOCD3 output	P23 input	P23 output	PO3 output	TXD4 output
		TIOCA3 input*1			
	$\overline{\text{IRQ11}}$ interrupt input*2				

Notes: 1. TIOCD3 input when MD3 to MD0 = B'0000 and IOD3 to IOD0 = B'10××.
2. $\overline{\text{IRQ11}}$ input when ITS11 = 1.

TPU channel 3 settings	(2)	(1)	(2)	(2)	(1)	(2)
MD3 to MD0	B'0000		B'0010	B'0011		
IOD3 to IOD0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	—	B'××00	Other than B'××00	
CCLR2 to CCLR0	—	—	—	—	Other than B'110	B'110
Output function	—	Output compare output	—	—	PWM mode 2 output	—

Legend:
×: Don't care

10.15 Port G

Port G is a 7-bit I/O port that also has other functions. The port G has the following registers.

- Port G data direction register (PGDDR)
- Port G data register (PGDR)
- Port G register (PORTG)
- Port Function Control Register 0 (PFCR0)

10.15.1 Port G Data Direction Register (PGDDR)

The individual bits of PGDDR specify input or output for the pins of port G.

PGDDR cannot be read; if it is, an undefined value will be read.

Bit	Bit Name	Initial Value	R/W	Description
7	—	0	—	Reserved
6	PG6DDR	0	W	• Modes 7 (when EXPE = 1), 1, 2, and 4 Pins PG6 to PG4 function as bus control input/output pins ($\overline{\text{BREQO}}$, $\overline{\text{BACK}}$, and $\overline{\text{BREQ}}$) when the appropriate bus controller settings are made. Otherwise, these pins are I/O ports, and their functions can be switched with PGDDR. When the $\overline{\text{CS}}$ output enable bits (CS3E to CS0E) are set to 1, pins PG3 to PG0 function as $\overline{\text{CS}}$ output pins when the corresponding PGDDR bit is set to 1, and as input ports when the bit is cleared to 0. When CS3E to CS0E are cleared to 0, pins PG3 to PG0 are I/O ports, and their functions can be switched with PGDDR. • Mode 7 (when EXPE = 0) Pins PG6 to PG0 are I/O ports, and their functions can be switched with PGDDR.
5	PG5DDR	0	W	
4	PG4DDR	0	W	
3	PG3DDR	0	W	
2	PG2DDR	0	W	
1	PG1DDR	0	W	
0	PG0DDR	1/0*	W	

Note: * PG0DDR is initialized to 1 in modes 1 and 2, and to 0 in modes 4 and 7.

11.3.4 Timer Interrupt Enable Register (TIER)

TIER registers control enabling or disabling of interrupt requests for each channel. The TPU has six TIER registers, one for each channel.

Bit	Bit Name	Initial value	R/W	Description
7	TTGE	0	R/W	A/D Conversion Start Request Enable Enables or disables generation of A/D conversion start requests by TGRA input capture/compare match. 0: A/D conversion start request generation disabled 1: A/D conversion start request generation enabled
6	—	1	—	Reserved This bit is always read as 1 and cannot be modified.
5	TCIEU	0	R/W	Underflow Interrupt Enable Enables or disables interrupt requests (TCIU) by the TCFU flag when the TCFU flag in TSR is set to 1 in channels 1, 2, 4, and 5. In channels 0 and 3, bit 5 is reserved. It is always read as 0 and cannot be modified. 0: Interrupt requests (TCIU) by TCFU disabled 1: Interrupt requests (TCIU) by TCFU enabled
4	TCIEV	0	R/W	Overflow Interrupt Enable Enables or disables interrupt requests (TCIV) by the TCFV flag when the TCFV flag in TSR is set to 1. 0: Interrupt requests (TCIV) by TCFV disabled 1: Interrupt requests (TCIV) by TCFV enabled
3	TGIED	0	R/W	TGR Interrupt Enable D Enables or disables interrupt requests (TGID) by the TGFD bit when the TGFD bit in TSR is set to 1 in channels 0 and 3. In channels 1, 2, 4, and 5, bit 3 is reserved. It is always read as 0 and cannot be modified. 0: Interrupt requests (TGID) by TGFD bit disabled 1: Interrupt requests (TGID) by TGFD bit enabled

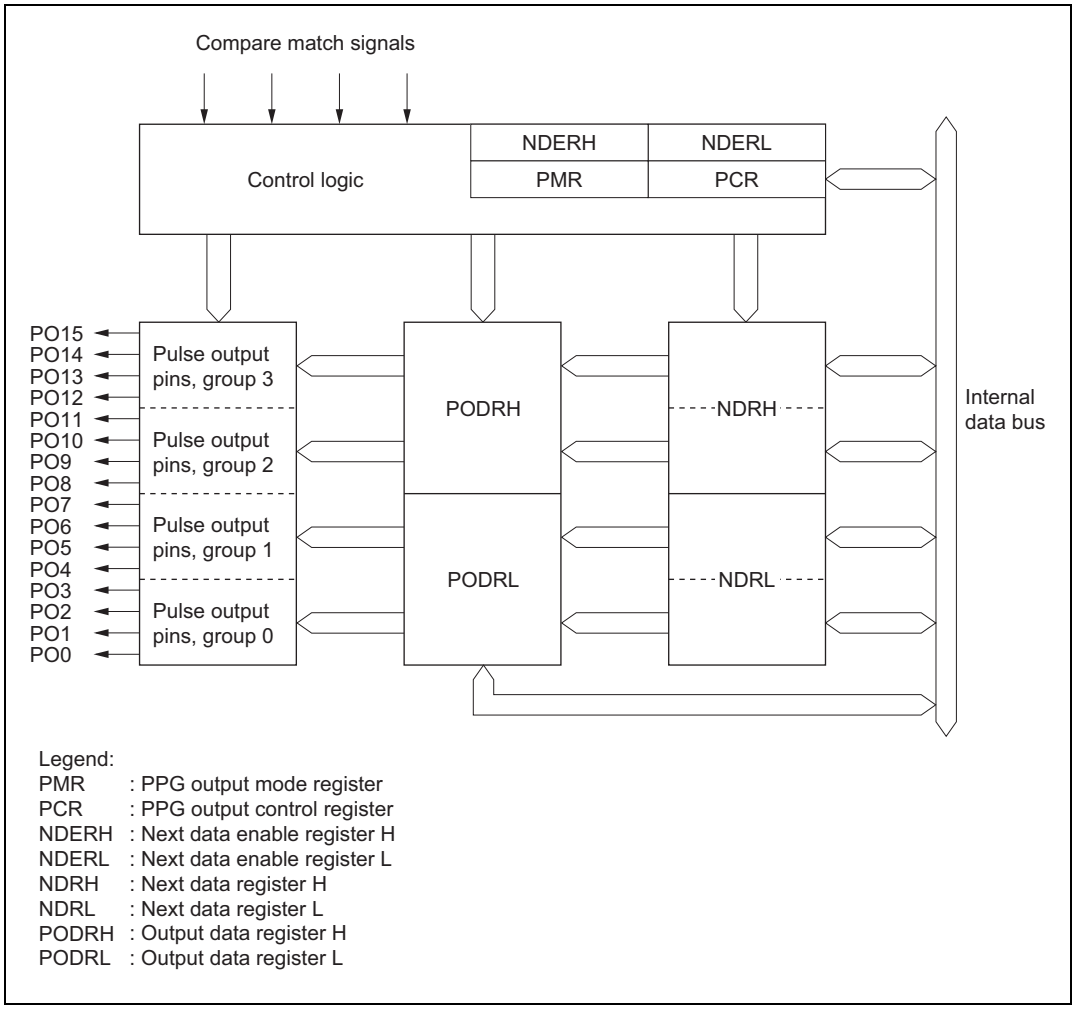


Figure 12.1 Block Diagram of PPG

Figure 13.1 shows a block diagram of the 8-bit timer module (TMR_0 and TMR_1).

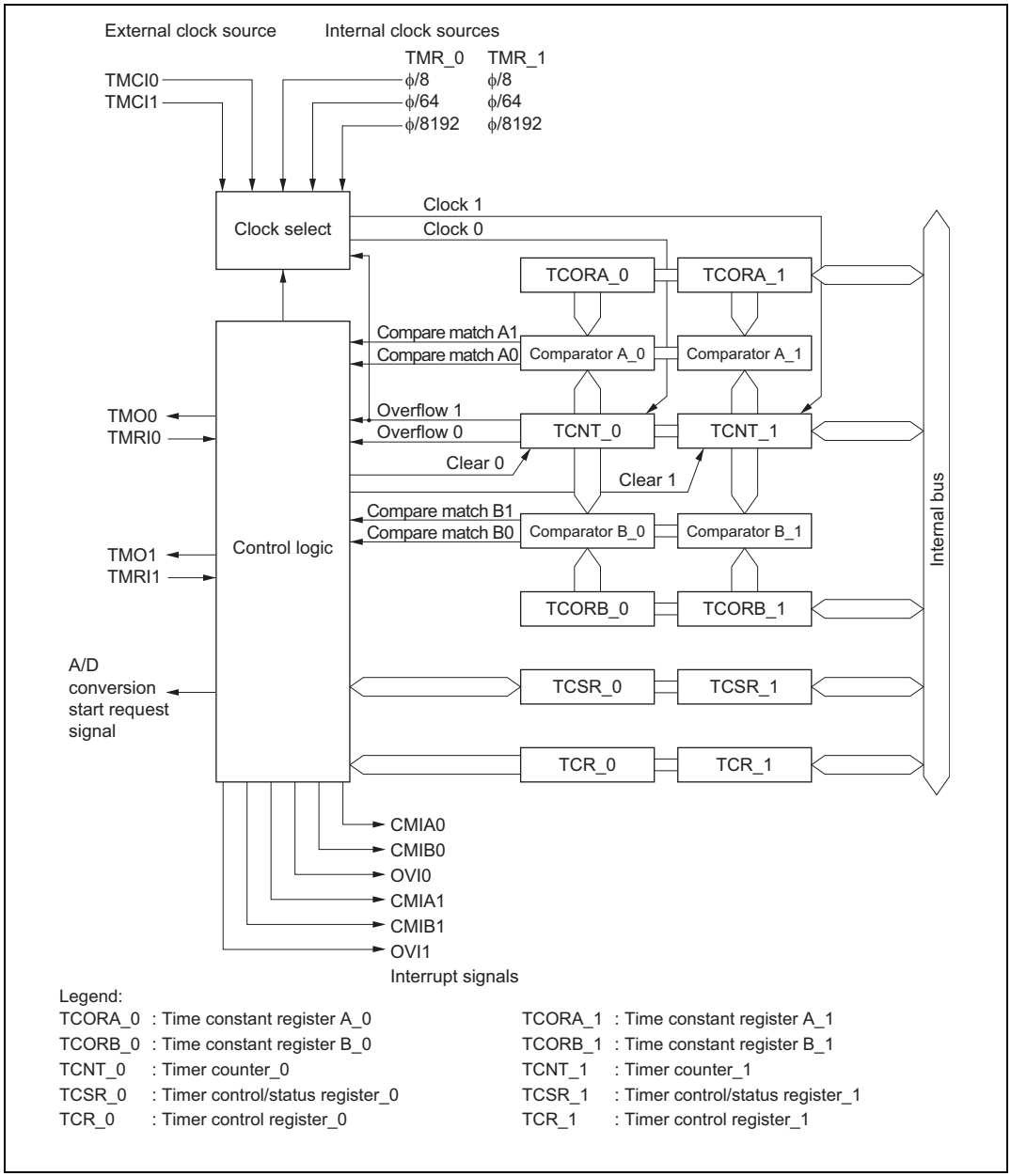


Figure 13.1 Block Diagram of 8-Bit Timer Module

15.3.8 Smart Card Mode Register (SCMR)

SCMR selects Smart Card interface mode and its format.

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 1	—	Reserved These bits are always read as 1.
3	SDIR	0	R/W	Smart Card Data Transfer Direction Selects the serial/parallel conversion format. 0: LSB-first in transfer 1: MSB-first in transfer The bit setting is valid only when the transfer data format is 8 bits. For 7-bit data, LSB-first is fixed.
2	SINV	0	R/W	Smart Card Data Invert Specifies inversion of the data logic level. The SINV bit does not affect the logic level of the parity bit. To invert the parity bit, invert the O/$\overline{E}$ bit in SMR. 0: TDR contents are transmitted as they are. Receive data is stored as it is in RDR. 1: TDR contents are inverted before being transmitted. Receive data is stored in inverted form in RDR.
1	—	1	—	Reserved This bit is always read as 1.
0	SMIF	0	R/W	Smart Card Interface Mode Select This bit is set to 1 to make the SCI operate in Smart Card interface mode. 0: Normal asynchronous mode or clocked synchronous mode 1: Smart card interface mode

- Programming Data (128 bytes): Data to be programmed
  The size is specified in the response to the programming unit inquiry.
- SUM (one byte): Checksum

Response

H'06

- Response, H'06, (one byte): Response to 128-byte programming
  On completion of programming, the boot program will return ACK.

Error Response

H'D0	ERROR

- Error response, H'D0, (one byte): Error response for 128-byte programming
- ERROR: (one byte): Error code
  H'11: Checksum Error
  H'2A: Address error
  The address is not within the specified MAT.
  H'53: Programming error
  A programming error has occurred and programming cannot be continued.

The specified address should match the unit for programming of data. For example, when the programming is in 128-byte units, the lower byte of the address should be H'00 or H'80. When there are less than 128 bytes of data to be programmed, the host should fill the rest with H'FF.

Sending the 128-byte programming command with the address of H'FFFFFFFF will stop the programming operation. The boot program will interpret this as the end of the programming and wait for selection of programming or erasing.

Command

H'50	Address	SUM

- Command, H'50, (one byte): 128-byte programming
- Programming Address (four bytes): End code is H'FF, H'FF, H'FF, H'FF.
- SUM (one byte): Checksum

Response

H'06

- Response, H'06, (one byte): Response to 128-byte programming
  On completion of programming, the boot program will return ACK.

Error Response

H'D0	ERROR

- Error Response, H'D0, (one byte): Error response for 128-byte programming

Section 25 List of Registers

The address list gives information on the on-chip I/O register addresses, how the register bits are configured, and the register states in each operating mode. The information is given as shown below.

1. Register addresses (address order)
- Registers are listed from the lower allocation addresses.
- Reserved addresses are indicated by — in the register name column. Do not access to reserved addresses.
- For the addresses of 16 or 32 bits, the MSB-side address is described.
- Registers are classified by functional modules.
- The access size is indicated.

2. Register bits
- Bit configurations of the registers are described in the same order as the register addresses.
- Reserved bits are indicated by — in the bit name column.
- For the registers of 16 or 32 bits, the MSB is described first.

3. Register states in each operating mode
- Register states are described in the same order as the register addresses.
- The register states described here are for the basic operating modes. If there is a specific reset for an on-chip peripheral module, refer to the section on that on-chip peripheral module.

25.1 Register Addresses (Address Order)

The data bus width indicates the numbers of bits by which the register is accessed.

The number of access states indicates the number of states based on the specified reference clock.

Table 26.8 Bus Timing (2)

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 33 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{WR}$ delay time 1	t_{WRD1}	—	15	ns	Figures 26.7 to 26.22
$\overline{WR}$ delay time 2	t_{WRD2}	—	15	ns	
$\overline{WR}$ pulse width 1	t_{WSW1}	1.0 × t_{cyc} –13	—	ns	
$\overline{WR}$ pulse width 2	t_{WSW2}	1.5 × t_{cyc} –13	—	ns	
Write data delay time	t_{WDD}	—	20	ns	
Write data setup time 1	t_{WDS1}	0.5 × t_{cyc} –15	—	ns	
Write data setup time 2	t_{WDS2}	1.0 × t_{cyc} –15	—	ns	
Write data setup time 3	t_{WDS3}	1.5 × t_{cyc} –15	—	ns	
Write data hold time 1	t_{WDH1}	0.5 × t_{cyc} –8	—	ns	
Write data hold time 2	t_{WDH2}	1.0 × t_{cyc} –8	—	ns	
Write data hold time 3	t_{WDH3}	1.5 × t_{cyc} –8	—	ns	
Write command setup time 1	t_{WCS1}	0.5 × t_{cyc} –10	—	ns	
Write command setup time 2	t_{WCS2}	1.0 × t_{cyc} –10	—	ns	
Write command hold time 1	t_{WCH1}	0.5 × t_{cyc} –10	—	ns	
Write command hold time 2	t_{WCH2}	1.0 × t_{cyc} –10	—	ns	
Read command setup time 1	t_{RCS1}	1.5 × t_{cyc} –10	—	ns	
Read command setup time 2	t_{RCS2}	2.0 × t_{cyc} –10	—	ns	
Read command hold time	t_{RCH}	0.5 × t_{cyc} –10	—	ns	
$\overline{CAS}$ delay time 1	t_{CASD1}	—	15	ns	
$\overline{CAS}$ delay time 2	t_{CASD2}	—	15	ns	
$\overline{CAS}$ setup time 1	t_{CSR1}	0.5 × t_{cyc} –10	—	ns	
$\overline{CAS}$ setup time 2	t_{CSR2}	1.5 × t_{cyc} –10	—	ns	
$\overline{CAS}$ pulse width 1	t_{CASW1}	1.0 × t_{cyc} –20	—	ns	
$\overline{CAS}$ pulse width 2	t_{CASW2}	1.5 × t_{cyc} –20	—	ns	
$\overline{CAS}$ precharge time 1	t_{CPW1}	1.0 × t_{cyc} –20	—	ns	
$\overline{CAS}$ precharge time 2	t_{CPW2}	1.5 × t_{cyc} –20	—	ns	
$\overline{OE}$ delay time 1	t_{OED1}	—	15	ns	
$\overline{OE}$ delay time 2	t_{OED2}	—	15	ns	
Precharge time 1	t_{PCH1}	1.0 × t_{cyc} –20	—	ns	
Precharge time 2	t_{PCH2}	1.5 × t_{cyc} –20	—	ns	

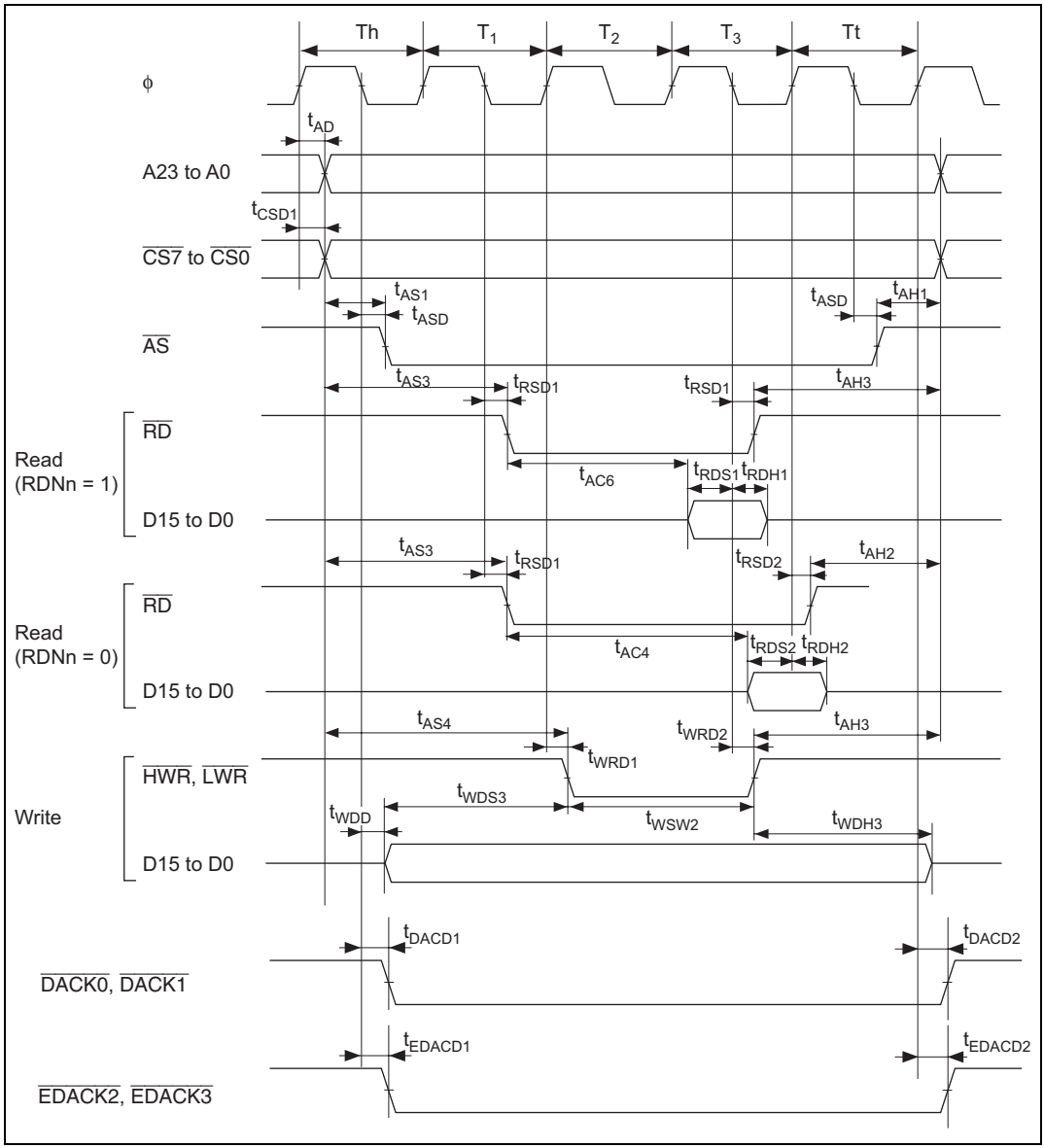


Figure 26.11 Basic Bus Timing: Three-State Access ($\overline{CS}$ Assertion Period Extended)

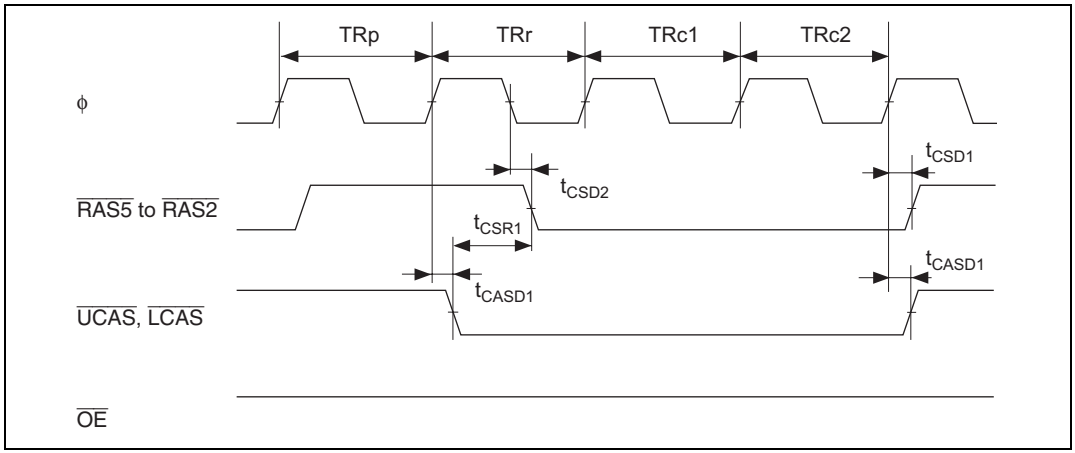


Figure 26.19 CAS-Before-RAS Refresh Timing

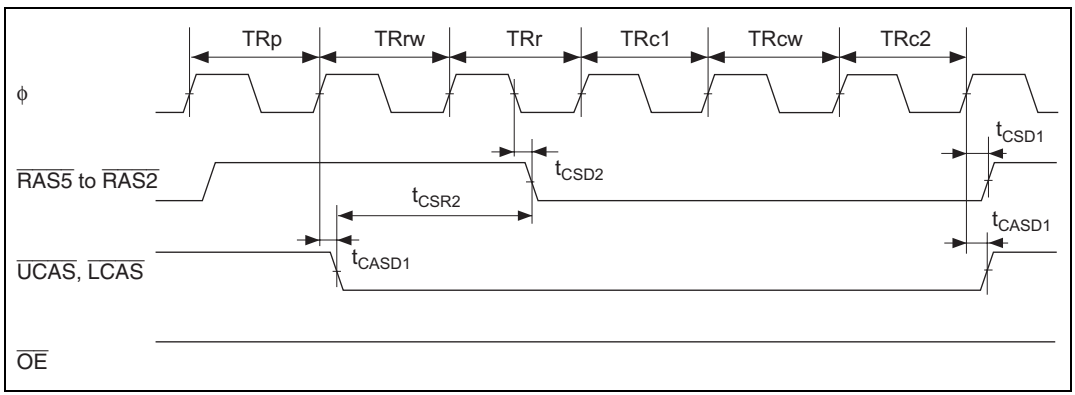


Figure 26.20 CAS-Before-RAS Refresh Timing (with Wait Cycle Insertion)