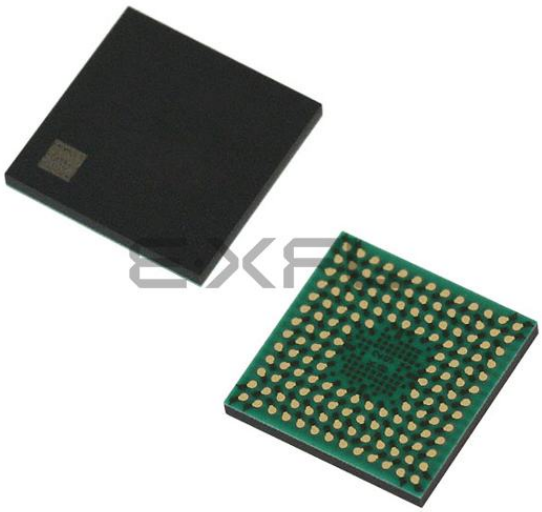

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	384KB (384K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2374vlp34v

In order to understand the details of the CPU's functions

Read the H8S/2600 Series, H8S/2000 Series Software Manual.

For the execution state of each instruction in this LSI, see Appendix D, Bus State during Execution of Instructions.

In order to understand the details of a register when its name is known

Read the index that is the final part of the manual to find the page number of the entry on the register. The addresses, bits, and initial values of the registers are summarized in section 25, List of Registers.

Examples:		
	Register name:	The following notation is used for cases when the same or a similar function, e.g. 16-bit timer pulse unit or serial communication, is implemented on more than one channel: XXX_N (XXX is the register name and N is the channel number)
	Bit order:	The MSB is on the left and the LSB is on the right.
	Number notation:	Binary is B'xxxx, hexadecimal is H'xxxx, decimal is xxxx.
	Signal notation:	An overbar is added to a low-active signal: $\overline{\text{xxxx}}$

Related Manuals: The latest versions of all related manuals are available from our web site. Please ensure you have the latest versions of all documents you require. http://www.renesas.com/

H8S/2378 Group and H8S/2378R Group Manuals:

Document Title	Document No.
H8S/2378 Group,H8S/2378R Group Hardware Manual	This manual
H8S/2600 Series, H8S/2000 Series Software Manual	REJ09B0139

User's Manuals for Development Tools:

Document Title	Document No.
H8S, H8/300 Series C/C++ Compiler, Assembler, Optimizing Linkage Editor Compiler Package V.6.01 User's Manual	REJ10B0161
H8S, H8/300 Series Simulator/Debugger User's Manual	REJ10B0211
H8S, H8/300 Series High-performance Embedded Workshop, High-performance Debugging Interface V.3 Tutorial	REJ10B0024
High-performance Embedded Workshop V.4.04 User's Manual	REJ10J1737

Section 5 Interrupt Controller

5.1 Features

- Two interrupt control modes

  Any of two interrupt control modes can be set by means of the INTM1 and INTM0 bits in the interrupt control register (INTCR).
- Priorities settable with IPR

  An interrupt priority register (IPR) is provided for setting interrupt priorities. Eight priority levels can be set for each module for all interrupts except NMI. NMI is assigned the highest priority level of 8, and can be accepted at all times.
- Independent vector addresses

  All interrupt sources are assigned independent vector addresses, making it unnecessary for the source to be identified in the interrupt handling routine.
- Seventeen external interrupts

  NMI is the highest-priority interrupt, and is accepted at all times. Rising edge or falling edge can be selected for NMI. Falling edge, rising edge, or both edge detection, or level sensing, can be selected for $\overline{\text{IRQ15}}$ to $\overline{\text{IRQ0}}$.
- DTC and DMAC control

  DTC and DMAC activations are performed by means of interrupts.

5.6.2 Interrupt Control Mode 2

In interrupt control mode 2, mask control is done in eight levels for interrupt requests except for NMI by comparing the EXR interrupt mask level (I2 to I0 bits) in the CPU and the IPR setting. Figure 5.4 shows a flowchart of the interrupt acceptance operation in this case.

1. If an interrupt source occurs when the corresponding interrupt enable bit is set to 1, an interrupt request is sent to the interrupt controller.
2. When interrupt requests are sent to the interrupt controller, the interrupt with the highest priority according to the interrupt priority levels set in IPR is selected, and lower-priority interrupt requests are held pending. If a number of interrupt requests with the same priority are generated at the same time, the interrupt request with the highest priority according to the priority system shown in table 5.2 is selected.
3. Next, the priority of the selected interrupt request is compared with the interrupt mask level set in EXR. An interrupt request with a priority no higher than the mask level set at that time is held pending, and only an interrupt request with a priority higher than the interrupt mask level is accepted.
4. When the CPU accepts an interrupt request, it starts interrupt exception handling after execution of the current instruction has been completed.
5. The PC, CCR, and EXR are saved to the stack area by interrupt exception handling. The PC saved on the stack shows the address of the first instruction to be executed after returning from the interrupt handling routine.
6. The T bit in EXR is cleared to 0. The interrupt mask level is rewritten with the priority level of the accepted interrupt.

   If the accepted interrupt is NMI, the interrupt mask level is set to H'7.
7. The CPU generates a vector address for the accepted interrupt and starts execution of the interrupt handling routine at the address indicated by the contents of the vector address in the vector table.

6.11.2 Pin States in External Bus Released State

Table 6.13 shows pin states in the external bus released state.

Table 6.13 Pin States in Bus Released State

Pins	Pin State
A23 to A0	High impedance
D15 to D0	High impedance
$\overline{\text{CSn}}$ (n = 7 to 0)	High impedance
$\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$	High impedance
$\overline{\text{AS}}$	High impedance
$\overline{\text{RD}}$	High impedance
($\overline{\text{OE}}$)	High impedance
$\overline{\text{HWR}}$, $\overline{\text{LWR}}$	High impedance
$\overline{\text{DACKn}}$ (n = 1, 0)	High
$\overline{\text{EDACKn}}$ (n = 3 to 0)	High

accessed next. Bits SAT1 and SAT0 in EDACR specify incrementing or decrementing. The address is fixed when SAT1 = 0, incremented when SAT1 = 1 and SAT0 = 0, and decremented when SAT1 = 1 and SAT0 = 1.

The size of the increment or decrement is determined by the size of the data transferred. When the DTSIZE bit in EDMDR = 0, the data is byte-size and the address is incremented or decremented by 1; when DTSIZE = 1, the data is word-size and the address is incremented or decremented by 2.

When a repeat area setting is made, the operation conforms to that setting. The upper part of the address set for the repeat area function is fixed, and is not affected by address updating.

When EDSAR is read during a transfer operation, a longword access must be used. During a transfer operation, EDSAR may be updated without regard to accesses from the CPU, and the correct values may not be read if the upper and lower words are read separately. In a longword access, the EXDMAC buffers the EDSAR value to ensure that the correct value is output.

Do not write to EDSAR for a channel on which a transfer operation is in progress.

EXDMA Destination Address Register (EDDAR): When the EDDAR address is accessed as the transfer destination, after the EDDAR value is output, EDDAR is updated with the address to be accessed next. Bits DAT1 and DAT0 in EDACR specify incrementing or decrementing. The address is fixed when DAT1 = 0, incremented when DAT1 = 1 and DAT0 = 0, and decremented when DAT1 = 1 and DAT0 = 1.

The size of the increment or decrement is determined by the size of the data transferred. When the DTSIZE bit in EDMDR = 0, the data is byte-size and the address is incremented or decremented by 1; when DTSIZE = 1, the data is word-size and the address is incremented or decremented by 2.

When a repeat area setting is made, the operation conforms to that setting. The upper part of the address set for the repeat area function is fixed, and is not affected by address updating.

When EDDAR is read during a transfer operation, a longword access must be used. During a transfer operation, EDDAR may be updated without regard to accesses from the CPU, and the correct values may not be read if the upper and lower words are read separately. In a longword access, the EXDMAC buffers the EDDAR value to ensure that the correct value is output.

Do not write to EDDAR for a channel on which a transfer operation is in progress.

9.5.2 Repeat Mode

In repeat mode, one operation transfers one byte or one word of data. Table 9.5 lists the register function in repeat mode. From 1 to 256 transfers can be specified. Once the specified number of transfers has ended, the initial state of the transfer counter and the address register specified as the repeat area is restored, and transfer is repeated. In repeat mode the transfer counter value does not reach H'00, and therefore CPU interrupts cannot be requested when DISEL = 0.

Table 9.5 Register Function in Repeat Mode

Name	Abbreviation	Function
DTC source address register	SAR	Designates source address
DTC destination address register	DAR	Designates destination address
DTC transfer count register AH	CRAH	Holds number of transfers
DTC transfer count register AL	CRAL	Designates transfer count
DTC transfer count register B	CRB	Not used

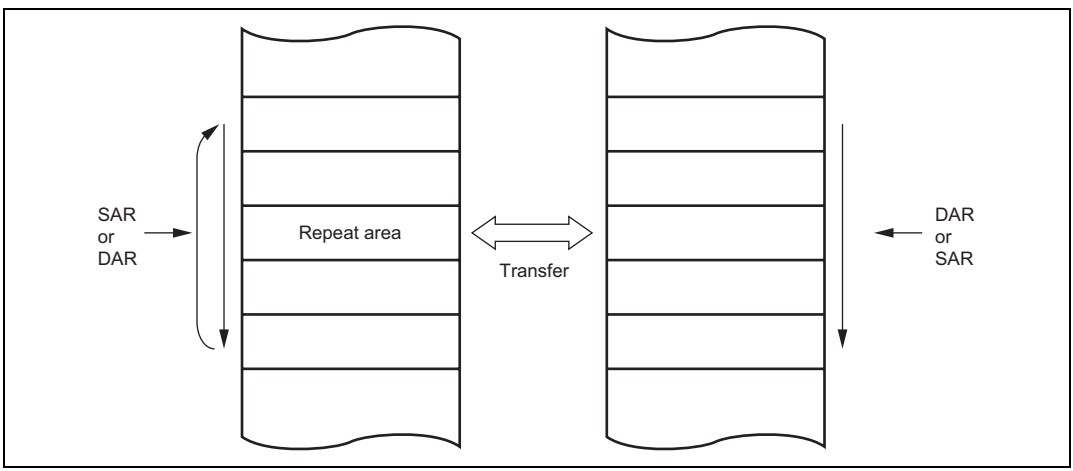

Figure 9.7 Memory Mapping in Repeat Mode

- PF4/$\overline{\text{HWR}}$

  The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PF4DDR.

Operating mode	1, 2, 4	7		
EXPE	—	0		1
PF4DDR	—	0	1	—
Pin function	$\overline{\text{HWR}}$ output	PF4 input	PF4 output	$\overline{\text{HWR}}$ output

- PF3/$\overline{\text{LWR}}$

  The pin function is switched as shown below according to the operating mode, bit EXPE, bit LWROE, and bit PF3DDR.

Operating mode	1, 2, 4			7				
EXPE	—			0		1		
LWROD	1	0		—		1	0	
PF3DDR	—	0	1	0	1	—	0	1
Pin function	$\overline{\text{LWR}}$ output	PF3 input	PF3 output	PF3 input	PF3 output	$\overline{\text{LWR}}$ output	PF3 input	PF3 output

12.4.7 Inverted Pulse Output

If the G3INV, G2INV, G1INV, and G0INV bits in PMR are cleared to 0, values that are the inverse of the PODR contents can be output.

Figure 12.10 shows the outputs when G3INV and G2INV are cleared to 0, in addition to the settings of figure 12.9.

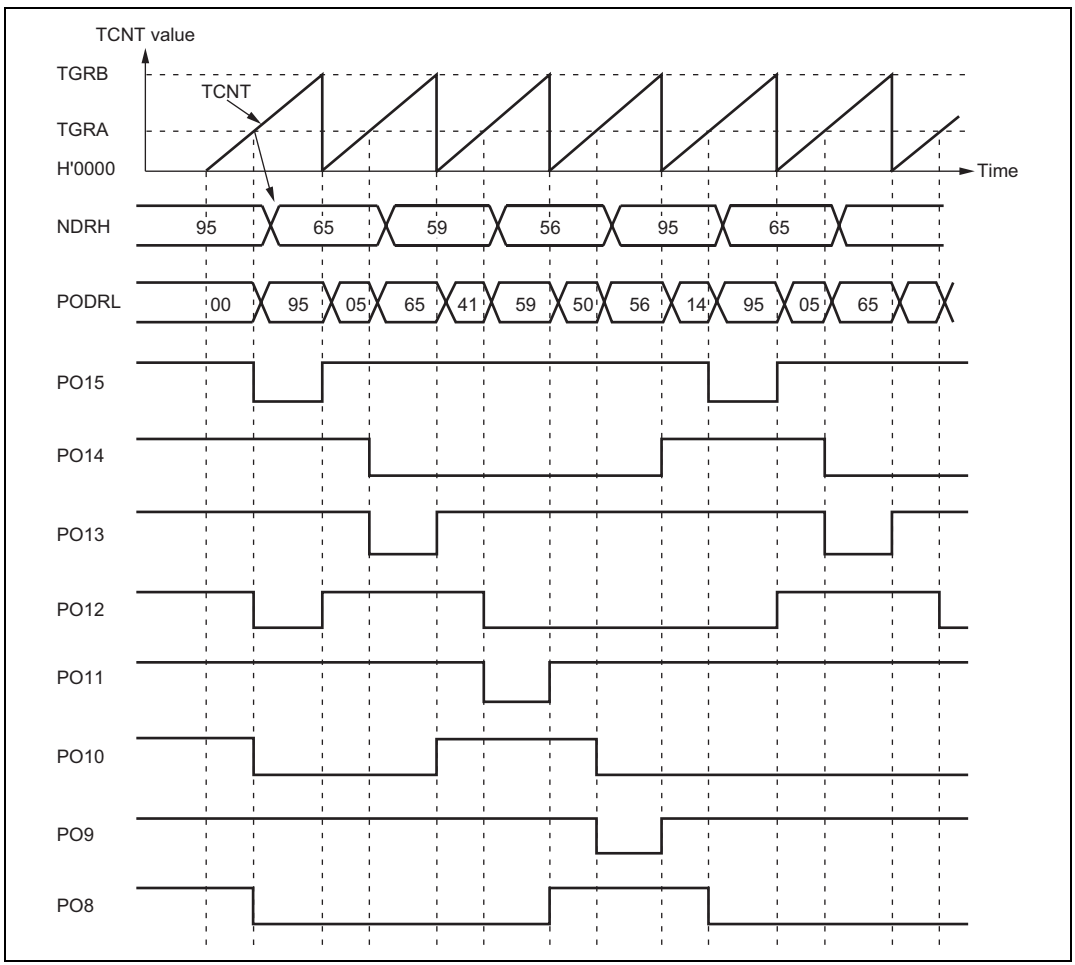

Figure 12.10 Inverted Pulse Output (Example)

13.5.2 Timing of CMFA and CMFB Setting when Compare-Match Occurs

The CMFA and CMFB flags in TCSR are set to 1 by a compare match signal generated when the TCOR and TCNT values match. The compare match signal is generated at the last state in which the match is true, just before the timer counter is updated. Therefore, when TCOR and TCNT match, the compare match signal is not generated until the next incrementation clock input. Figure 13.5 shows this timing.

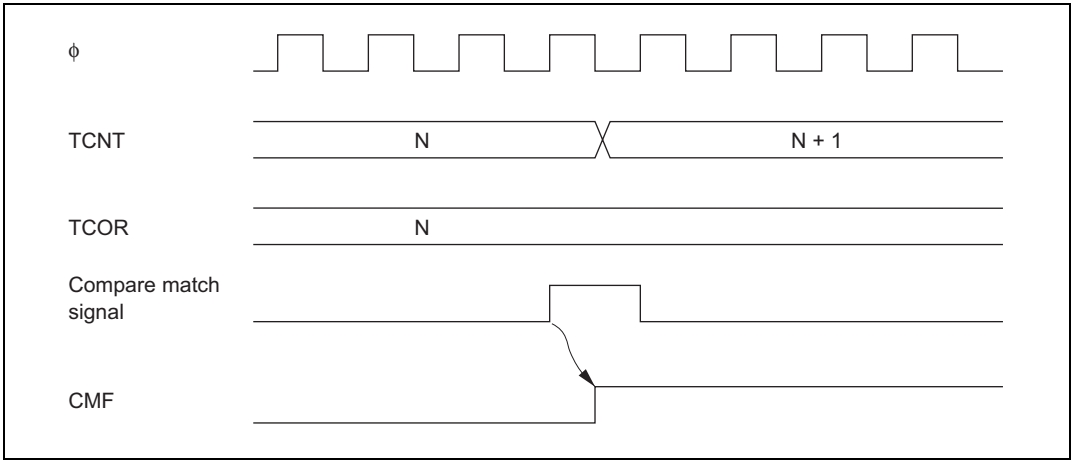

Figure 13.5 Timing of CMF Setting

13.8.2 Contention between TCNT Write and Increment

If a timer counter clock pulse is generated during the T_2 state of a TCNT write cycle, the write takes priority and the counter is not incremented.

Figure 13.11 shows this operation.

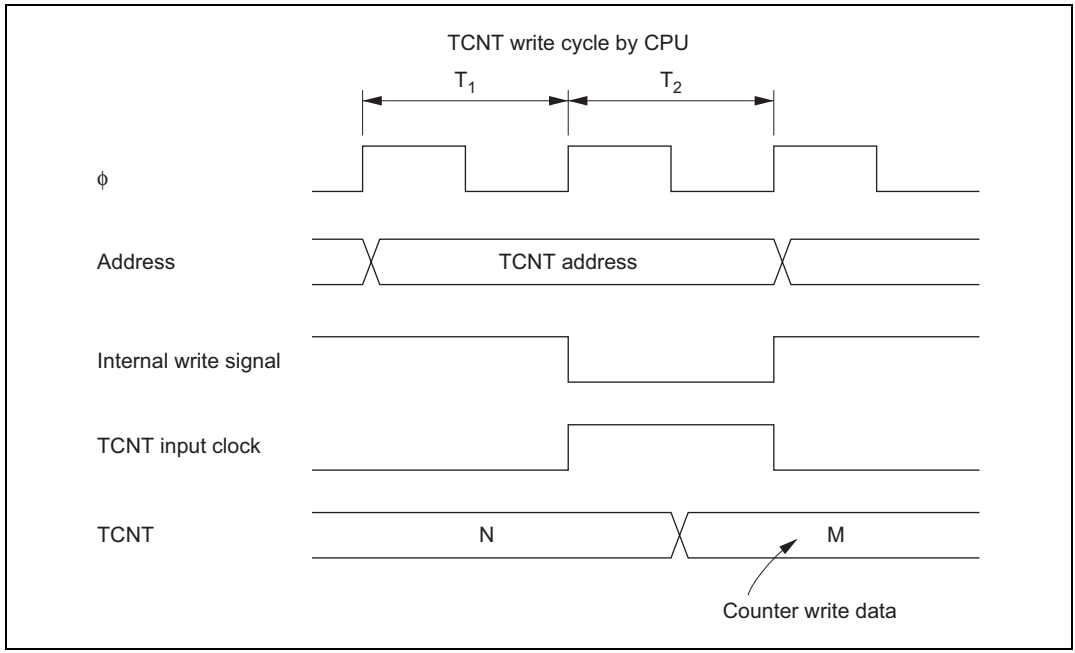

Figure 13.11 Contention between TCNT Write and Increment

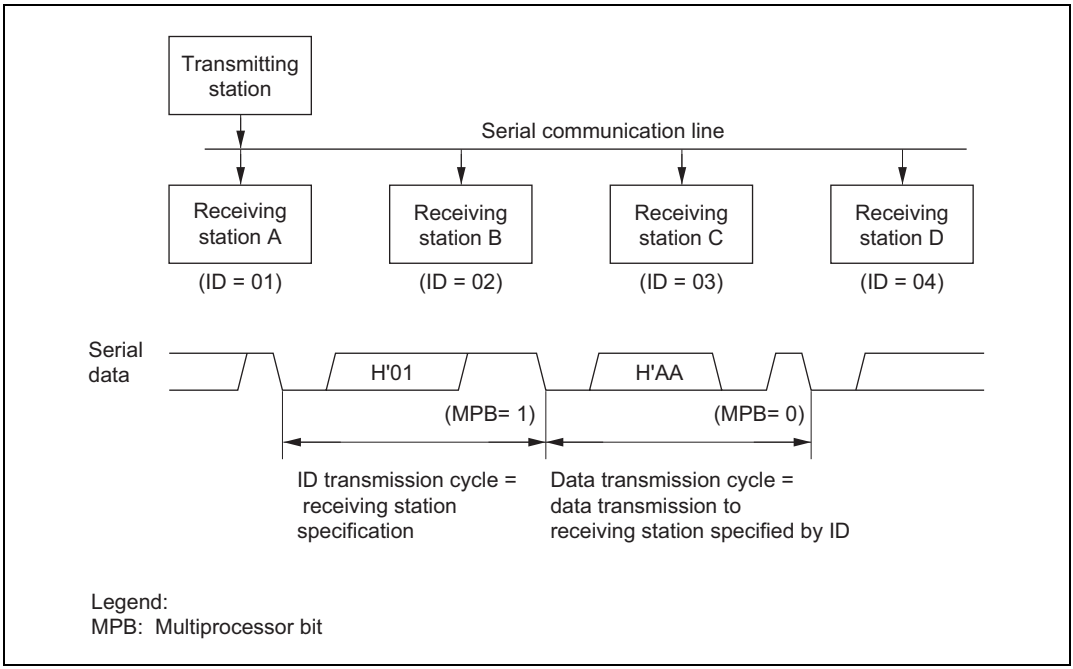

Figure 15.10 Example of Communication Using Multiprocessor Format (Transmission of Data H'AA to Receiving Station A)

15.5.1 Multiprocessor Serial Data Transmission

Figure 15.11 shows a sample flowchart for multiprocessor serial data transmission. For an ID transmission cycle, set the MPBT bit in SSR to 1 before transmission. For a data transmission cycle, clear the MPBT bit in SSR to 0 before transmission. All other SCI operations are the same as those in asynchronous mode.

16.6 Bit Synchronous Circuit

In master mode,

- When SCL is driven to low by the slave device
- When the rising speed of SCL is lower by the load of the SCL line (load capacitance or pull-up resistance)

This module has a possibility that high level period may be short in the two states described above. Therefore it monitors SCL and communicates by bit with synchronization.

Figure 16.18 shows the timing of the bit synchronous circuit and table 16.4 shows the time when SCL output changes from low to Hi-Z then SCL is monitored.

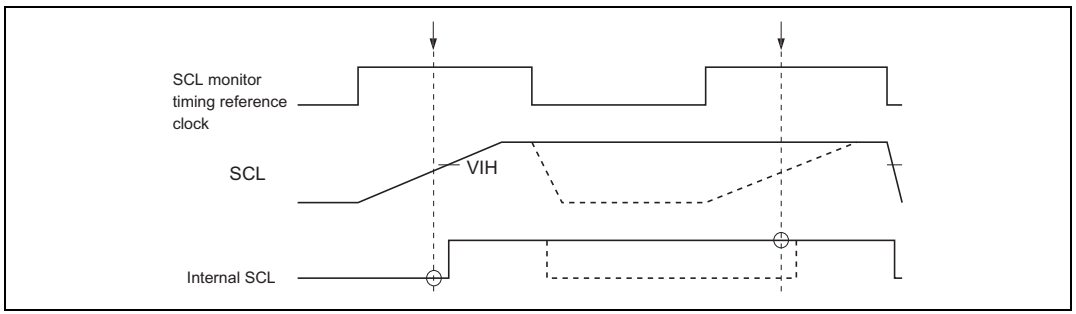

Figure 16.18 Timing of the Bit Synchronous Circuit

Table 16.4 Time for monitoring SCL

CKS3	CKS2	Time for monitoring SCL
0	0	7.5 tcyc
	1	19.5 tcyc
1	0	17.5 tcyc
	1	41.5 tcyc

23.3 PLL Circuit

The PLL circuit has the function of multiplying the frequency of the clock from the oscillator by a factor of 1, 2, or 4. The multiplication factor is set with the STC1 and the STC0 bits in PLLCR. The phase of the rising edge of the internal clock is controlled so as to match that of the rising edge of the EXTAL pin.

When the multiplication factor of the PLL circuit is changed, the operation varies according to the setting of the STCS bit in SCKCR.

When STCS = 0, the setting becomes valid after a transition to software standby mode. The transition time count is performed in accordance with the setting of bits STS3 to STS0 in SBYCR. For details on SBYCR, refer to section 24.1.1, Standby Control Register (SBYCR).

1. The initial PLL circuit multiplication factor is 1.
2. A value is set in bits STS3 to STS0 to give the specified transition time.
3. The target value is set in bits STC1 and STC0, and a transition is made to software standby mode.
4. The clock pulse generator stops and the value set in STC1 and STC0 becomes valid.
5. Software standby mode is cleared, and a transition time is secured in accordance with the setting in STS3 to STS0.
6. After the set transition time has elapsed, this LSI resumes operation using the target multiplication factor.

When STCS = 1, this LSI operates using the new multiplication factor immediately after bits STC1 and STC0 are rewritten.

23.4 Frequency Divider

The frequency divider divides the PLL output clock to generate a 1/2, 1/4, or 1/8 clock.

- MSTPCRL

Bit	Bit Name	Initial Value	R/W	Module
7	MSTP7	1	R/W	D/A converter (channels 4 and 5)*
6	MSTP6	1	R/W	A/D converter
5	MSTP5	1	R/W	Serial communication interface 4 (SCI_4)
4	MSTP4	1	R/W	Serial communication interface 3 (SCI_3)
3	MSTP3	1	R/W	Serial communication interface 2 (SCI_2)
2	MSTP2	1	R/W	Serial communication interface 1 (SCI_1)
1	MSTP1	1	R/W	Serial communication interface 0 (SCI_0)
0	MSTP0	1	R/W	8-bit timer (TMR)

Note: * Not supported by the H8S2375, H8S/2575R, H8S/2373, and H8S/2373R.

24.1.3 Extension Module Stop Control Registers H and L (EXMSTPCRH, EXMSTPCRL)

EXMSTPCR performs all-module-clocks-stop mode control with MSTPCR.

When entering all-module-clocks-stop mode, set EXMSTPCR to H'FFFF. Otherwise, set EXMSTPCR to H'FFFD.

- EXMSTPCRH

Bit	Bit Name	Initial Value	R/W	Module
15 to 12	—	All 1	R/W	Reserved Read/write is enabled. 1 should be written in writing.
11	MSTP27	1	R/W	—
10	MSTP26	1	R/W	—
9	MSTP25	1	R/W	—
8	MSTP24	1	R/W	—

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access States
DMA control register 0A	DMACR_0A	8	H'FF22	DMAC	16	2
DMA control register 0B	DMACR_0B	8	H'FF23	DMAC	16	2
DMA control register 1A	DMACR_1A	8	H'FF24	DMAC	16	2
DMA control register 1B	DMACR_1B	8	H'FF25	DMAC	16	2
DMA band control register H	DMABCRH	8	H'FF26	DMAC	16	2
DMA band control register L	DMABCRL	8	H'FF27	DMAC	16	2
DTC enable register A	DTCERA	8	H'FF28	DTC	16	2
DTC enable register B	DTCERB	8	H'FF29	DTC	16	2
DTC enable register C	DTCERC	8	H'FF2A	DTC	16	2
DTC enable register D	DTCERD	8	H'FF2B	DTC	16	2
DTC enable register E	DTCERE	8	H'FF2C	DTC	16	2
DTC enable register F	DTCERF	8	H'FF2D	DTC	16	2
DTC enable register G	DTCERG	8	H'FF2E	DTC	16	2
DTC enable register H	DTCERH	8	H'FF2F	DTC	16	2
DTC vector register	DTVECR	8	H'FF30	DTC	16	2
Interrupt control register	INTCR	8	H'FF31	INT	16	2
IRQ enable register	IER	16	H'FF32	INT	16	2
IRQ status register	ISR	16	H'FF34	INT	16	2
Standby control register	SBYCR	8	H'FF3A	SYSTEM	8	2
System clock control register	SCKCR	8	H'FF3B	SYSTEM	8	2
System control register	SYSCR	8	H'FF3D	SYSTEM	8	2
Mode control register	MDCR	8	H'FF3E	SYSTEM	8	2
Module stop control register H	MSTPCRH	8	H'FF40	SYSTEM	8	2
Module stop control register L	MSTPCRL	8	H'FF41	SYSTEM	8	2
Extension module stop control register H	EXMSTPCRH	8	H'FF42	SYSTEM	8	2
Extension module stop control register L	EXMSTPCRL	8	H'FF43	SYSTEM	8	2
PLL control register	PLLCR	8	H'FF45	SYSTEM	8	2
PPG output control register	PCR	8	H'FF46	PPG	8	2
PPG output mode register	PMR	8	H'FF47	PPG	8	2
Next data enable register H	NDERH	8	H'FF48	PPG	8	2

(4) DMAC and EXDMAC Timing

Table 26.22 DMAC and EXDMAC Timing

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V, ϕ = 8 MHz to 35 MHz, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item	Symbol	Min.	Max.	Unit	Test Conditions
$\overline{\text{DREQ}}$ setup time	t_{DRQS}	25	—	ns	Figure 26.31
$\overline{\text{DREQ}}$ hold time	t_{DRQH}	10	—		
$\overline{\text{TEND}}$ delay time	t_{TED}	—	18	ns	Figure 26.30
$\overline{\text{DACK}}$ delay time 1	t_{DACD1}	—	18		Figures 26.28 and 26.29
$\overline{\text{DACK}}$ delay time 2	t_{DACD2}	—	18		
$\overline{\text{EDREQ}}$ setup time	t_{EDRQS}	25	—	ns	Figure 26.31
$\overline{\text{EDREQ}}$ hold time	t_{EDRQH}	10	—		
$\overline{\text{ETEND}}$ delay time	t_{ETED}	—	18	ns	Figure 26.30
$\overline{\text{EDACK}}$ delay time 1	t_{EDACD1}	—	18		Figure 26.28 and 26.29
$\overline{\text{EDACK}}$ delay time 2	t_{EDACD2}	—	18		
$\overline{\text{EDRAK}}$ delay time	t_{EDRKD}	—	18	ns	Figure 26.32

26.3.2 DC Characteristics

Table 26.28 DC Characteristics

Conditions: V_{CC} = 3.0 V to 3.6 V, AV_{CC} = 3.0 V to 3.6 V, V_{ref} = 3.0 V to AV_{CC}, V_{SS} = AV_{SS} = 0 V*1, T_a = –20°C to +75°C (regular specifications), T_a = –40°C to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Schmitt trigger input voltage	Port 1, port 2, P50 to P53*2, port 6*2, port 8*2, PA4 to PA7*2, PF1*2, PF2*2, PH2*2, PH3*2	VT^-	$V_{CC} \times 0.2$	—	—	V	
		VT^+	—	—	$V_{CC} \times 0.7$	V	
		$VT^+ - VT^-$	$V_{CC} \times 0.07$	—	—	V	
Input high voltage	$\overline{STBY}$, MD2 to MD0	V_{IH}	$V_{CC} \times 0.9$	—	V_{CC} +0.3	V	
	$\overline{RES}$, NMI, EMLE		$V_{CC} \times 0.9$	—	V_{CC} +0.3	V	
	EXTAL		$V_{CC} \times 0.7$	—	V_{CC} +0.3	V	
	Port 3, P50 to P53*3, ports 6*3 and 8*3, ports A to H*3		2.2	—	V_{CC} +0.3	V	
	Port 4, Port 9		2.2	—	AV_{CC} +0.3	V	
Input low voltage	$\overline{RES}$, $\overline{STBY}$, MD2 to MD0, EMLE	V_{IL}	–0.3	—	$V_{CC} \times 0.1$	V	
	NMI, EXTAL		–0.3	—	$V_{CC} \times 0.2$	V	
	Ports 3 to 6*3, Port 8*3, ports A to H*3, port 9		–0.3	—	$V_{CC} \times 0.2$	V	
Output high voltage	All output pins	V_{OH}	V_{CC} –0.5	—	—	V	I_{OH} = –200 μA
			V_{CC} –1.0	—	—	V	I_{OH} = –1 mA
Output low voltage	All output pins	V_{OL}	—	—	0.4	V	I_{OL} = 1.6 mA
	P32 to P35*4		—	—	0.5	V	I_{OL} = 8.0 mA

Notes: 1. When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.
2. When used as $\overline{IRQ0}$ to $\overline{IRQ15}$.
3. When used as other than $\overline{IRQ0}$ to $\overline{IRQ15}$.
4. When used as SCL0, SCL1, SDA0, and SDA1.

Item	Symbol	Min.	Max.	Unit	Test Conditions
Address read data access time 1	T_{AA1}	—	$1.0 \times t_{cyc} - 25$	ns	Figures 26.7 to 26.20, 26.25
Address read data access time 2	T_{AA2}	—	$1.5 \times t_{cyc} - 25$	ns	
Address read data access time 3	T_{AA3}	—	$2.0 \times t_{cyc} - 25$	ns	
Address read data access time 4	T_{AA4}	—	$2.5 \times t_{cyc} - 25$	ns	
Address read data access time 5	T_{AA5}	—	$3.0 \times t_{cyc} - 25$	ns	