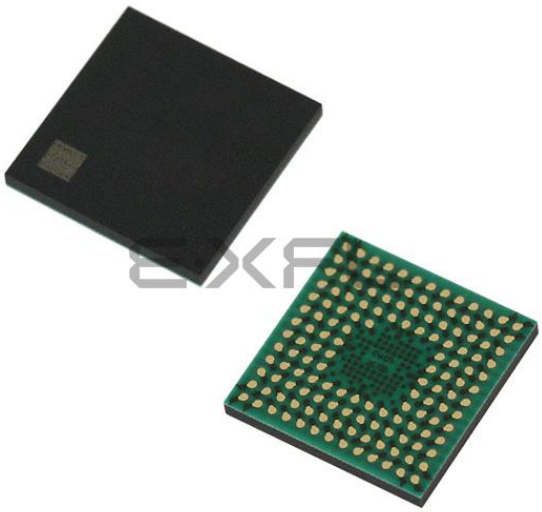

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	35MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2378bvlp35v

		Pin No.					
Type	**Symbol**	**H8S/2378 0.18µm F-ZTAT Group, H8S/2378R 0.18µm F-ZTAT Group (LQFP-144)**	**H8S/2378 0.18µm F-ZTAT Group, H8S/2378R 0.18µm F-ZTAT Group (LGA-145)**	**H8S/2377 H8S/2377R**	**H8S/2375 H8S/2373 H8S/2375R H8S/2373R**	**I/O**	**Function**
Clock	XTAL	96	F13	96	96	Input	For connection to a crystal oscillator. See section 23, Clock Pulse Generator, for typical connection diagrams for a crystal resonator and external clock input.
	EXTAL	97	E13	97	97	Input	For connection to a crystal oscillator. The EXTAL pin can also input an external clock. See section 23, Clock Pulse Generator, for typical connection diagrams for a crystal resonator and external clock input.
	ϕ	94	F10	94	94	Output	Supplies the system clock to external devices.
	SDRAMϕ[*1]	36	M1	36	36	Output	When a synchro-nous DRAM is connected, this pin is connected to the CLK pin of the synchronous DRAM. For details, refer to section 6, Bus Controller (BSC).

Bit	Bit Name	Initial Value	R/W	Description
12	CAST	0	R/W	Column Address Output Cycle Number Select Selects whether the column address output cycle in DRAM access comprises 3 states or 2 states. The setting of this bit applies to all areas designated as DRAM space. 0: Column address output cycle comprises 2 states 1: Column address output cycle comprises 3 states
11	—	0	R/W	Reserved This bit can be read from or written to. However, the write value should always be 0.

6.7.11 Byte Access Control

When synchronous DRAM with a ×16-bit configuration is connected, DQMU and DQML are used for the control signals needed for byte access.

Figures 6.49 and 6.50 show the control timing for DQM, and figure 6.51 shows an example of connection of byte control by DQMU and DQML.

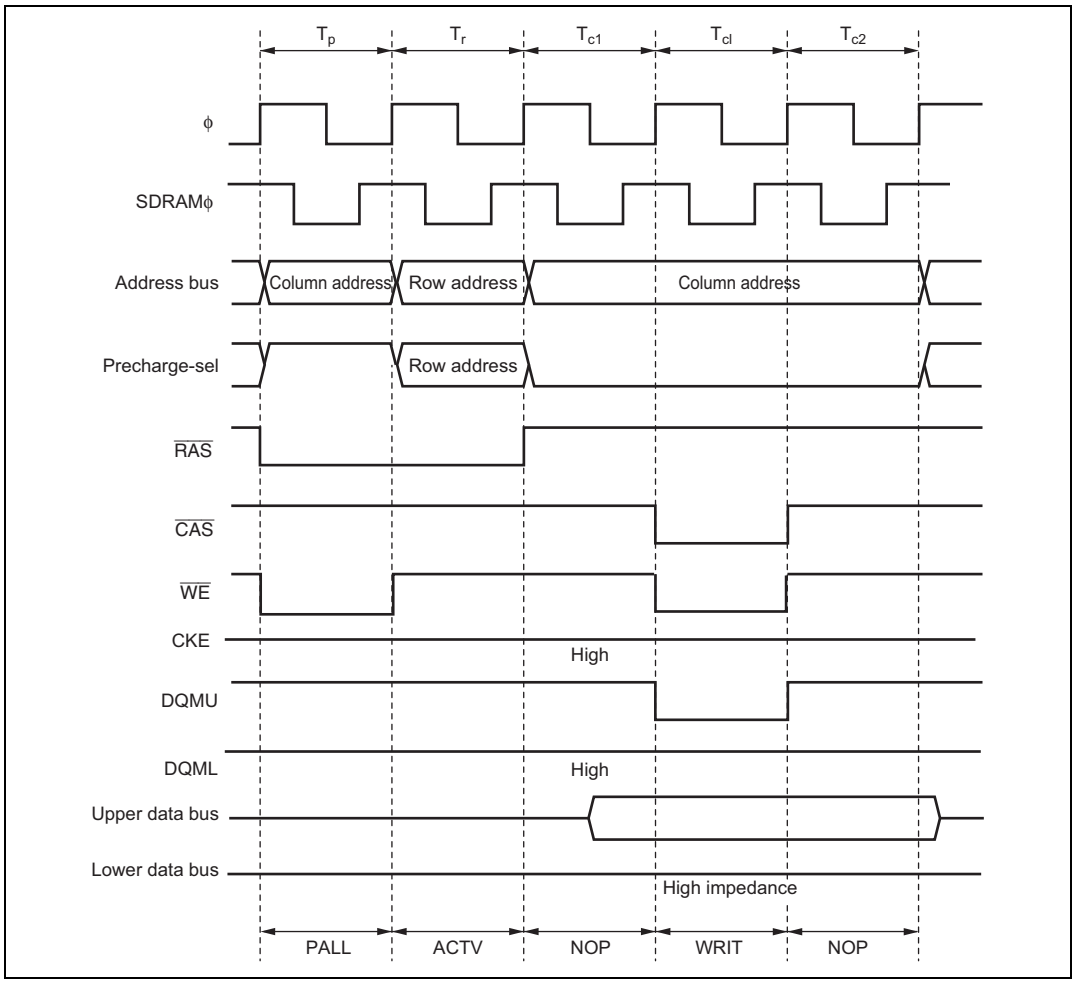

Figure 6.49 DQMU and DQML Control Timing (Upper Byte Write Access: SDWCD = 0, CAS Latency 2)

Block Transfer Mode:

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	—	Reserved These bits are always read as 0 and cannot be modified.
23 to 16		Undefined	R/W	Block Size These bits specify the block size (number of bytes or number of words) for block transfer. Setting H'01 specifies one as the block, while setting H'00 specifies the maximum block size, that is 256. The register value always indicates the specified block size.
15 to 0		Undefined	R/W	16-Bit Transfer Counter These bits specify the number of block transfers. Setting H'0001 specifies one block transfer. Setting H'0000 means no specification for the number of transfers, and the transfer counter function is halted. In this case, there is no transfer end interrupt by the transfer counter. Setting H'FFFF specifies the maximum number of block transfers, that is 65,535. During EXDMA transfer, this counter shows the remaining number of block transfers.

External Request/Cycle Steal Mode/Normal Transfer Mode: In external request mode, an EXDMA transfer cycle is started a minimum of three cycles after a transfer request is accepted. The next transfer request is accepted after the end of a one-transfer-unit EXDMA cycle. For external bus space CPU cycles, at least two bus cycles are generated before the next EXDMA cycle.

If a transfer request is generated for another channel, an EXDMA cycle for the other channel is generated before the next EXDMA cycle.

The $\overline{\text{EDREQ}}$ pin sensing timing is different for low level sensing and falling edge sensing. The same applies to transfer request acceptance and transfer start timing.

Figures 8.35 to 8.38 show operation timing examples for various conditions.

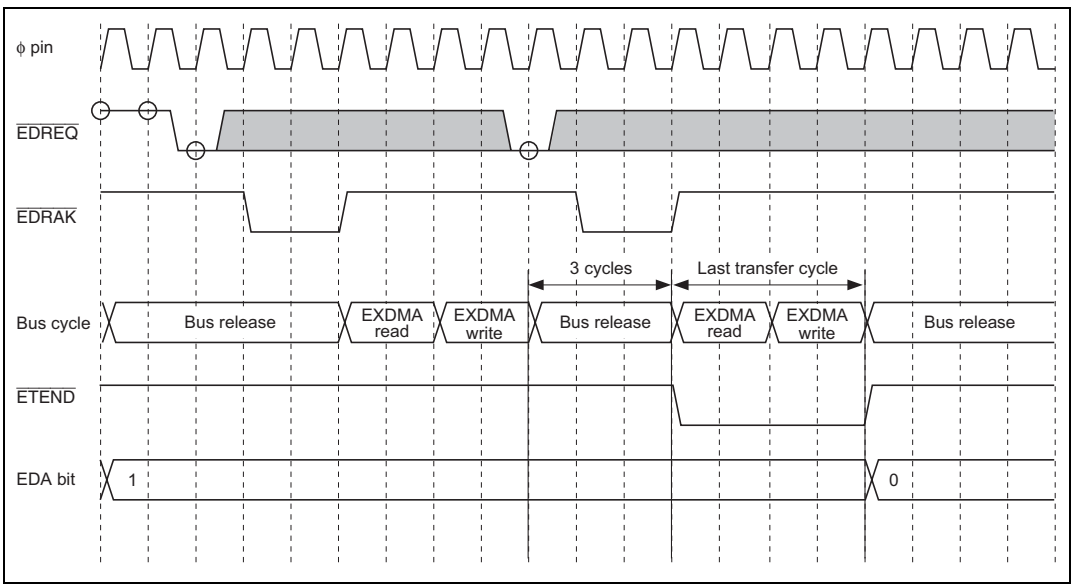

Figure 8.35 External Request/Cycle Steal Mode/Normal Transfer Mode (No Contention/Dual Address Mode/Low Level Sensing)

9.7.2 Chain Transfer

An example of DTC chain transfer is shown in which pulse output is performed using the PPG. Chain transfer can be used to perform pulse output data transfer and PPG output trigger cycle updating. Repeat mode transfer to NDR of the PPG is performed in the first half of the chain transfer, and normal mode transfer to the TPU's TGR in the second half. This is because clearing of the activation source and interrupt generation at the end of the specified number of transfers are restricted to the second half of the chain transfer (transfer when CHNE = 0).

1. Perform settings for transfer to NDR of the PPG. Set MRA to source address incrementing (SM1 = 1, SM0 = 0), fixed destination address (DM1 = DM0 = 0), repeat mode (MD1 = 0, MD0 = 1), and word size (Sz = 1). Set the source side as a repeat area (DTS = 1). Set MRB to chain mode (CHNE = 1, DISEL = 0). Set the data table start address in SAR, the NDRH address in DAR, and the data table size in CRAH and CRAL. CRB can be set to any value.
2. Perform settings for transfer to the TPU's TGR. Set MRA to source address incrementing (SM1 = 1, SM0 = 0), fixed destination address (DM1 = DM0 = 0), normal mode (MD1 = MD0 = 0), and word size (Sz = 1). Set the data table start address in SAR, the TGRA address in DAR, and the data table size in CRA. CRB can be set to any value.
3. Locate the TPU transfer register information consecutively after the NDR transfer register information.
4. Set the start address of the NDR transfer register information to the DTC vector address.
5. Set the bit corresponding to TGIA in DTCER to 1.
6. Set TGRA as an output compare register (output disabled) with TIOR, and enable the TGIA interrupt with TIER.
7. Set the initial output value in PODR, and the next output value in NDR. Set bits in DDR and NDER for which output is to be performed to 1. Using PCR, select the TPU compare match to be used as the output trigger.
8. Set the CST bit in TSTR to 1, and start the TCNT count operation.
9. Each time a TGRA compare match occurs, the next output value is transferred to NDR and the set value of the next output trigger period is transferred to TGRA. The activation source TGFA flag is cleared.
10. When the specified number of transfers are completed (the TPU transfer CRA value is 0), the TGFA flag is held at 1, the DTCE bit is cleared to 0, and a TGIA interrupt request is sent to the CPU. Termination processing should be performed in the interrupt handling routine.

- P61/TMRI1/$\overline{\text{DREQ1}}$/$\overline{\text{IRQ9}}$

  The pin function is switched as shown below according to the combination of bit P61DDR and bit ITS9 in ITSR.

P61DDR	0	1
Pin function	P61 input	P61 output
	TMRI1 input*1	
	$\overline{\text{DREQ1}}$ input	
	$\overline{\text{IRQ9}}$ interrupt input*2	

Notes: 1. When used as the counter reset input pin for the TMR, both the CCLR1 and CCLR0 bits in TCR_1 should be set to 1.
2. $\overline{\text{IRQ9}}$ interrupt input when ITS9 = 0.

- P60/TMRI0/$\overline{\text{DREQ0}}$/$\overline{\text{IRQ8}}$

  The pin function is switched as shown below according to the combination of bit and bit ITS8 in ITSR.

P60DDR	0	1
Pin function	P60 input	P60 output
	TMRI0 input*1	
	$\overline{\text{DREQ0}}$ input	
	$\overline{\text{IRQ8}}$ interrupt input*2	

Notes: 1. When used as the counter reset input pin for the TMR, both the CCLR1 and CCLR0 bits in TCR_0 should be set to 1.
2. $\overline{\text{IRQ8}}$ interrupt input when ITS8 = 0.

10.12.4 Port D Pull-up Control Register (PDPCR)

PDPCR controls on/off states of the input pull-up MOS of port D. PDPCR is valid in mode 7.

Bit	Bit Name	Initial Value	R/W	Description
7	PD7PCR	0	R/W	When PDDDR = 0 (input port), the input pull-up MOS of the input pin is on when the corresponding bit is set to 1.
6	PD6PCR	0	R/W	
5	PD5PCR	0	R/W	
4	PD4PCR	0	R/W	
3	PD3PCR	0	R/W	
2	PD2PCR	0	R/W	
1	PD1PCR	0	R/W	
0	PD0PCR	0	R/W	

10.12.5 Pin Functions

Port D pins also function as the pins for data I/Os. The correspondence between the register specification and the pin functions is shown below.

- PD7/D15, PD6/D14, PD5/D13, PD4/D12, PD3/D11, PD2/D10, PD1/D9, PD0/D8

  The pin function is switched as shown below according to the operating mode, bit EXPE, and bit PDDDR.

Operating mode	1, 2, 4	7		
EXPE	—	0		1
PDnDDR	—	0	1	—
Pin function	Data I/O	PDn input	PDn output	Data I/O

Legend: n = 7 to 0

10.13.2 Port E Data Register (PEDR)

PEDR stores output data for the port E pins.

Bit	Bit Name	Initial Value	R/W	Description
7	PE7DR	0	R/W	Output data for a pin is stored when the pin function is specified to a general purpose I/O.
6	PE6DR	0	R/W	
5	PE5DR	0	R/W	
4	PE4DR	0	R/W	
3	PE3DR	0	R/W	
2	PE2DR	0	R/W	
1	PE1DR	0	R/W	
0	PE0DR	0	R/W	

10.13.3 Port E Register (PORTE)

PORTE shows port E pin states.

PORTE cannot be modified.

Bit	Bit Name	Initial Value	R/W	Description
7	PE7	—*	R	If a port E read is performed while PEDDR bits are set to 1, the PEDR values are read. If a port E read is performed while PEDDR bits are cleared to 0, the pin states are read.
6	PE6	—*	R	
5	PE5	—*	R	
4	PE4	—*	R	
3	PE3	—*	R	
2	PE2	—*	R	
1	PE1	—*	R	
0	PE0	—*	R	

Note: * Determined by the states of pins PE7 to PE0.

Bit	Bit Name	Initial value	R/W	Description
3	TGFD	0	R/(W)*	Input Capture/Output Compare Flag D Status flag that indicates the occurrence of TGRD input capture or compare match in channels 0 and 3. In channels 1, 2, 4, and 5, bit 3 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRD while TGRD is functioning as output compare register • When TCNT value is transferred to TGRD by input capture signal while TGRD is functioning as input capture register [Clearing conditions] • When DTC is activated by TGID interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFD after reading TGFD = 1
2	TGFC	0	R/(W)*	Input Capture/Output Compare Flag C Status flag that indicates the occurrence of TGRC input capture or compare match in channels 0 and 3. In channels 1, 2, 4, and 5, bit 2 is reserved. It is always read as 0 and cannot be modified. [Setting conditions] • When TCNT = TGRC while TGRC is functioning as output compare register • When TCNT value is transferred to TGRC by input capture signal while TGRC is functioning as input capture register [Clearing conditions] • When DTC is activated by TGIC interrupt while DISEL bit of MRB in DTC is 0 • When 0 is written to TGFC after reading TGFC = 1

Table 11.30 PWM Output Registers and Output Pins

		Output Pins	
Channel	**Registers**	**PWM Mode 1**	**PWM Mode 2**
0	TGRA_0	TIOCA0	TIOCA0
	TGRB_0		TIOCB0
	TGRC_0	TIOCC0	TIOCC0
	TGRD_0		TIOCD0
1	TGRA_1	TIOCA1	TIOCA1
	TGRB_1		TIOCB1
2	TGRA_2	TIOCA2	TIOCA2
	TGRB_2		TIOCB2
3	TGRA_3	TIOCA3	TIOCA3
	TGRB_3		TIOCB3
	TGRC_3	TIOCC3	TIOCC3
	TGRD_3		TIOCD3
4	TGRA_4	TIOCA4	TIOCA4
	TGRB_4		TIOCB4
5	TGRA_5	TIOCA5	TIOCA5
	TGRB_5		TIOCB5

Note: In PWM mode 2, PWM output is not possible for the TGR register in which the cycle is set.

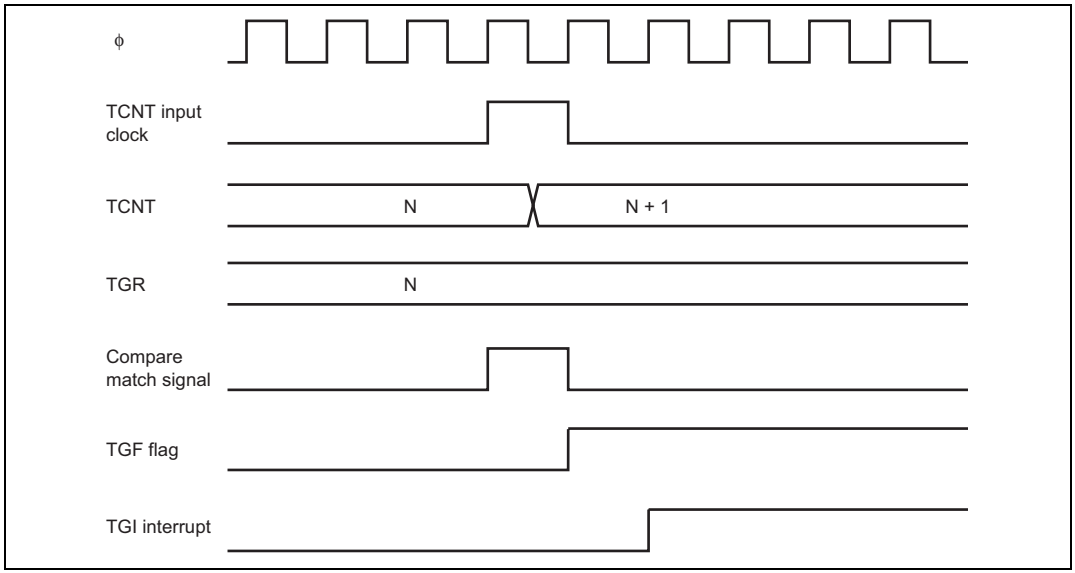

Figure 11.38 TGI Interrupt Timing (Compare Match)

TGF Flag Setting Timing in Case of Input Capture: Figure 11.39 shows the timing for setting of the TGF flag in TSR by input capture occurrence, and the TGI interrupt request signal timing.

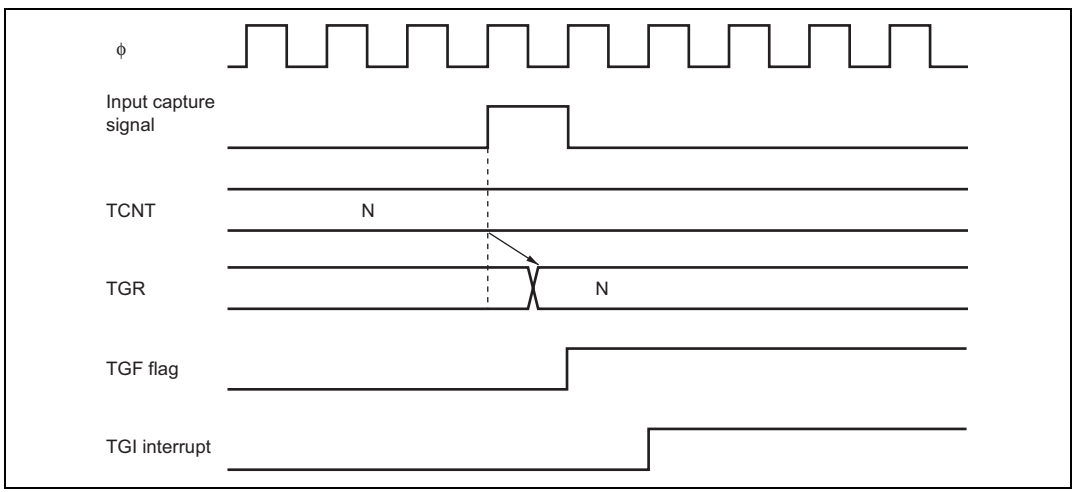

Figure 11.39 TGI Interrupt Timing (Input Capture)

Section 16 I²C Bus Interface 2 (IIC2) (Option)

An I²C bus interface is an option. When using the optional functions, take notice of the following item:

1. For the masked ROM version, W is added to the model name of the product that uses optional functions.
   For example: HD6432375WFQ

This LSI has a two-channel I²C bus interface.

The I²C bus interface conforms to and provides a subset of the NXP Semiconductors I²C bus (inter-IC bus) interface (Rev. 03) standard and fast mode functions. The register configuration that controls the I²C bus differs partly from the NXP Semiconductors configuration, however.

Figure 16.1 shows a block diagram of the I²C bus interface 2.

Figure 16.2 shows an example of I/O pin connections to external circuits.

16.1 Features

- Continuous transmission/reception

  Since the shift register, transmit data register, and receive data register are independent from each other, the continuous transmission/reception can be performed.
- Start and stop conditions generated automatically in master mode
- Selection of acknowledge output levels when receiving
- Automatic loading of acknowledge bit when transmitting
- Bit synchronization/wait function

  In master mode, the state of SCL is monitored per bit, and the timing is synchronized automatically

  If transmission/reception is not yet possible, set the SCL to low until preparations are completed.
- Six interrupt sources

  Transmit-data-empty (including slave-address match), transmit-end, receive-data-full (including slave-address match), arbitration lost, NACK detection, and stop condition detection
- Direct bus drive

  Two pins, SCL and SDA pins function as NMOS open-drain outputs.

16.3.4 I²C Bus Interrupt Enable Register (ICIER)

ICIER is an 8-bit readable/writable register that enables or disables interrupt sources and acknowledge bits, sets acknowledge bits to be transferred, and confirms acknowledge bits to be received.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable When the TDRE bit in ICSR is set to 1, this bit enables or disables the transmit data empty interrupt (TXI). 0: Transmit data empty interrupt request (TXI) is disabled. 1: Transmit data empty interrupt request (TXI) is enabled.
6	TEIE	0	R/W	Transmit End Interrupt Enable This bit enables or disables the transmit end interrupt (TEI) at the rising of the ninth clock while the TDRE bit in ICSR is 1. TEI can be canceled by clearing the TEND bit or the TEIE bit to 0. 0: Transmit end interrupt request (TEI) is disabled. 1: Transmit end interrupt request (TEI) is enabled.
5	RIE	0	R/W	Receive interrupt enable This bit enables or disables the receive data full interrupt request (RXI) when a received data is transferred from ICDRS to ICDRR and the RDRF bit in ICSR is set to 1. RXI can be canceled by clearing the RDRF or RIE bit to 0. 0: Receive data full interrupt request (RXI) is disabled. 1: Receive data full interrupt request (RXI) is enabled.

20.7.2 Erase/Erase-Verify

When erasing flash memory, the erase/erase-verify flowchart shown in figure 20.8 should be followed.

1. Prewriting (setting erase block data to all 0s) is not necessary.
2. Erasing is performed in block units. Make only a single-bit specification in the erase block registers (EBR1 and EBR2). To erase multiple blocks, each block must be erased in turn.
3. The time during which the E bit is set to 1 is the flash memory erase time.
4. The watchdog timer (WDT) is set to prevent overprogramming due to program runaway, etc. Set a value greater than ($y + z + \alpha + \beta$) ms as the WDT overflow period.
5. For a dummy write to a verify address, write 1-byte data H'FF to an address whose lower two bits are B'00. Verify data can be read in longwords from the address to which a dummy write was performed.
6. If the read data is not erased, set erase mode again, and repeat the erase/erase-verify sequence as before. The maximum number of repetitions of the erase/erase-verify sequence (N) must not be exceeded.

20.7.3 Interrupt Handling when Programming/Erasing Flash Memory

All interrupts, including NMI input, are disabled when flash memory is being programmed or erased, and while the boot program is executing in boot mode. There are three reasons for this:

1. Interrupt during programming or erasing might cause a violation of the programming or erasing algorithm, with the result that normal operation could not be assured.
2. If the interrupt exception handling is started when the vector address has not been programmed yet or the flash memory is being programmed or erased, the vector would not be read correctly, possibly resulting in CPU runaway.
3. If an interrupt occurred during boot program execution, it would not be possible to execute the normal boot mode sequence.

Section 21 Flash Memory (0.18-μm F-ZTAT Version)

The flash memory has the following features. Figure 21.1 shows a block diagram of the flash memory.

21.1 Features

- Size

Product Classification		ROM Size	ROM Address
H8S/2378	HD64F2378B	512 kbytes	H'000000 to H'07FFFF (Modes 3 to 5 and 7)
H8S/2378R	HD64F2378R		
H8S/2374	HD64F2374	384 kbytes	H'000000 to H'05FFFF (Modes 3 to 5 and 7)
H8S/2374R	HD64F2374R		
H8S/2372	HD64F2372	256 kbytes	H'000000 to H'03FFFF (Modes 3 to 5 and 7)
H8S/2372R	HD64F2372R		
H8S/2371	HD64F2371		
H8S/2371R	HD64F2371R		
H8S/2370	HD64F2370		
H8S/2370R	HD64F2370R		

- Two flash-memory MATs according to LSI initiation mode
  The on-chip flash memory has two memory spaces in the same address space (hereafter referred to as memory MATs). The mode setting in the initiation determines which memory MAT is initiated first. The MAT can be switched by using the bank-switching method after initiation.
  - The user memory MAT is initiated at a power-on reset in user mode: 256 kbytes/ 384 kbytes/512 kbytes
  - The user boot memory MAT is initiated at a power-on reset in user boot mode: 8 kbytes
- Programming/erasing interface by the download of on-chip program
  This LSI has a dedicated programming/erasing program. After downloading this program to the on-chip RAM, programming/erasing can be performed by setting the argument parameter. The user branch is also supported.

(4) Inquiry and Selection States

The boot program returns information from the flash memory in response to the host's inquiry commands and sets the device code, clock mode, and bit rate in response to the host's selection command.

Inquiry and selection commands are listed below.

Table 21.11 Inquiry and Selection Commands

Command	Command Name	Description
H'20	Supported Device Inquiry	Inquiry regarding device codes
H'10	Device Selection	Selection of device code
H'21	Clock Mode Inquiry	Inquiry regarding numbers of clock modes and values of each mode
H'11	Clock Mode Selection	Indication of the selected clock mode
H'22	Multiplication Ratio Inquiry	Inquiry regarding the number of frequency-multiplied clock types, the number of multiplication ratios, and the values of each multiple
H'23	Operating Clock Frequency Inquiry	Inquiry regarding the maximum and minimum values of the main clock and peripheral clocks
H'24	User Boot MAT Information Inquiry	Inquiry regarding the number of user boot MATs and the start and last addresses of each MAT
H'25	User MAT Information Inquiry	Inquiry regarding the a number of user MATs and the start and last addresses of each MAT
H'26	Block for Erasing Information Inquiry	Inquiry regarding the number of blocks and the start and last addresses of each block
H'27	Programming Unit Inquiry	Inquiry regarding the unit of programming data
H'3F	New Bit Rate Selection	Selection of new bit rate
H'40	Transition to Programming/Erasing State	Erasing of user MAT and user boot MAT, and entry to programming/erasing state
H'4F	Boot Program Status Inquiry	Inquiry into the operated status of the boot program

The selection commands, which are device selection (H'10), clock mode selection (H'11), and new bit rate selection (H'3F), should be sent from the host in that order. These commands will certainly be needed. When two or more selection commands are sent at once, the last command will be valid.

Table 23.2 Crystal Resonator Characteristics

Frequency (MHz)	8	12	16	20	25
R_S max (Ω)	80	60	50	40	40
C_0 max (pF)	7	7	7	7	7

23.2.2 External Clock Input

An external clock signal can be input as shown in the examples in figure 23.4. If the XTAL pin is left open, make sure that parasitic capacitance is no more than 10 pF. When the counter clock is input to the XTAL pin, make sure that the external clock is held high in standby mode.

Table 23.3 shows the input conditions for the external clock. When an external clock is used, the range of its frequencies is from 8 to 25 MHz.

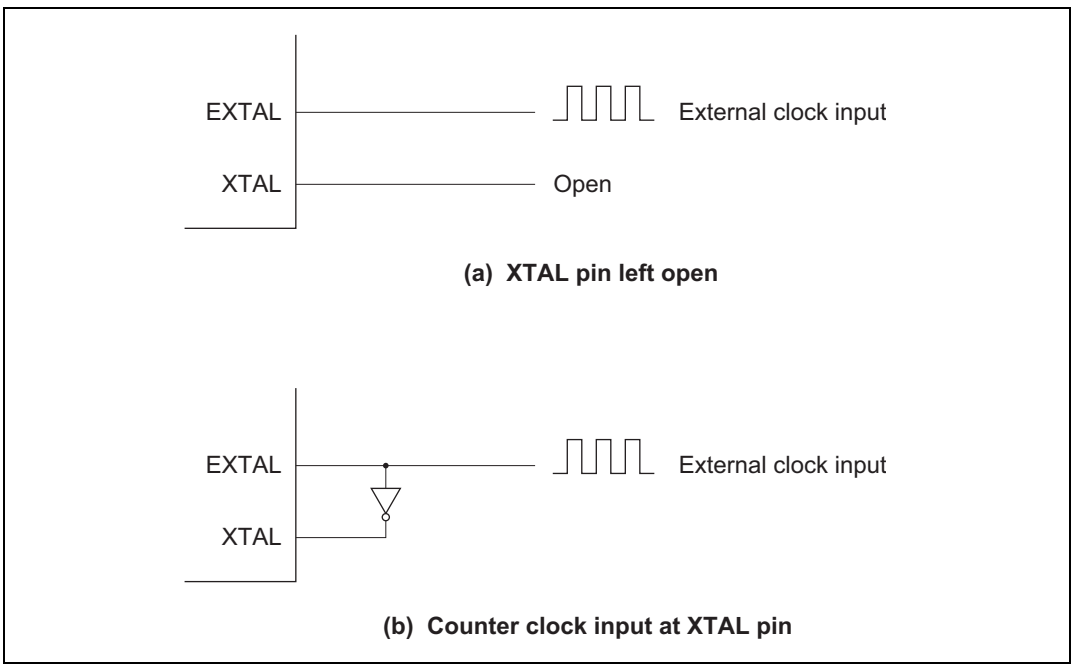

Figure 23.4 External Clock Input (Examples)

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reference power supply current	During A/D and D/A conversion	AI_{CC}	—	3.0 (3.0 V)	6.0	mA	
	Idle		—	0.01	5.0	μA	
RAM standby voltage		V_{RAM}	2.0	—	—	V	

Notes: 1. When the A/D and D/A converters are not used, the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

2. Current consumption values are for $V_{IH}min = V_{CC} - 0.2$ V and $V_{IL}max = 0.2$ V with all output pins unloaded and all input pull-up MOSs in the off state.

3. The values are for $V_{RAM} \leq V_{CC} < 3.0$ V, $V_{IH}min = V_{CC} \times 0.9$, and $V_{IL}max = 0.3$ V.

4. I_{CC} depends on V_{CC} and f as follows:

$I_{CC}max = 1.0\ (mA) + 1.0\ (mA/(MHz \times V)) \times V_{CC} \times f$ (normal operation)

$I_{CC}max = 1.0\ (mA) + 0.85\ (mA/(MHz \times V)) \times V_{CC} \times f$ (sleep mode)

Table 26.4 Permissible Output Currents

Conditions: $V_{CC} = 3.0$ V to 3.6 V, $AV_{CC} = 3.0$ V to 3.6 V, $V_{ref} = 3.0$ V to AV_{CC}, $V_{SS} = AV_{SS} = 0$ V*, $T_a = -20$°C to +75°C (regular specifications), $T_a = -40$°C to +85°C (wide-range specifications)

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	SCL0, 1, SDA0, 1	I_{OL}	—	—	8.0	mA
	Output pins other than the above		—	—	2.0	
Permissible output low current (total)	Total of all output pins	ΣI_{OL}	—	—	80	mA
Permissible output high current (per pin)	All output pins	$-I_{OH}$	—	—	2.0	mA
Permissible output high current (total)	Total of all output pins	$\Sigma -I_{OH}$	—	—	40	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in table 26.4.

Note: * When the A/D and D/A converters are not used, do not leave the AV_{CC}, V_{ref}, and AV_{SS} pins should not be open. Connect the AV_{CC} and V_{ref} pins to V_{CC}, and the AV_{SS} pin to V_{SS}.

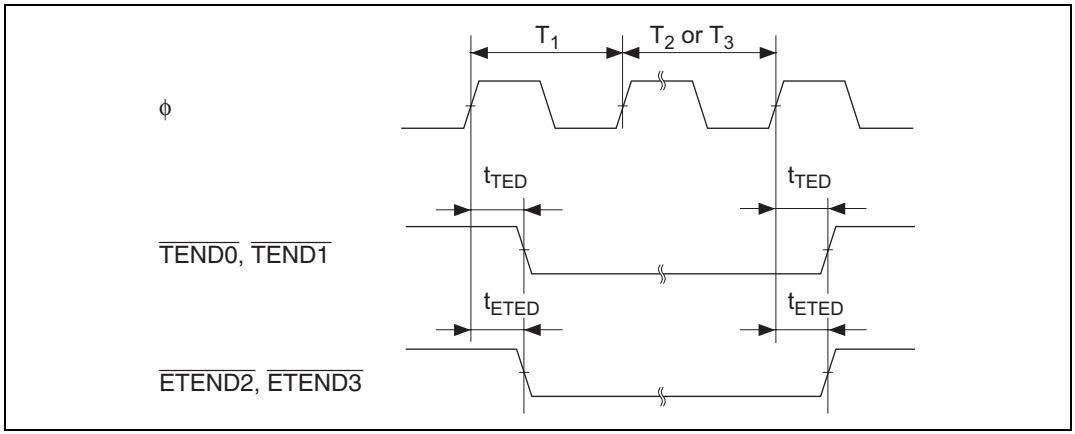

Figure 26.30 DMAC and EXDMAC $\overline{\text{TEND}}$/$\overline{\text{ETEND}}$ Output Timing

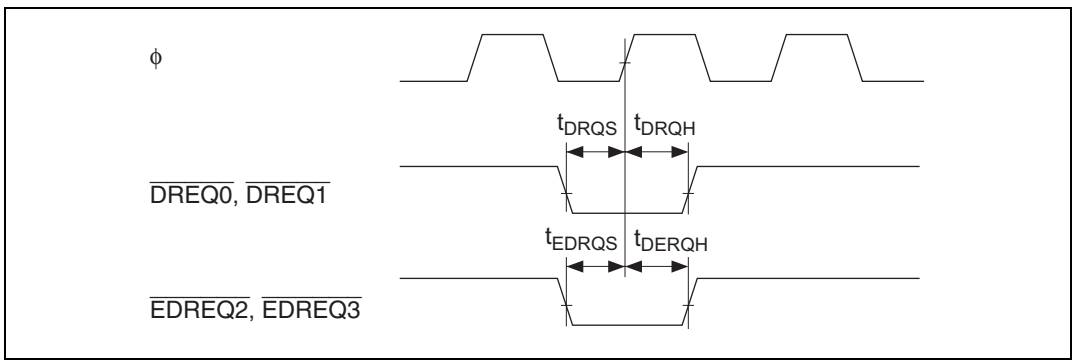

Figure 26.31 DMAC and EXDMAC $\overline{\text{DREQ}}$/$\overline{\text{EDREQ}}$ Input Timing

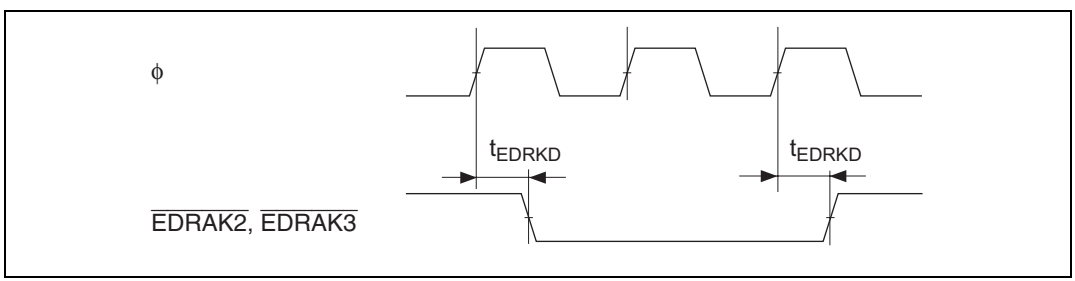

Figure 26.32 EXDMAC $\overline{\text{EDRAK}}$ Output Timing