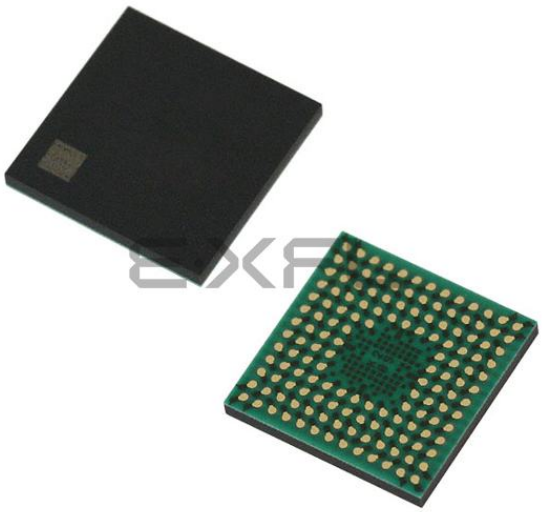

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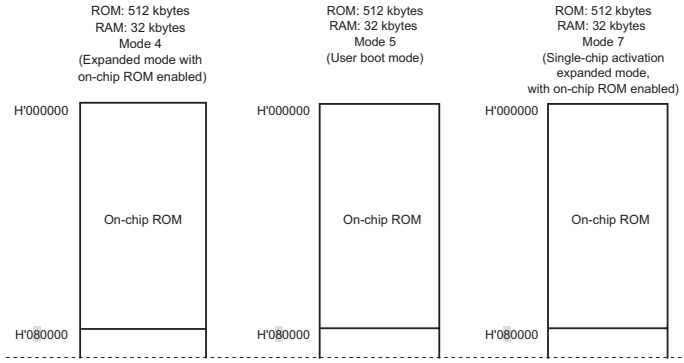
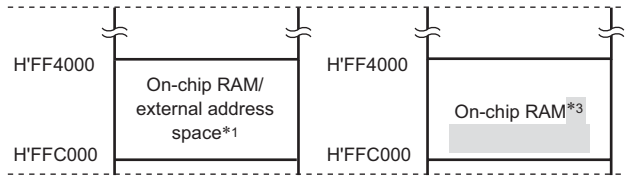
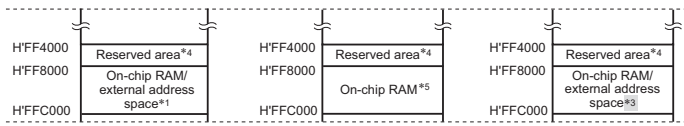
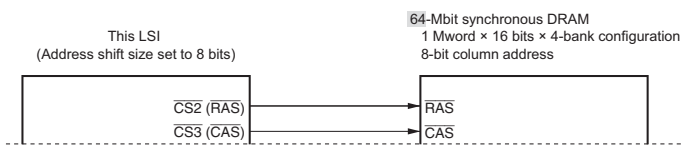
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	H8S/2000
Core Size	16-Bit
Speed	34MHz
Connectivity	I²C, IrDA, SCI, SmartCard
Peripherals	DMA, POR, PWM, WDT
Number of I/O	96
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 3.6V
Data Converters	A/D 16x10b; D/A 6x8b
Oscillator Type	External
Operating Temperature	-20°C ~ 75°C (TA)
Mounting Type	Surface Mount
Package / Case	145-TFLGA
Supplier Device Package	145-TFLGA (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/df2378rvlp34v

Main Revisions for This Edition

Item	Page	Revision (See Manual for Details)
3.4 Memory Map in Each Operating Mode Figure 3.2 Memory Map for H8S/2378 and H8S/2378R (2)	79	Figure amended 
Figure 3.7 Memory Map for H8S/2374 and H8S/2374R (1)	84	Figure amended 
Figure 3.15 Memory Map for H8S/2370 and H8S/2370R (2)	92	Figure amended 
6.7.11 Byte Access Control Figure 6.51 Example of DQMU and DQML Byte Control	230	Figure amended 
6.9.2 Pin States in Idle Cycle Table 6.12 Pin States in Idle Cycle	268	Table amended **Pins** — **Pin State** EDACKn (n = 3, 2) — High
7.3.7 DMA Terminal Control Register (DMATCR)	306	Description amended … The TEND pin is available only for channel B in short address mode.

		Pin No.					
Type	**Symbol**	**H8S/2378 0.18µm F-ZTAT Group, H8S/2378R 0.18µm F-ZTAT Group (LQFP-144)**	**H8S/2378 0.18µm F-ZTAT Group, H8S/2378R 0.18µm F-ZTAT Group (LGA-145)**	**H8S/2377 H8S/2377R**	**H8S/2375 H8S/2373 H8S/2375R H8S/2373R**	**I/O**	**Function**
Clock	XTAL	96	F13	96	96	Input	For connection to a crystal oscillator. See section 23, Clock Pulse Generator, for typical connection diagrams for a crystal resonator and external clock input.
	EXTAL	97	E13	97	97	Input	For connection to a crystal oscillator. The EXTAL pin can also input an external clock. See section 23, Clock Pulse Generator, for typical connection diagrams for a crystal resonator and external clock input.
	ϕ	94	F10	94	94	Output	Supplies the system clock to external devices.
	SDRAMϕ[*1]	36	M1	36	36	Output	When a synchro-nous DRAM is connected, this pin is connected to the CLK pin of the synchronous DRAM. For details, refer to section 6, Bus Controller (BSC).

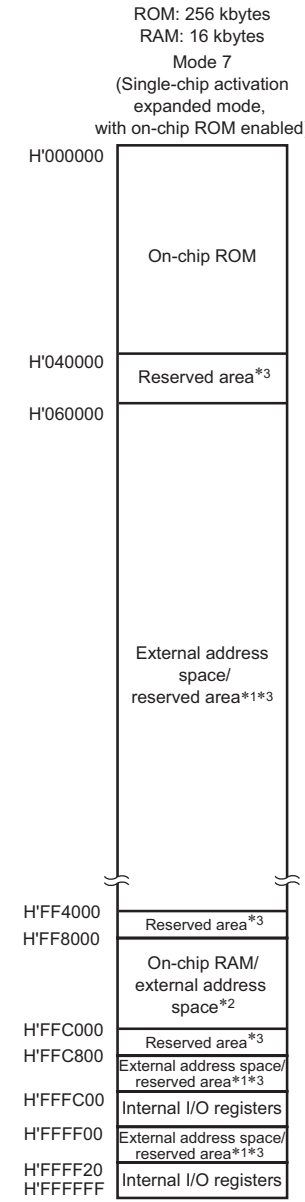
2.6.1 Table of Instructions Classified by Function

Tables 2.3 to 2.10 summarize the instructions in each functional category. The notation used in tables 2.3 to 2.10 is defined below.

Table 2.2 Operation Notation

Symbol	Description
Rd	General register (destination)*
Rs	General register (source)*
Rn	General register*
ERn	General register (32-bit register)
(EAd)	Destination operand
(EAs)	Source operand
EXR	Extended control register
CCR	Condition-code register
N	N (negative) flag in CCR
Z	Z (zero) flag in CCR
V	V (overflow) flag in CCR
C	C (carry) flag in CCR
PC	Program counter
SP	Stack pointer
#IMM	Immediate data
disp	Displacement
+	Addition
–	Subtraction
×	Multiplication
÷	Division
∧	Logical AND
∨	Logical OR
⊕	Logical exclusive OR
→	Move
~	NOT (logical complement)
:8/:16/:24/:32	8-, 16-, 24-, or 32-bit length

Note: * General registers include 8-bit registers (R0H to R7H, R0L to R7L), 16-bit registers (R0 to R7, E0 to E7), and 32-bit registers (ER0 to ER7).



Notes: 1. When EXPE = 1, external address space; when EXPE = 0, reserved area.
2. When EXPE = 1, external address space with RAME = 0, on-chip RAM with RAME = 1.
When EXPE = 0, on-chip RAM.
3. A reserved area should not be accessed.

Figure 3.6 Memory Map for H8S/2375 and H8S/2375R (2)

4.7 Stack Status after Exception Handling

Figure 4.3 shows the stack after completion of trap instruction exception handling and interrupt exception handling.

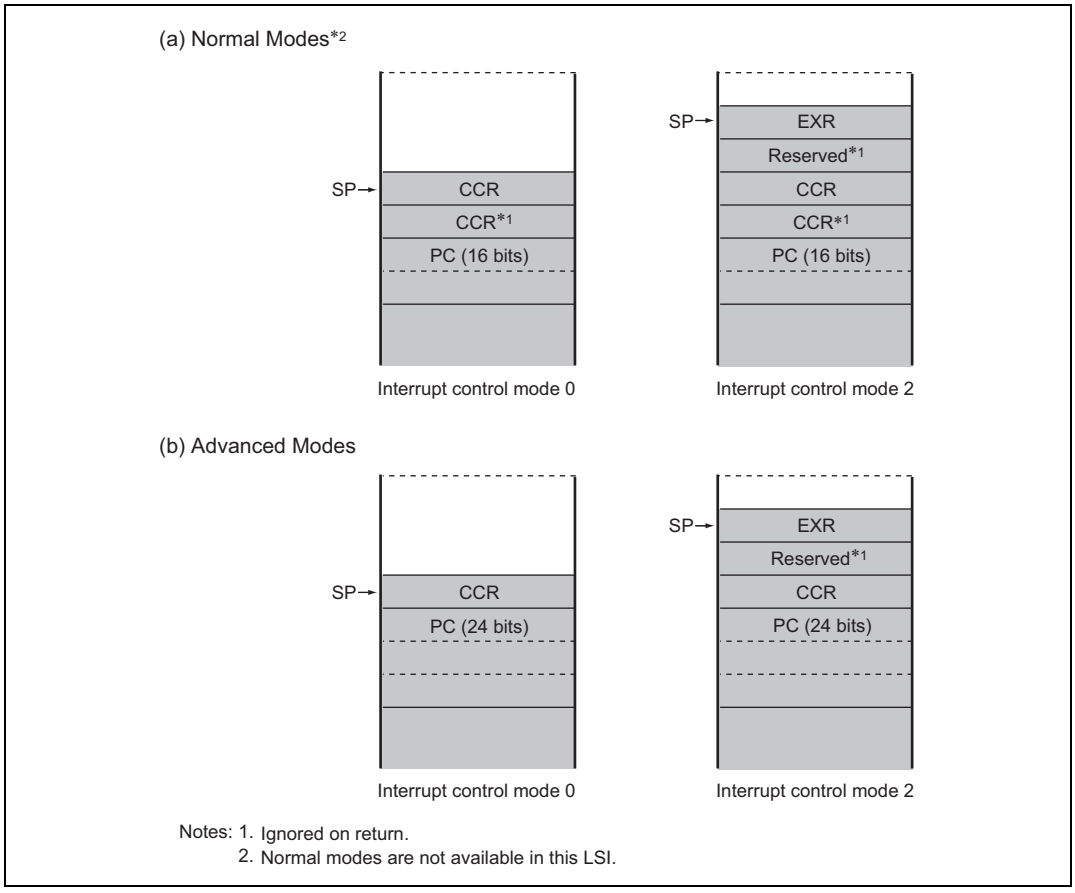


Figure 4.3 Stack Status after Exception Handling

6.7 Synchronous DRAM Interface

In the H8S/2378R Group, external address space areas 2 to 5 can be designated as continuous synchronous DRAM space, and synchronous DRAM interfacing performed. The synchronous DRAM interface allows synchronous DRAM to be directly connected to this LSI. A synchronous DRAM space of up to 8 Mbytes can be set by means of bits RMTS2 to RMTS0 in DRAMCR. Synchronous DRAM of CAS latency 1 to 4 can be connected.

Note: The synchronous DRAM interface is not supported by the H8S/2378 Group.

6.7.1 Setting Continuous Synchronous DRAM Space

Areas 2 to 5 are designated as continuous synchronous DRAM space by setting bits RMTS2 to RMTS0 in DRAMCR. The relation between the settings of bits RMTS2 to RMTS0 and synchronous DRAM space is shown in table 6.7. Possible synchronous DRAM interface settings are and continuous area (areas 2 to 5).

Table 6.7 Relation between Settings of Bits RMTS2 to RMTS0 and Synchronous DRAM Space

RMTS2	RMTS1	RMTS0	Area 5	Area 4	Area 3	Area 2
0	0	1	Normal space	Normal space	Normal space	DRAM space
	1	0	Normal space	Normal space	DRAM space	DRAM space
		1	DRAM space	DRAM space	DRAM space	DRAM space
1	0	0	Continuous synchronous DRAM space			
		1	Mode settings of synchronous DRAM			
	1	0	Reserved (setting prohibited)			
		1	Continuous DRAM space			

With continuous synchronous DRAM space, $\overline{CS2}$, $\overline{CS3}$, $\overline{CS4}$ pins are used as $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$ signal. The ($\overline{OE}$) pin of the synchronous DRAM is used as the CKE signal, and the $\overline{CS5}$ pin is used as synchronous DRAM clock (SDRAMϕ). The bus specifications for continuous synchronous DRAM space conform to the settings for area 2. The pin wait and program wait for the continuous synchronous DRAM are invalid.

Commands for the synchronous DRAM can be specified by combining $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, and address-precharge-setting command (Precharge-sel) output on the upper column addresses.

6.9.2 Pin States in Idle Cycle

Table 6.12 shows the pin states in an idle cycle.

Table 6.12 Pin States in Idle Cycle

Pins	Pin State
A23 to A0	Contents of following bus cycle
D15 to D0	High impedance
$\overline{CSn}$ (n = 7 to 0)	High*1 *2
$\overline{UCAS}$, $\overline{LCAS}$	High*2
$\overline{AS}$	High
$\overline{RD}$	High
($\overline{OE}$)	High
$\overline{HWR}$, $\overline{LWR}$	High
$\overline{DACKn}$ (n = 1, 0)	High
$\overline{EDACKn}$ (n = 3, 2)	High

Notes: 1. Remains low in DRAM space RAS down mode.
2. Remains low in a DRAM space refresh cycle.

6.10 Write Data Buffer Function

This LSI has a write data buffer function for the external data bus. Using the write data buffer function enables external writes and DMA single address mode transfers to be executed in parallel with internal accesses. The write data buffer function is made available by setting the WDBE bit to 1 in BCR.

Figure 6.83 shows an example of the timing when the write data buffer function is used. When this function is used, if an external address space write or DMA single address mode transfer continues for two states or longer, and there is an internal access next, an external write only is executed in the first state, but from the next state onward an internal access (on-chip memory or internal I/O register read/write) is executed in parallel with the external address space write rather than waiting until it ends.

Bit	Bit Name	Initial Value	R/W	Description
3	DTIE1B	0	R/W	Data Transfer End Interrupt Enable 1B
2	DTIE1A	0	R/W	Data Transfer End Interrupt Enable 1A
1	DTIE0B	0	R/W	Data Transfer End Interrupt Enable 0B
0	DTIE0A	0	R/W	Data Transfer End Interrupt Enable 0A These bits enable or disable an interrupt to the CPU or DTC when transfer ends. If the DTIE bit is set to 1 when DTE = 0, the DMAC regards this as indicating the end of a transfer, and issues a transfer end interrupt request to the CPU or DTC. A transfer end interrupt can be canceled either by clearing the DTIE bit to 0 in the interrupt handling routine, or by performing processing to continue transfer by setting the transfer counter and address register again, and then setting the DTE bit to 1.

Full Address Mode:

- DMABCRH

Bit	Bit Name	Initial Value	R/W	Description
15	FAE1	0	R/W	Full Address Enable 1 Specifies whether channel 1 is to be used in short address mode or full address mode. In full address mode, channels 1A and 1B are used together as channel 1. 0: Short address mode 1: Full address mode
14	FAE0	0	R/W	Full Address Enable 0 Specifies whether channel 0 is to be used in short address mode or full address mode. In full address mode, channels 0A and 0B are used together as channel 0. 0: Short address mode 1: Full address mode

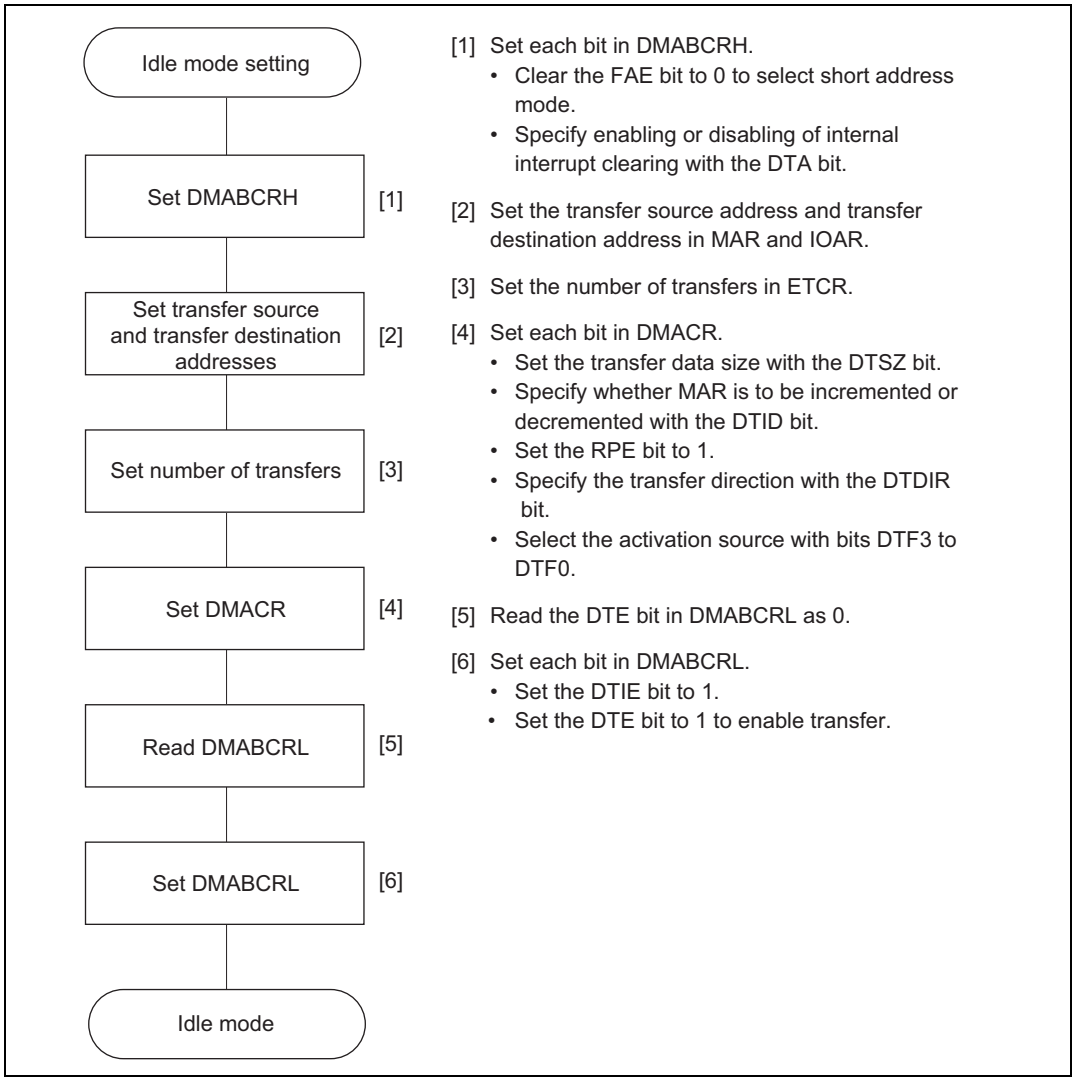


Figure 7.6 Example of Idle Mode Setting Procedure

7.5.4 Repeat Mode

Repeat mode can be specified by setting the RPE bit in DMACR to 1, and clearing the DTIE bit in DMABCRL to 0. In repeat mode, MAR is updated after each byte or word transfer in response to a single transfer request, and this is executed the number of times specified in ETCRL. On completion of the specified number of transfers, MAR and ETCRL are automatically restored to their original settings and operation continues. One address is specified by MAR, and the other by

Caution is required when setting the repeat area overflow interrupt of the repeat area function in block transfer mode. See section 8.4.6, Repeat Area Function, for details.

Block transfer is aborted if an NMI interrupt is generated. See section 8.4.12, Ending DMA Transfer, for details.

Figure 8.8 shows an example of DMA transfer timing in block transfer mode.

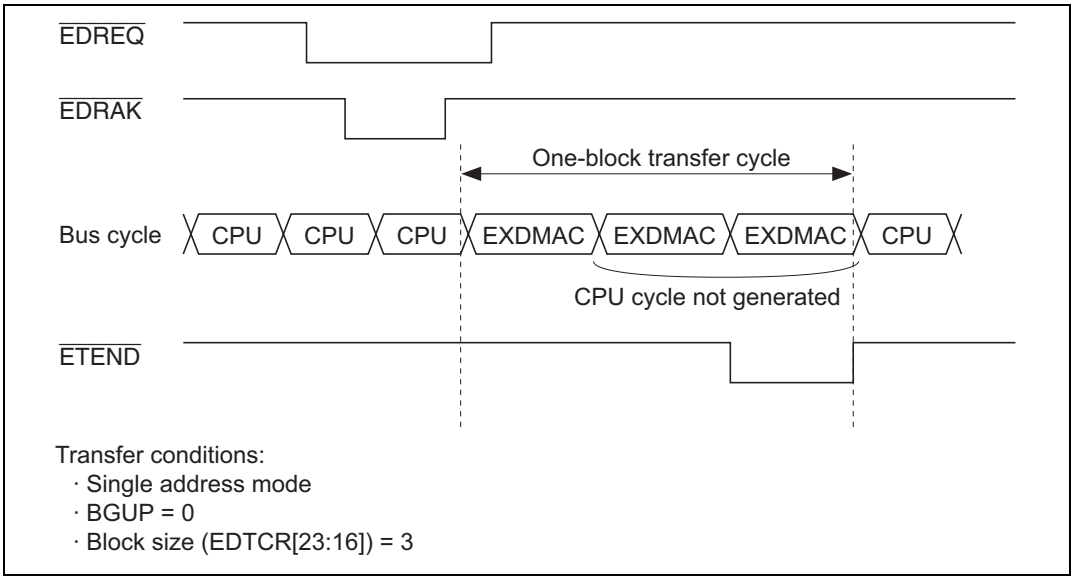
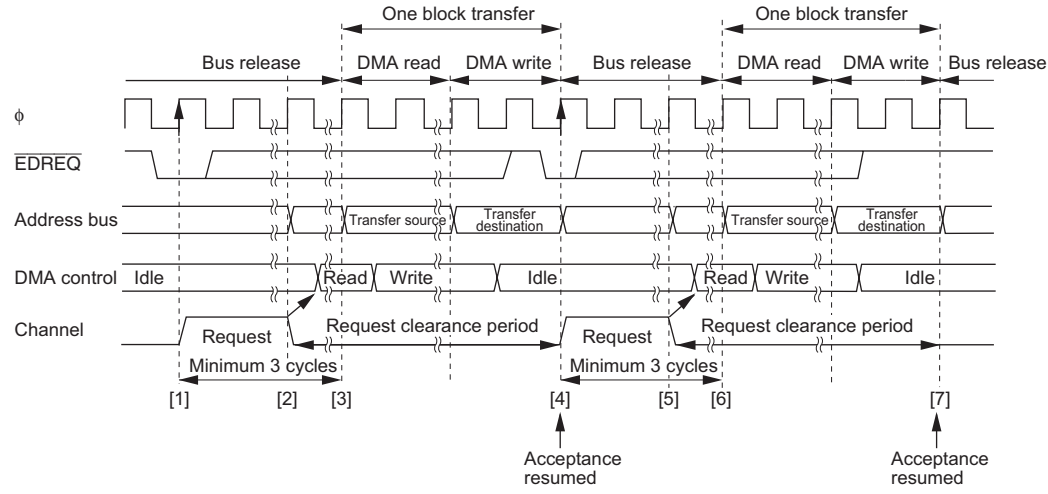


Figure 8.8 Example of Timing in Block Transfer Mode

8.4.6 Repeat Area Function

The EXDMAC has a function for designating a repeat area for source addresses and/or destination addresses. When a repeat area is designated, the address register values repeat within the range specified as the repeat area. Normally, when a ring buffer is involved in a transfer, an operation is required to restore the address register value to the buffer start address each time the address register value is the last address in the buffer (i.e. when ring buffer address overflow occurs), but if the repeat area function is used, the operation that restores the address register value to the buffer start address is performed automatically within the EXDMAC.

The repeat area function can be set independently for the source address register and the destination address register.



[1] Acceptance after transfer enabling; $\overline{\text{EDREQ}}$ pin low level is sampled at rise of ϕ, and request is held.
[2], [5] Request is cleared at end of next bus cycle, and activation is started in EXDMAC.
[3], [6] DMA cycle start; $\overline{\text{EDREQ}}$ pin high level sampling is started at rise of ϕ.
[4], [7] When $\overline{\text{EDREQ}}$ pin high level has been sampled, acceptance is resumed after completion of dead cycle. (As in [1], $\overline{\text{EDREQ}}$ pin low level is sampled at rise of ϕ, and request is held.)

Figure 8.19 Example of Block Transfer Mode Transfer Activated by $\overline{\text{EDREQ}}$ Pin Falling Edge

$\overline{\text{EDREQ}}$ pin sampling is performed in each cycle starting at the next rise of ϕ after the end of the EDMDR write cycle for setting the transfer-enabled state.

When a low level is sampled at the $\overline{\text{EDREQ}}$ pin while acceptance via the $\overline{\text{EDREQ}}$ pin is possible, the request is held within the EXDMAC. Then when activation is initiated within the EXDMAC, the request is cleared, and $\overline{\text{EDREQ}}$ pin high level sampling for edge sensing is started. If $\overline{\text{EDREQ}}$ pin high level sampling is completed by the end of the DMA write cycle, acceptance resumes after the end of the write cycle, and $\overline{\text{EDREQ}}$ pin low level sampling is performed again; this sequence of operations is repeated until the end of the transfer.

9.5.5 Interrupt Sources

An interrupt request is issued to the CPU when the DTC finishes the specified number of data transfers, or a data transfer for which the DISEL bit was set to 1. In the case of interrupt activation, the interrupt set as the activation source is generated. These interrupts to the CPU are subject to CPU mask level and interrupt controller priority level control.

In the case of activation by software, a software activated data transfer end interrupt (SWDTEND) is generated.

When the DISEL bit is 1 and one data transfer has ended, or the specified number of transfers has ended, after data transfer ends, the SWDTE bit is held at 1 and an SWDTEND interrupt is generated. The interrupt handling routine should clear the SWDTE bit to 0.

When the DTC is activated by software, an SWDTEND interrupt is not generated during a data transfer wait or during data transfer even if the SWDTE bit is set to 1.

9.5.6 Operation Timing

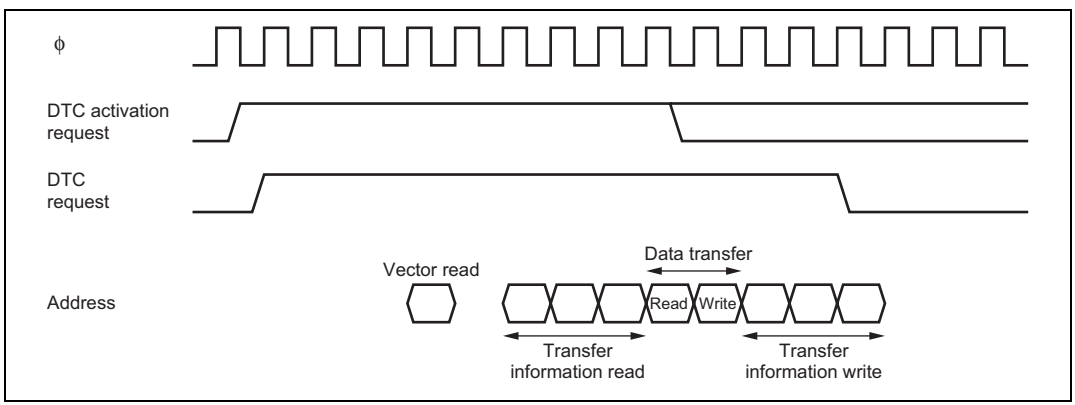


Figure 9.10 DTC Operation Timing (Example in Normal Mode or Repeat Mode)

Mode 7 (EXPE = 0)

EDRAKE	—			
TPU channel 2 settings	(1) in table below	(2) in table below		
P16DDR	—	0	1	1
NDER14	—	—	0	1
Pin function	TIOCA2 output	P16 input	P16 output	PO14 output
		TIOCA2 input*1		

TPU channel 2 settings	(2)	(1)	(2)	(1)	(1)	(2)
MD3 to MD0	B'0000, B'01××		B'001×	B'0010	B'0011	
IOA3 to IOA0	B'0000 B'0100 B'1×××	B'0001 to B'0011 B'0101 to B'0111	B'××00	Other than B'××00		
CCLR1, CCLR0	—	—	—	—	Other than B'10	B'10
Output function	—	Output compare output	—	PWM*2 mode 1 output	PWM mode 2 output	—

Legend:

×: Don't care

Notes: 1. TIOCA2 input when MD3 to MD0 = B'0000, B'000, and B'01×× and IOB3 = 1.

2. TIOCB2 output disabled.

3. Not supported by the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.

Buffer Operation Timing: Figures 11.36 and 11.37 show the timings in buffer operation.

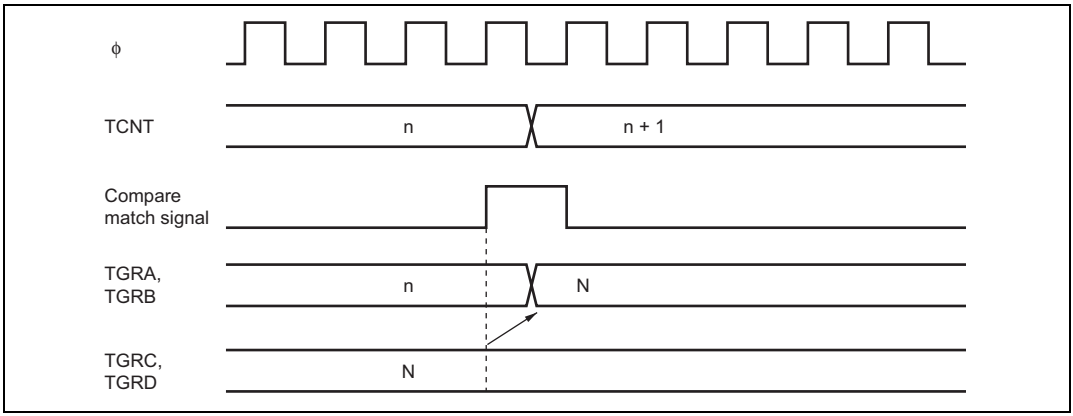


Figure 11.36 Buffer Operation Timing (Compare Match)

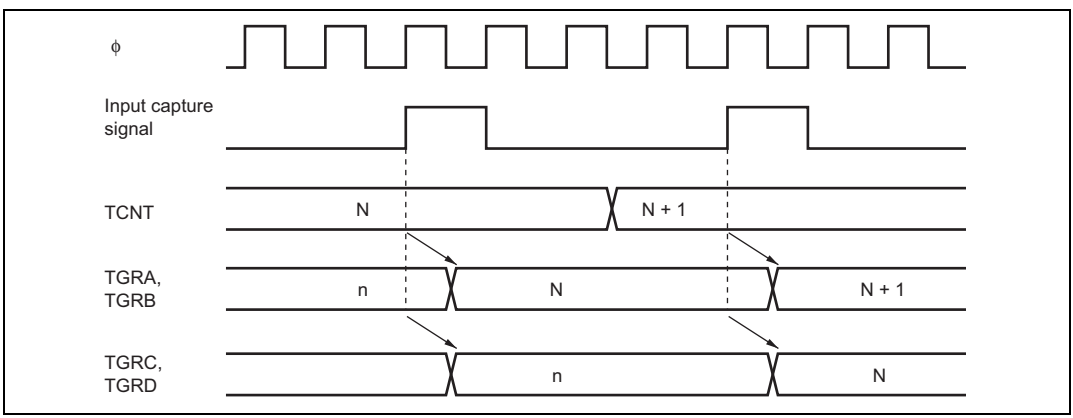


Figure 11.37 Buffer Operation Timing (Input Capture)

11.9.2 Interrupt Signal Timing

TGF Flag Setting Timing in Case of Compare Match: Figure 11.38 shows the timing for setting of the TGF flag in TSR by compare match occurrence, and the TGI interrupt request signal timing.

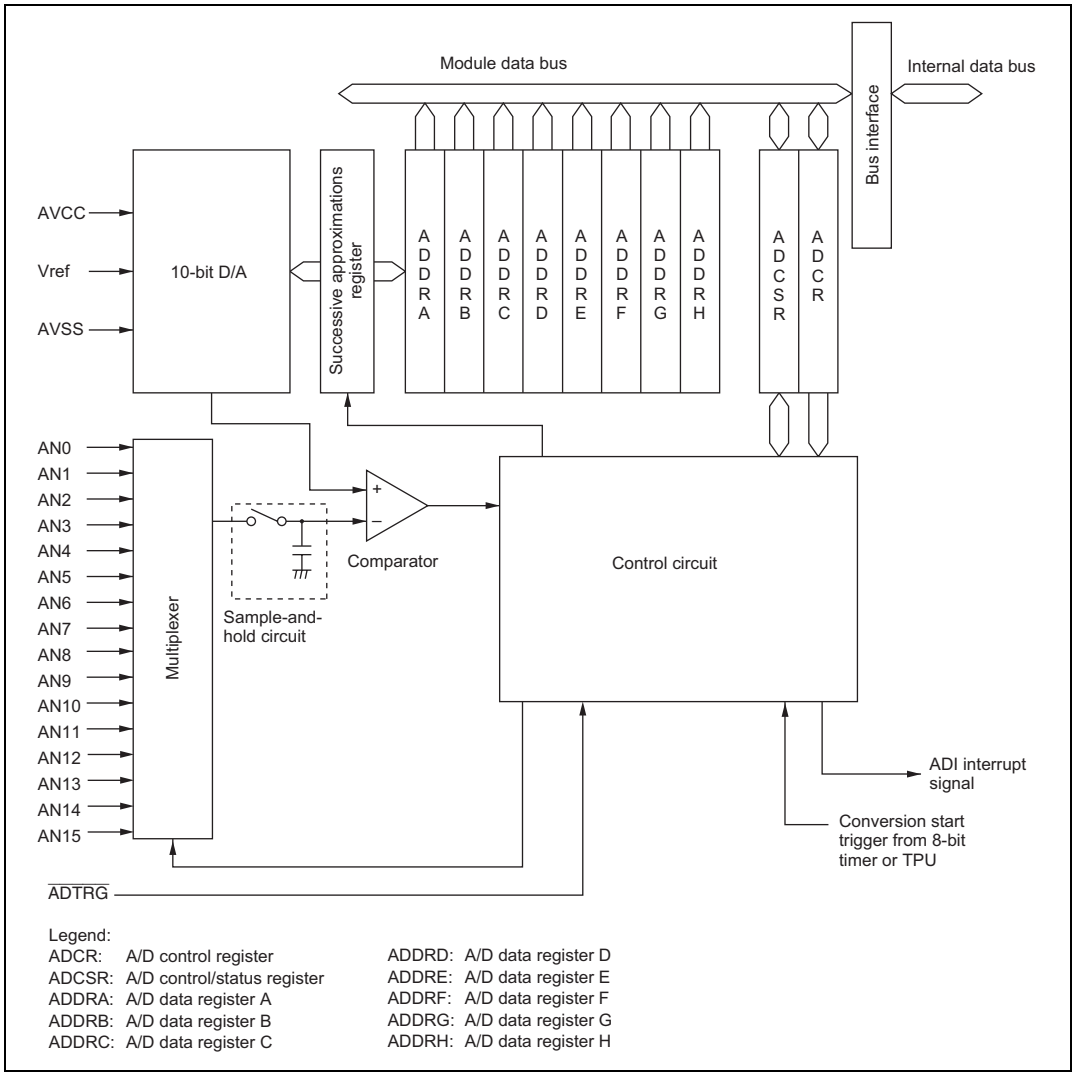


Figure 17.1 Block Diagram of A/D Converter

21.3.2 Programming/Erasing Interface Parameter

The programming/erasing interface parameter specifies the operating frequency, storage place for program data, programming destination address, and erase block and exchanges the processing result for the downloaded on-chip program. This parameter uses the general registers of the CPU (ER0 and ER1) or the on-chip RAM area. The initial value is undefined at a power-on reset or in hardware standby mode.

When download, initialization, or on-chip program is executed, registers of the CPU except for ER0 and ER1 are stored. The return value of the processing result is written in ER0, ER1. Since the stack area is used for storing the registers except for ER0, ER1, the stack area must be saved at the processing start. (A maximum size of a stack area to be used is 128 bytes.)

The programming/erasing interface parameter is used in the following four items.

1. Download control
2. Initialization before programming or erasing
3. Programming
4. Erasing

These items use different parameters. The correspondence table is shown in table 21.4. The meaning of the bits in FPFR varies in each processing program: initialization, programming, or erasure. For details, see descriptions of FPFR for each process.

Item	Storable/Executable Area			Selected MAT	
	On-chip RAM	User MAT	External Space (Expanded Mode)	User MAT	Embedded Program Storage Area
Execution of Programming	○	×	×	○	
Determination of Program Result	○	×	○	○	
Operation for Program Error	○	×	○	○	
Operation for FKEY Clear	○	×	○	○	

Note: * Transferring the data to the on-chip RAM enables this area to be used.

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access States
Port C data register	PCDR	8	H'FF6B	PORT	8	2
Port D data register	PDDR	8	H'FF6C	PORT	8	2
Port E data register	PEDR	8	H'FF6D	PORT	8	2
Port F data register	PFDR	8	H'FF6E	PORT	8	2
Port G data register	PGDR	8	H'FF6F	PORT	8	2
Port H register	PORTH	8	H'FF70	PORT	8	2
Port H data register	PHDR	8	H'FF72	PORT	8	2
Port H data direction register	PHDDR	8	H'FF74	PORT	8	2
Serial mode register_0	SMR_0	8	H'FF78	SCI_0	8	2
Bit rate register_0	BRR_0	8	H'FF79	SCI_0	8	2
Serial control register_0	SCR_0	8	H'FF7A	SCI_0	8	2
Transmit data register_0	TDR_0	8	H'FF7B	SCI_0	8	2
Serial status register_0	SSR_0	8	H'FF7C	SCI_0	8	2
Receive data register_0	RDR_0	8	H'FF7D	SCI_0	8	2
Smart card mode register_0	SCMR_0	8	H'FF7E	SCI_0	8	2
Serial mode register_1	SMR_1	8	H'FF80	SCI_1	8	2
Bit rate register_1	BRR_1	8	H'FF81	SCI_1	8	2
Serial control register_1	SCR_1	8	H'FF82	SCI_1	8	2
Transmit data register_1	TDR_1	8	H'FF83	SCI_1	8	2
Serial status register_1	SSR_1	8	H'FF84	SCI_1	8	2
Receive data register_1	RDR_1	8	H'FF85	SCI_1	8	2
Smart card mode register_1	SCMR_1	8	H'FF86	SCI_1	8	2
Serial mode register_2	SMR_2	8	H'FF88	SCI_2	8	2
Bit rate register_2	BRR_2	8	H'FF89	SCI_2	8	2
Serial control register_2	SCR_2	8	H'FF8A	SCI_2	8	2
Transmit data register_2	TDR_2	8	H'FF8B	SCI_2	8	2
Serial status register_2	SSR_2	8	H'FF8C	SCI_2	8	2
Receive data register_2	RDR_2	8	H'FF8D	SCI_2	8	2
Smart card mode register_2	SCMR_2	8	H'FF8E	SCI_2	8	2
A/D data register A	ADDRA	16	H'FF90	A/D	16	2

Register Name	Abbreviation	Number of Bits	Address	Module	Data Width	Access States
Timer general register B_0	TGRB_0	16	H'FFDA	TPU_0	16	2
Timer general register C_0	TGRC_0	16	H'FFDC	TPU_0	16	2
Timer general register D_0	TGRD_0	16	H'FFDE	TPU_0	16	2
Timer control register_1	TCR_1	8	H'FFE0	TPU_1	16	2
Timer mode register_1	TMDR_1	8	H'FFE1	TPU_1	16	2
Timer I/O control register_1	TIOR_1	8	H'FFE2	TPU_1	16	2
Timer interrupt enable register_1	TIER_1	8	H'FFE4	TPU_1	16	2
Timer status register_1	TSR_1	8	H'FFE5	TPU_1	16	2
Timer counter_1	TCNT_1	16	H'FFE6	TPU_1	16	2
Timer general register A_1	TGRA_1	16	H'FFE8	TPU_1	16	2
Timer general register B_1	TGRB_1	16	H'FFEA	TPU_1	16	2
Timer control register_2	TCR_2	8	H'FFF0	TPU_2	16	2
Timer mode register_2	TMDR_2	8	H'FFF1	TPU_2	16	2
Timer I/O control register_2	TIOR_2	8	H'FFF2	TPU_2	16	2
Timer interrupt enable register_2	TIER_2	8	H'FFF4	TPU_2	16	2
Timer status rgister_2	TSR_2	8	H'FFF5	TPU_2	16	2
Timer counter_2	TCNT_2	16	H'FFF6	TPU_2	16	2
Timer general register A_2	TGRA_2	16	H'FFF8	TPU_2	16	2
Timer general register B_2	TGRB_2	16	H'FFFA	TPU_2	16	2

Notes: 1. If the pulse output group 2 and pulse output group 3 output triggers are the same according to the PCR setting, the NDRH address will be H'FF4C, and if different, the address of NDRH for group 2 will be H'FF4E, and that for group 3 will be H'FF4C. Similarly, if the pulse output group 0 and pulse output group 1 output triggers are the same according to the PCR setting, the NDRL address will be H'FF4D, and if different, the address of NDRL for group 0 will be H'FF4F, and that for group 1 will be H'FF4D.

2. For writing, refer to section 14.6.1, Notes on Register Access.
3. Not supported by the H8S/2375, H8S/2375R, H8S/2373, and H8S/2373R.
4. Supported only by the H8S/2378 0.18μm F-ZTAT Group and H8S/2378R 0.18μm F-ZTAT Group.
5. These addresses should not be accessed in the H8S/2375, H8S/2375R, H8S/2373, H8S/2373R, H8S/2376, H8S/2377, and H8S/2377R.

Notes: 1. Follow the program/erase algorithms when making the time settings.
2. Programming time per 128 bytes. (Indicates the total time during which the P bit is set in flash memory control register 1 (FLMCR1). Does not include the program-verify time.)
3. Time to erase one block. (Indicates the time during which the E bit is set in FLMCR1. Does not include the erase-verify time.)
4. Maximum programming time

$$t_P(\max) = \sum_{i=1}^{N} \text{wait time after P bit setting (z)}$$

5. The maximum number of programming (N) should be set as shown below according to the actual set value of (z) so as not to exceed the maximum programming time (t_P(max)).

   The wait time after P bit setting (z) should be changed as follows according to the number of programming (n).

   Number of programming (n)

   $1 \leq n \leq 6$ $z = 30$ µs

   $7 \leq n \leq 1000$ $z = 200$ µs

   (Additional programming)

   Number of programming (n)

   $1 \leq n \leq 6$ $z = 10$ µs
6. For the maximum erase time (t_E(max)), the following relationship applies between the wait time after E bit setting (z) and the maximum number of erases (N):

   $t_E(\max) =$ Wait time after E bit setting (z) $\times$ maximum number of erases (N)
7. The minimum number of rewrites after which all characteristics are guaranteed. (Characteristics are guaranteed over a range of one rewrite to the minimum number of rewrites.)
8. Reference value for 25°C. (Rewrites usually function up to this standard value.)
9. The data retention characteristics within the specification range, including the minimum number of rewrites.

26.1.7 Usage Note

The F-ZTAT and masked ROM versions both satisfy the electrical characteristics shown in this manual, but actual electrical characteristic values, operating margins, noise margins, and other properties may vary due to differences in manufacturing process, on-chip ROM, layout patterns, and so on.

When system evaluation testing is carried out using the F-ZTAT version, the same evaluation testing should also be conducted for the masked ROM version when changing over to that version.