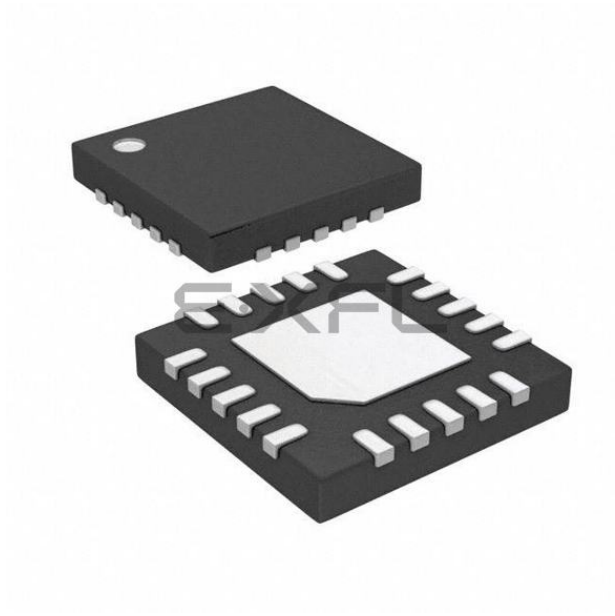

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## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | PIC |
| Core Size | 8-Bit |
| Speed | 20MHz |
| Connectivity | - |
| Peripherals | Brown-out Detect/Reset, POR, WDT |
| Number of I/O | 17 |
| Program Memory Size | 1.5KB (1K x 12) |
| Program Memory Type | FLASH |
| EEPROM Size | 64 x 8 |
| RAM Size | 68 x 8 |
| Voltage - Supply (Vcc/Vdd) | 2V ~ 5.5V |
| Data Converters | A/D 8x8b |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 125°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 20-UFQFN Exposed Pad |
| Supplier Device Package | 20-UQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/pic16f527-e-gz |

## 1.0 GENERAL DESCRIPTION

The PIC16F527 device from Microchip Technology is a low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontroller. It employs a RISC architecture with only 36 single-word/single-cycle instructions. All instructions are single cycle except for program branches, which take two cycles. The PIC16F527 device delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy to remember instruction set reduces development time significantly.

The PIC16F527 product is equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are several oscillator configurations to choose from, including INTRC Internal Oscillator mode and the power-saving LP (Low-Power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC16F527 device is available in the cost-effective Flash programmable version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC16F527 product is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full-featured programmer. All the tools are supported on IBM® PC and compatible machines.

### 1.1 Applications

The PIC16F527 device fits in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16F527 device very versatile, even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

**TABLE 1-1: FEATURES AND MEMORY OF PIC16F527**

| | | PIC16F527 |
|---|---|---|
| Clock | Maximum Frequency of Operation (MHz) | 20 |
| Memory | Flash Program Memory | 1024 |
| | SRAM Data Memory (bytes) | 68 |
| | Flash Data Memory (bytes) | 64 |
| Peripherals | Timer Module(s) | TMR0 |
| | Wake-up from Sleep on Pin Change | Yes |
| Features | I/O Pins | 17 |
| | Input Pins | 1 |
| | Internal Pull-ups | Yes |
| | In-Circuit Serial Programming™ | Yes |
| | Number of Instructions | 36 |
| | Packages | 20-pin PDIP, SOIC, SSOP, QFN, UQFN |
| | Interrupts | Yes |

## 2.0 PIC16F527 DEVICE VARIETIES

A variety of packaging options are available. Depending on application and production requirements, the proper device option can be selected using the information in this section. When placing orders, please use the PIC16F527 Product Identification System at the back of this data sheet to specify the correct part number.

### 2.1 Quick Turn Programming (QTP) Devices

Microchip offers a QTP programming service for factory production orders. This service is made available for users who choose not to program medium-to-high quantity units and whose code patterns have stabilized. The devices are identical to the Flash devices but with all Flash locations and fuse options already programmed by the factory. Certain code and prototype verification procedures do apply before production shipments are available. Please contact your local Microchip Technology sales office for more details.

### 2.2 Serialized Quick Turn Programming$^{SM}$ (SQTP$^{SM}$) Devices

Microchip offers a unique programming service, where a few user-defined locations in each device are programmed with different serial numbers. The serial numbers may be random, pseudo-random or sequential.

Serial programming allows each device to have a unique number, which can serve as an entry code, password or ID number.

**TABLE 3-2: PIC16F527 PINOUT DESCRIPTION (CONTINUED)**

| Name | Function | Input Type | Output Type | Description |
|---|---|---|---|---|
| RC2/AN6/OP2 | RC2 | ST | CMOS | Bidirectional I/O port. |
| | AN6 | AN | — | ADC channel input. |
| | OP2 | — | AN | Op amp 2 output. |
| RC3/AN7/OP1 | RC3 | ST | CMOS | Bidirectional I/O port. |
| | AN7 | AN | — | ADC channel input. |
| | OP1 | — | AN | Op amp 1 output. |
| RC4/C2OUT | RC4 | ST | CMOS | Bidirectional I/O port. |
| | C2OUT | — | CMOS | Comparator 2 output. |
| RC5 | RC5 | ST | CMOS | Bidirectional I/O port. |
| RC6/OP1- | RC6 | ST | CMOS | Bidirectional I/O port. |
| | OP1- | AN | — | Op amp 1 inverting input. |
| RC7/OP1+ | RC7 | ST | CMOS | Bidirectional I/O port. |
| | OP1+ | AN | — | Op amp 1 non-inverting input. |
| $V_{DD}$ | $V_{DD}$ | — | P | Positive supply for logic and I/O pins. |
| $V_{SS}$ | $V_{SS}$ | — | P | Ground reference for logic and I/O pins. |

**Legend:** I = Input, O = Output, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage, AN = Analog Voltage

**TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)**

| Address | Name | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Value on POR/BOR | Value on all other Resets |
|---|---|---|---|---|---|---|---|---|---|---|---|
| **Bank 2** | | | | | | | | | | | |
| N/A | W(2) | Working Register (W) | | | | | | | | xxxx xxxx | xxxx xxxx |
| N/A | TRIS | I/O Control Registers (TRISA, TRISB, TRISC) | | | | | | | | 1111 1111 | 1111 1111 |
| N/A | OPTION | Contains control bits to configure Timer0 and Timer0/WDT prescaler | | | | | | | | 1111 1111 | 1111 1111 |
| N/A | BSR(2) | — | — | — | — | — | — | BSR1 | BSR0 | ---- -000 | ---- -0uu |
| 40h | INDF | Uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 41h | TMR0 | Timer0 module Register | | | | | | | | xxxx xxxx | uuuu uuuu |
| 42h | PCL(1) | Low-order eight bits of PC | | | | | | | | 1111 1111 | 1111 1111 |
| 43h | STATUS(2) | Reserved | Reserved | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | -001 1xxx | -00q qqqq |
| 44h | FSR(2) | — | Indirect data memory address pointer | | | | | | | 0xxx xxxx | 0uuu uuuu |
| 45h | OSCCAL | CAL6 | CAL5 | CAL4 | CAL3 | CAL2 | CAL1 | CAL0 | — | 1111 111- | uuuu uuu- |
| 46h | PORTA | — | — | RA5 | RA4 | RA3 | RA2 | RA1 | RA0 | --xx xxxx | --uu uuuu |
| 47h | PORTB | RB7 | RB6 | RB5 | RB4 | — | — | — | — | xxxx ---- | uuuu ---- |
| 48h | PORTC | RC7 | RC6 | RC5 | RC4 | RC3 | RC2 | RC1 | RC0 | xxxx xxxx | uuuu uuuu |
| 49h | ADCON0 | ADCS1 | ADCS0 | CHS3 | CHS2 | CHS1 | CHS0 | GO/$\overline{DONE}$ | ADON | 1111 1100 | 1111 1100 |
| 4Ah | ADRES | ADC Conversion Result | | | | | | | | xxxx xxxx | uuuu uuuu |
| 4Bh | INTCON0 | ADIF | CWIF | T0IF | RAIF | — | — | — | GIE | 0000 ---0 | 0000 ---0 |
| **Bank 3** | | | | | | | | | | | |
| N/A | W(2) | Working Register (W) | | | | | | | | xxxx xxxx | xxxx xxxx |
| N/A | TRIS | I/O Control Registers (TRISA, TRISB, TRISC) | | | | | | | | 1111 1111 | 1111 1111 |
| N/A | OPTION | Contains control bits to configure Timer0 and Timer0/WDT prescaler | | | | | | | | 1111 1111 | 1111 1111 |
| N/A | BSR(2) | — | — | — | — | — | — | BSR1 | BSR0 | ---- -000 | ---- -0uu |
| 60h | INDF | Uses contents of FSR to address data memory (not a physical register) | | | | | | | | xxxx xxxx | uuuu uuuu |
| 61h | IW(3) | Interrupt Working Register. (Addressed also as W register when within ISR) | | | | | | | | xxxx xxxx | xxxx xxxx |
| 62h | PCL(1) | Low-order eight bits of PC | | | | | | | | 1111 1111 | 1111 1111 |
| 63h | STATUS(2) | Reserved | Reserved | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | -001 1xxx | -00q qqqq |
| 64h | FSR(2) | — | Indirect data memory address pointer | | | | | | | 0xxx xxxx | 0uuu uuuu |
| 65h | INTCON1 | ADIE | CWIE | T0IE | RAIE | — | — | — | WUR | 0000 ---0 | 0000 ---0 |
| 66h | ISTATUS(3) | Reserved | Reserved | PA0 | $\overline{TO}$ | $\overline{PD}$ | Z | DC | C | -xxx xxxx | -00q qqqq |
| 67h | IFSR(3) | — | Indirect data memory address pointer | | | | | | | 0xxx xxxx | 0uuu uuuu |
| 68h | IBSR(3) | — | — | — | — | — | — | BSR1 | BSR0 | ---- -0xx | ---- -0uu |
| 69h | OPACON | — | — | — | — | — | — | OPA2ON | OPA1ON | ---- --00 | ---- --00 |
| 6Bh | INTCON0 | ADIF | CWIF | T0IF | RAIF | — | — | — | GIE | 0000 ---0 | 0000 ---0 |

**Legend:** x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable), q = value depends on condition.
Shaded cells = unimplemented or unused

**Note 1:** The upper byte of the Program Counter is not directly accessible. See **Section 4.6 "Program Counter"** for an explanation of how to access these bits.

**2:** Registers are implemented as two physical registers. When executing from within an ISR, a secondary register is used at the same logical location. Both registers are persistent. See **Section 8.11 "Interrupts"**.

**3:** These registers show the contents of the registers in the other context: ISR or main line code. See **Section 8.11 "Interrupts"**.

## 5.0 SELF-WRITABLE FLASH DATA MEMORY CONTROL

Flash Data memory consists of 64 bytes of self-writable memory and supports a self-write capability that can write a single byte of memory at one time. Data to be written to the self-writable data memory is first written into a write latch before writing the data to Flash memory.

Although each Flash data memory location is 12 bits wide, access is limited to the lower eight bits. The upper four bits will automatically default to '1' in any self-write procedure. The lower eight bits are fully readable and writable during normal operation and throughout the full $V_{DD}$ range.

The self-writable Flash data memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers, EECON, EEDATA and EEADR.

### 5.1 Reading Flash Data Memory

To read a Flash data memory location the user must:

- Write the EEADR register
- Set the RD bit of the EECON register

The value written to the EEADR register determines which Flash data memory location is read. Setting the RD bit of the EECON register initiates the read. Data from the Flash data memory read is available in the EEDATA register immediately. The EEDATA register will hold this value until another read is initiated or it is modified by a write operation. Program execution is suspended while the read cycle is in progress. Execution will continue with the instruction following the one that sets the WR bit. See Example 5-1 for sample code.

**EXAMPLE 5-1: READING FROM FLASH DATA MEMORY**

```
MOVLB     0x01          ; Switch to Bank 1
MOVF      DATA_EE_ADDR,W;
MOVWF     EEADR         ; Data Memory
                        ; Address to read
BSF       EECON, RD     ; EE Read
MOVF      EEDATA, W     ; W = EEDATA
```

**Note:** Only a BSF command will work to enable the Flash data memory read documented in Example 5-1. No other sequence of commands will work, no exceptions.

**Note 1:** To prevent accidental corruption of the Flash data memory, an unlock sequence is required to initiate a write or erase cycle. This sequence requires that the bit set instructions used to configure the EECON register happen exactly as shown in Example 5-2 and Example 5-3, depending on the operation requested.

**2:** In order to prevent any disruptions of self-writes or row erases performed on the self-writable Flash data memory, interrupts should be disabled prior to executing those routines.

#### 5.1.1 ERASING FLASH DATA MEMORY

A row must be manually erased before writing new data. The following sequence must be performed for a single row erase.

1. Load EEADR with an address in the row to be erased.
2. Set the FREE bit to enable the erase.
3. Set the WREN bit to enable write access to the array.
4. Disable interrupts.
5. Set the WR bit to initiate the erase cycle.

If the WREN bit is not set in the instruction cycle after the FREE bit is set, the FREE bit will be cleared in hardware.

If the WR bit is not set in the instruction cycle after the WREN bit is set, the WREN bit will be cleared in hardware.

Sample code that follows this procedure is included in Example 5-2.

Program execution is suspended while the erase cycle is in progress. Execution will continue with the instruction following the one that sets the WR bit.

**EXAMPLE 5-2: ERASING A FLASH DATA MEMORY ROW**

```
MOVLB     0x01          ; Switch to Bank 1
MOVLW     EE_ADR_ERASE  ; LOAD ADDRESS OF ROW TO
                        ; ERASE
MOVWF     EEADR         ;
BSF       EECON,FREE    ; SELECT ERASE
BSF       EECON,WREN    ; ENABLE WRITES
BSF       EECON,WR      ; INITITATE ERASE
```

## 6.7 I/O Programming Considerations

### 6.7.1 BIDIRECTIONAL I/O PORTS

Some instructions operate internally as read followed by write operations. The BCF and BSF instructions, for example, read the entire port into the CPU, execute the bit operation and rewrite the result. Caution must be used when these instructions are applied to a port where one or more pins are used as input/outputs. For example, a BSF operation on bit 5 of PORTB will cause all eight bits of PORTB to be read into the CPU, bit 5 to be set and the PORTB value to be written to the output latches. If another bit of PORTB is used as a bidirectional I/O pin (say bit 0) and it is defined as an input at this time, the input signal present on the pin itself would be read into the CPU and rewritten to the data latch of this particular pin, overwriting the previous content. As long as the pin stays in the Input mode, no problem occurs. However, if bit 0 is switched into Output mode later on, the content of the data latch may now be unknown.

Example 6-1 shows the effect of two sequential Read-Modify-Write instructions (e.g., BCF, BSF, etc.) on an I/O port.

A pin actively outputting a high or a low should not be driven from external devices at the same time in order to change the level on this pin ("wired OR", "wired AND"). The resulting high output currents may damage the chip.

**EXAMPLE 6-1: READ-MODIFY-WRITE INSTRUCTIONS ON AN I/O PORT(e.g. PIC16F527)**

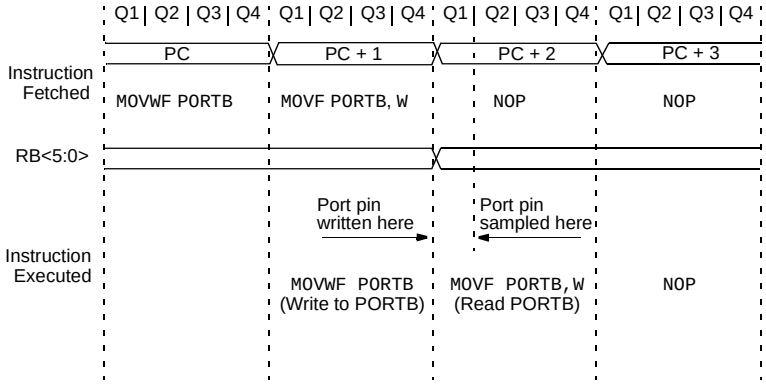
```
;Initial PORTB Settings
;PORTB<5:3> Inputs
;PORTB<2:0> Outputs
;
;   PORTB latch PORTB pins
;   ----------------------
  BCF       PORTB, 5    ;--01 -ppp--11 pppp
  BCF       PORTB, 4    ;--10 -ppp--11 pppp
  MOVLW     007h        ;
  TRIS      PORTB       ;--10 -ppp--11 pppp
;
```

**Note 1:** The user may have expected the pin values to be '--00 pppp'. The 2nd BCF caused RB5 to be latched as the pin value (High).

### 6.7.2 SUCCESSIVE OPERATIONS ON I/O PORTS

The actual write to an I/O port happens at the end of an instruction cycle, whereas for reading, the data must be valid at the beginning of the instruction cycle (Figure 6-2). Therefore, care must be exercised if a write followed by a read operation is carried out on the same I/O port. The sequence of instructions should allow the pin voltage to stabilize (load dependent) before the next instruction causes that file to be read into the CPU. Otherwise, the previous state of that pin may be read into the CPU rather than the new state. When in doubt, it is better to separate these instructions with a NOP or another instruction not accessing this I/O port.

**FIGURE 6-2: SUCCESSIVE I/O OPERATION**




This example shows a write to PORTB followed by a read from PORTB.

Data setup time = (0.25 $T_{CY}$ – $T_{PD}$)

where: $T_{CY}$ = instruction cycle.

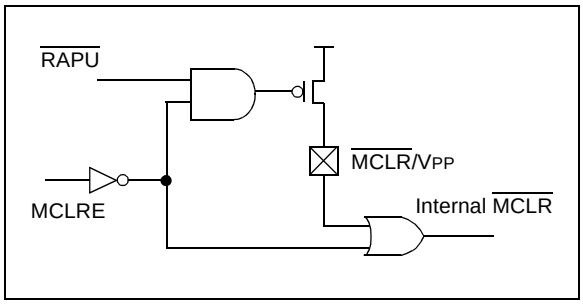
$T_{PD}$ = propagation delay

Therefore, at higher clock frequencies, a write followed by a read may be problematic.

### 8.4.1 MCLR ENABLE

This Configuration bit, when set to a '1', enables the external MCLR Reset function. When cleared to '0', the MCLR function is tied to the internal VDD and the pin is assigned to be an input-only pin function. See Figure 8-6.

**FIGURE 8-6: MCLR SELECT**




## 8.5 Power-on Reset (POR)

The PIC16F527 device incorporates an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the internal POR, program the MCLR/VPP pin as MCLR and tie through a resistor to VDD, or program the pin as an input pin. An internal weak pull-up resistor is implemented using a transistor (refer to Table 15-8 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See **Section 15.0 "Electrical Characteristics"** for details.

When the device starts normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 8-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 8.6 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects MCLR to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

A power-up example where MCLR is held low is shown in Figure 8-8. VDD is allowed to rise and stabilize before bringing MCLR high. The chip will actually come out of Reset TDRT msec after MCLR goes high.

In Figure 8-9, the on-chip Power-on Reset feature is being used (MCLR and VDD are tied together or the pin is programmed to be an input pin). The VDD is stable before the start-up timer times out and there is no problem in getting a proper Reset. However, Figure 8-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that MCLR is high and when MCLR and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (see Figure 8-9).

| **Note:** | When the device starts normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met. |
|---|---|

For additional information, refer to Application Notes *AN522, Power-Up Considerations* (DS00522) and *AN607, Power-up Trouble Shooting* (DS00607).

**TABLE 8-7: INTERRUPT PRIORITIES**

| | In Sleep | GIE | WUR |
|---|---|---|---|
| Vector or Wake-up and Vector | X | 1 | 0 |
| Wake-up Reset | 1 | X | 1 |
| Wake-up Inline | 1 | 0 | 0 |
| Watchdog Wake-up Inline | 1 | X | 0 |
| Watchdog Wake-up Reset | 1 | X | 1 |

**REGISTER 9-2: ADRES: A/D CONVERSION RESULTS REGISTER**

| R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X | R/W-X |
|---|---|---|---|---|---|---|---|
| ADRES7 | ADRES6 | ADRES5 | ADRES4 | ADRES3 | ADRES2 | ADRES1 | ADRES0 |
| bit 7 | | | | | | | bit 0 |

| **Legend:** | | | |
|---|---|---|---|
| R = Readable bit | W = Writable bit | U = Unimplemented bit, read as '0' | |
| -n = Value at POR | '1' = Bit is set | '0' = Bit is cleared | x = Bit is unknown |

bit 7-0 **ADRES<7:0>**: ADC Result Register bits

**EXAMPLE 9-1: PERFORMING AN ANALOG-TO-DIGITAL CONVERSION**

```
;Sample code operates out of BANK0
       MOVLW 0xF1     ;configure A/D
       MOVWF ADCON0
       BSF ADCON0, 1  ;start conversion
loop0  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W  ;read result
       MOVWF result0  ;save result

       BSF ADCON0, 2  ;setup for read of
                      ;channel 1
       BSF ADCON0, 1  ;start conversion
loop1  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W  ;read result
       MOVWF result1  ;save result

       BSF ADCON0, 3  ;setup for read of
       BCF ADCON0, 2  ;channel 2
       BSF ADCON0, 1  ;start conversion
loop2  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W  ;read result
       MOVWF result2  ;save result
```

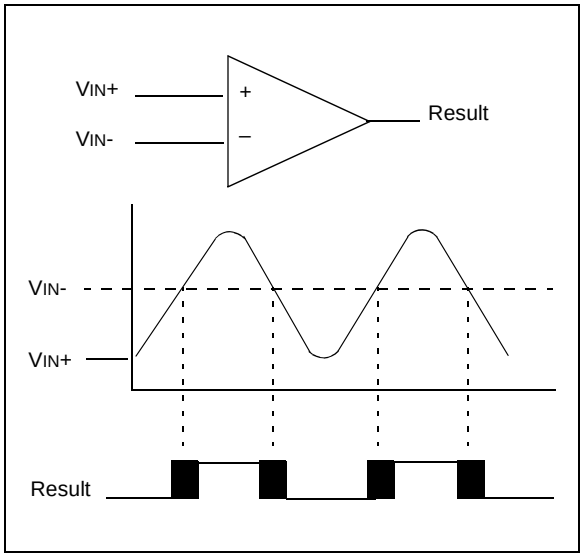
**EXAMPLE 9-2: CHANNEL SELECTION CHANGE DURING CONVERSION**

```
       MOVLW 0xF1     ;configure A/D
       MOVWF ADCON0
       BSF ADCON0, 1  ;start conversion
       BSF ADCON0, 2  ;setup for read of
                      ;channel 1
loop0  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W  ;read result
       MOVWF result0  ;save result

       BSF ADCON0, 1  ;start conversion
       BSF ADCON0, 3  ;setup for read of
       BCF ADCON0, 2  ;channel 2
loop1  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W  ;read result
       MOVWF result1  ;save result

       BSF ADCON0, 1  ;start conversion
loop2  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W  ;read result
       MOVWF result2  ;save result
       CLRF ADCON0    ;optional: returns
       ;pins to Digital mode and turns off
       ;the ADC module
```

## 10.1 Comparator Operation

A single comparator is shown in Figure 10-2 along with the relationship between the analog input levels and the digital output. When the analog input at VIN+ is less than the analog input VIN-, the output of the comparator is a digital low level. The shaded area of the output of the comparator in Figure 10-2 represent the uncertainty due to input offsets and response time. See Table 15-2 for Common Mode Voltage.

**FIGURE 10-2: SINGLE COMPARATOR**




## 10.2 Comparator Reference

An internal reference signal may be used depending on the comparator operating mode. The analog signal that is present at VIN- is compared to the signal at VIN+, and the digital output of the comparator is adjusted accordingly (see Figure 10-2). Please see **Section 11.0 "Comparator Voltage Reference Module"** for internal reference specifications.

## 10.3 Comparator Response Time

Response time is the minimum time after selecting a new reference voltage or input source before the comparator output is to have a valid level. If the comparator inputs are changed, a delay must be used to allow the comparator to settle to its new state. Please see Table 15-7 for comparator response time specifications.

## 10.4 Comparator Output

The comparator output is read through the CxOUT bit in the CM1CON0 or CM2CON0 register. This bit is read-only. The comparator output may also be used externally, see **Section 10.1 "Comparator Operation"**.

| **Note:** | Analog levels on any pin that is defined as a digital input may cause the input buffer to consume more current than is specified. |
|---|---|

## 10.5 Comparator Wake-up Flag

The Comparator Wake-up Flag bit, CWIF, in the INTCON0 register, is set whenever all of the following conditions are met:

- $\overline{\text{C1WU}}$ = 0 (CM1CON0<0>) or $\overline{\text{C2WU}}$ = 0 (CM2CON0<0>)
- CM1CON0 or CM2CON0 has been read to latch the last known state of the C1OUT and C2OUT bit (`MOVF CM1CON0, W`)
- The output of a comparator has changed state

The wake-up flag may be cleared in software or by another device Reset.

## 10.6 Comparator Operation During Sleep

When the comparator is enabled it is active. To minimize power consumption while in Sleep mode, turn off the comparator before entering Sleep.

## 10.7 Effects of Reset

A Power-on Reset (POR) forces the CMxCON0 register to its Reset state. This forces the Comparator input pins to analog Reset mode. Device current is minimized when analog inputs are present at Reset time.

## 10.8 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 10-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and VSS. The analog input, therefore, must be between VSS and VDD. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latch-up may occur. A maximum source impedance of 10 kΩ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

**FIGURE 15-1: PIC16F527 VOLTAGE-FREQUENCY GRAPH, -40°C ≤ TA ≤ +125°C**

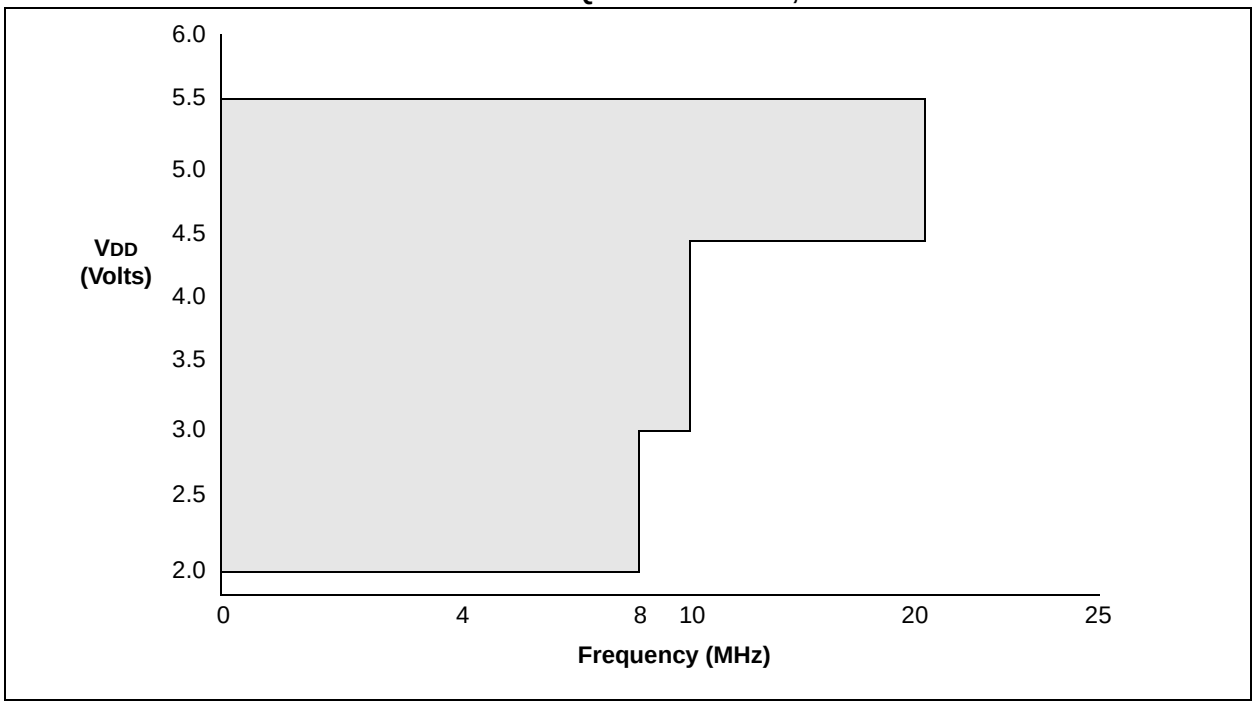



**FIGURE 15-2: MAXIMUM OSCILLATOR FREQUENCY TABLE**

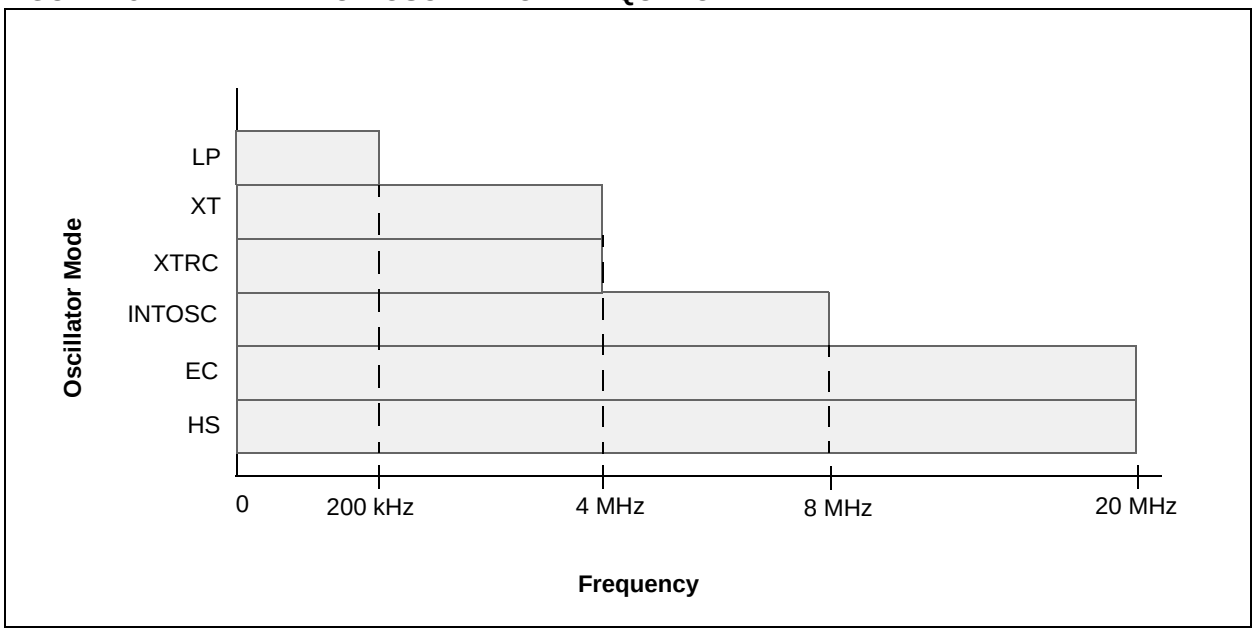


**TABLE 15-1: DC CHARACTERISTICS: PIC16F527 (INDUSTRIAL, EXTENDED) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.†** | **Max.** | **Units** | **Conditions** |
| | VOH | **Output High Voltage** | | | | | |
| D090 | | I/O ports/CLKOUT | VDD – 0.7 | — | — | V | IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C |
| D090A | | | VDD – 0.7 | — | — | V | IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C |
| D092 | | OSC2 | VDD – 0.7 | — | — | V | IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C |
| D092A | | | VDD – 0.7 | — | — | V | IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C |

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F527 be driven with external clock in RC mode.

**2:** The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

**4:** This spec applies to all weak pull-up devices, including the weak pull-up found on $\overline{MCLR}$.

**TABLE 15-1: DC CHARACTERISTICS: PIC16F527 (INDUSTRIAL, EXTENDED) (CONTINUED)**

| DC CHARACTERISTICS | | | Standard Operating Conditions (unless otherwise specified)<br>Operating temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended) | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.†** | **Max.** | **Units** | **Conditions** |
| | | **Capacitive Loading Specs on Output Pins** | | | | | |
| D100 | COSC2 | OSC2 pin | — | — | 15 | pF | In XT, HS and LP modes when external clock is used to drive OSC1. |
| D101 | CIO | All I/O pins and OSC2 | — | — | 50 | pF | |
| | | **Flash Data Memory** | | | | | |
| D120 | ED | Byte endurance | 100K | 1M | — | E/W | -40°C ≤ TA ≤ +85°C |
| D120A | ED | Byte endurance | 10K | 100K | — | E/W | +85°C ≤ TA ≤ +125°C |
| D121 | VDRW | VDD for read/write | VMIN | — | 5.5 | V | |

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F527 be driven with external clock in RC mode.

**2:** The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as coming out of the pin.

**4:** This spec applies to all weak pull-up devices, including the weak pull-up found on $\overline{\text{MCLR}}$.

**TABLE 15-7: CALIBRATED INTERNAL RC FREQUENCIES**

| **AC Characteristics** | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial),<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range is described in **Section 15.1 "DC Characteristics: PIC16F527 (Industrial)"**. | | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Freq. Tolerance** | **Min.** | **Typ.†** | **Max.** | **Units** | **Conditions** |
| F10 | FOSC | Internal Calibrated INTOSC Frequency(1) | ±1% | 7.92 | 8.00 | 8.08 | MHz | 3.5V, 25C |
| | | | ±2% | 7.84 | 8.00 | 8.16 | MHz | 2.5V ≤ VDD ≤ 5.5V<br>0°C ≤ TA ≤ +85°C |
| | | | ±5% | 7.60 | 8.00 | 8.40 | MHz | 2.0V ≤ VDD ≤ 5.5V<br>-40°C ≤ TA ≤ +85°C (Ind.)<br>-40°C ≤ TA ≤ +125°C (Ext.) |

* These parameters are characterized but not tested.

† Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**Note 1:** To ensure these oscillator frequency tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 uF and 0.01 uF values in parallel are recommended.

### TABLE 15-9: BOR, POR, WATCHDOG TIMER AND DEVICE RESET TIMER

| AC Characteristics | | | Standard Operating Conditions (unless otherwise specified)<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range is described in **Section 15.1 "DC Characteristics: PIC16F527 (Industrial)"**. | | | | |
|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| 30 | TMCL | $\overline{\text{MCLR}}$ Pulse Width (low) | 2000* | — | — | ns | VDD = 5.0V |
| 31 | TWDT | Watchdog Timer Time-out Period (no prescaler) | 9*<br>9* | 18*<br>18 | 30*<br>40* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| 32 | TDRT | Device Reset Timer Period | 9*<br>9* | 18*<br>18 | 30*<br>40* | ms<br>ms | VDD = 5.0V (Industrial)<br>VDD = 5.0V (Extended) |
| 34 | TIOZ | I/O High-impedance from $\overline{\text{MCLR}}$ low | — | — | 2000* | ns | |
| 35 | VBOR | Brown-out Reset Voltage | 1.95 | — | 2.25 | V | **(Note 2)** |
| 36* | VHYST | Brown-out Reset Hysteresis | — | 50 | — | mV | |
| 37* | TBOR | Brown-out Reset Minimum Detection Period | 100 | — | — | µs | VDD ≤ VBOR |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**2:** To ensure these voltage tolerances, VDD and VSS must be capacitively decoupled as close to the device as possible. 0.1 µF and 0.01 µF values in parallel are recommended.

### TABLE 15-10: DRT (DEVICE RESET TIMER PERIOD)

| Oscillator Configuration | POR Reset | Subsequent Resets |
|---|---|---|
| IntRC, ExtRC, and EC | 10 µs (typical) + 18 ms (DRTEN = 1) | 10 µs (typical) + 18 ms (DRTEN = 1) |
| XT, HS and LP | 18 ms (typical) | 18 ms (typical) |

### TABLE 15-11: PULL-UP RESISTOR RANGES

| VDD (Volts) | Temperature (°C) | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| **RB0-RB7** | | | | | |
| 2.0 | -40 | 73K | 105K | 186K | Ω |
| | 25 | 73K | 113K | 187K | Ω |
| | 85 | 82K | 123K | 190K | Ω |
| | 125 | 86K | 132k | 190K | Ω |
| 5.5 | -40 | 15K | 21K | 33K | Ω |
| | 25 | 15K | 22K | 34K | Ω |
| | 85 | 19K | 26k | 35K | Ω |
| | 125 | 23K | 29K | 35K | Ω |
| **$\overline{\text{MCLR}}$** | | | | | |
| 2.0 | -40 | 63K | 81K | 96K | Ω |
| | 25 | 77K | 93K | 116K | Ω |
| | 85 | 82K | 96k | 116K | Ω |
| | 125 | 86K | 100K | 119K | Ω |
| 5.5 | -40 | 16K | 20k | 22K | Ω |
| | 25 | 16K | 21K | 23K | Ω |
| | 85 | 24K | 25k | 28K | Ω |
| | 125 | 26K | 27K | 29K | Ω |

**FIGURE 15-8: TIMER0 CLOCK TIMINGS**

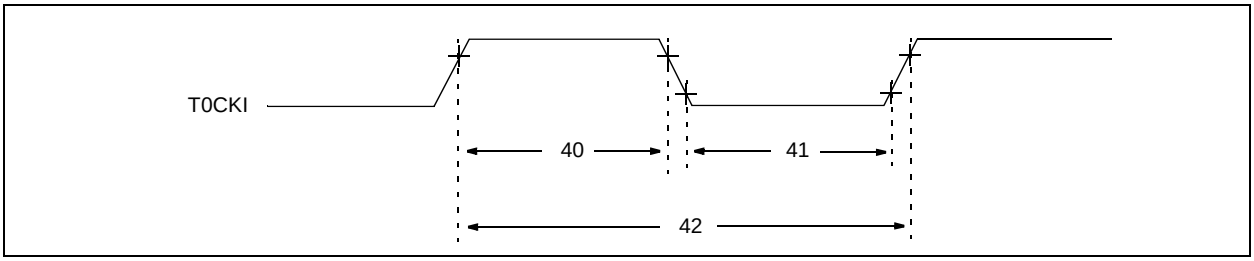



**TABLE 15-12: TIMER0 CLOCK REQUIREMENTS**

| **AC Characteristics** | | | | **Standard Operating Conditions (unless otherwise specified)**<br>Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)<br>-40°C ≤ TA ≤ +125°C (extended)<br>Operating voltage VDD range is described in **Section 15.1 "DC Characteristics: PIC16F527 (Industrial)"**. | | | | |
|---|---|---|---|---|---|---|---|---|
| **Param. No.** | **Sym.** | **Characteristic** | | **Min.** | **Typ.(1)** | **Max.** | **Units** | **Conditions** |
| 40 | Tt0H | T0CKI High Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 41 | Tt0L | T0CKI Low Pulse Width | No Prescaler | 0.5 TCY + 20* | — | — | ns | |
| | | | With Prescaler | 10* | — | — | ns | |
| 42 | Tt0P | T0CKI Period | | 20 or TCY + 40* N | — | — | ns | Whichever is greater. N = Prescale Value (1, 2, 4,..., 256) |

* These parameters are characterized but not tested.

**Note 1:** Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

**FIGURE 16-6: IDD TYPICAL, INTOSC**

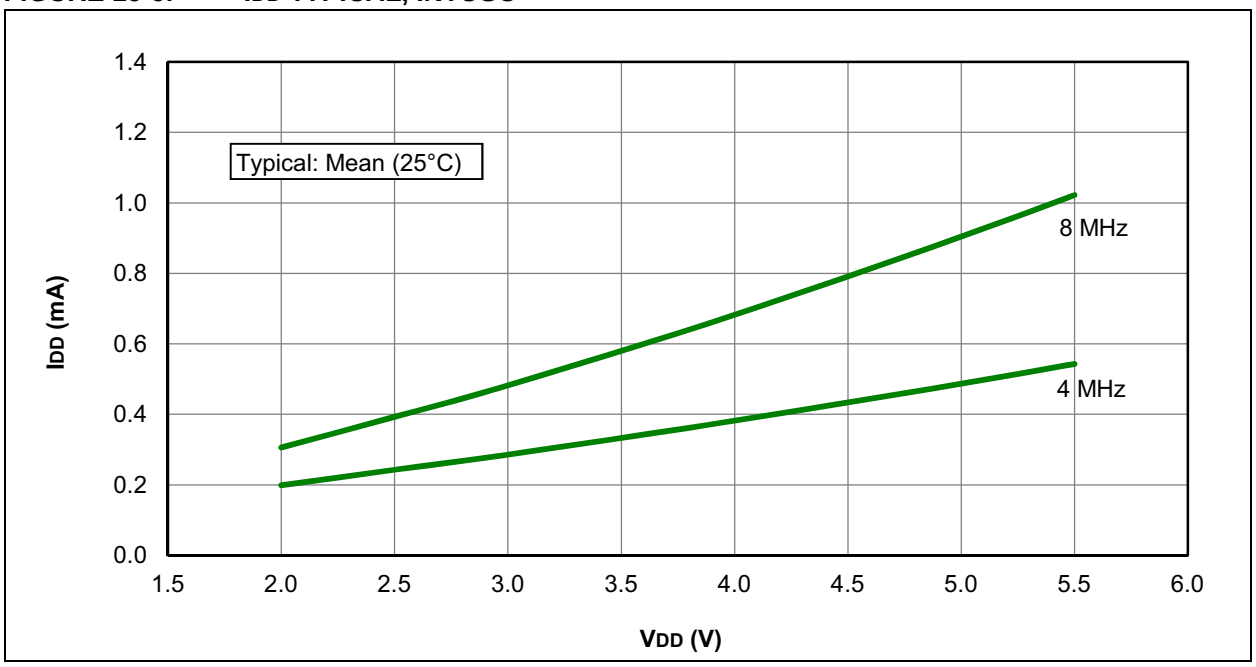



**FIGURE 16-7: IDD MAXIMUM, INTOSC**

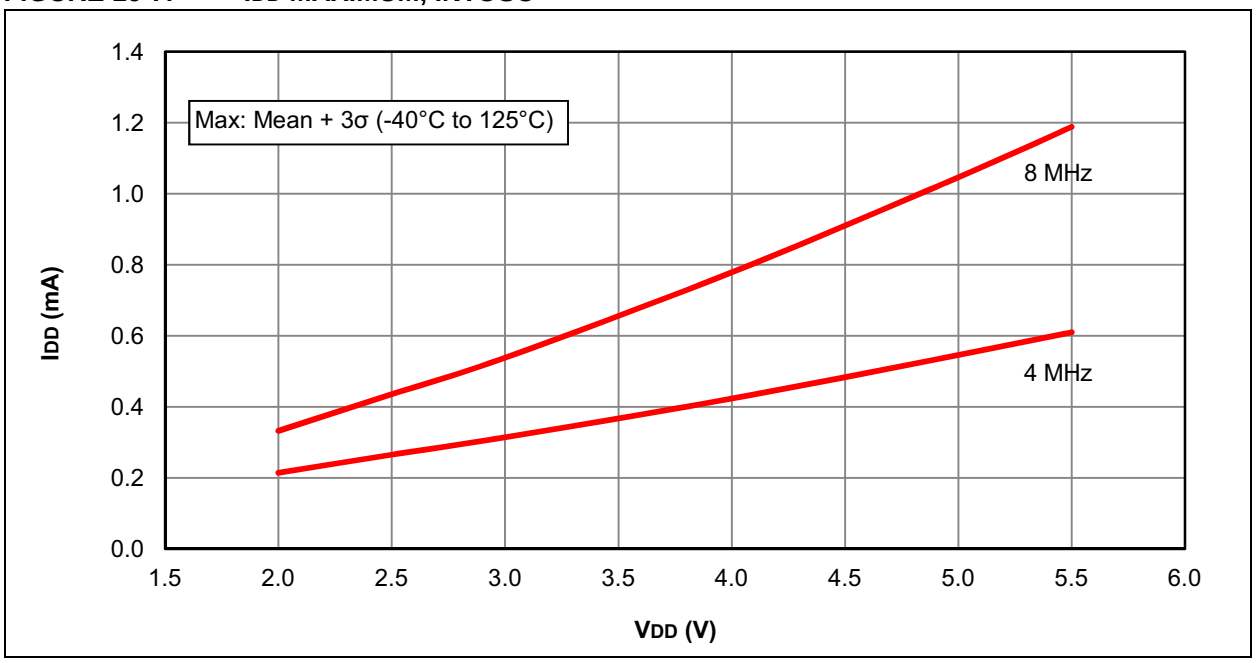


**FIGURE 16-8: IDD TYPICAL, HS OSCILLATOR**

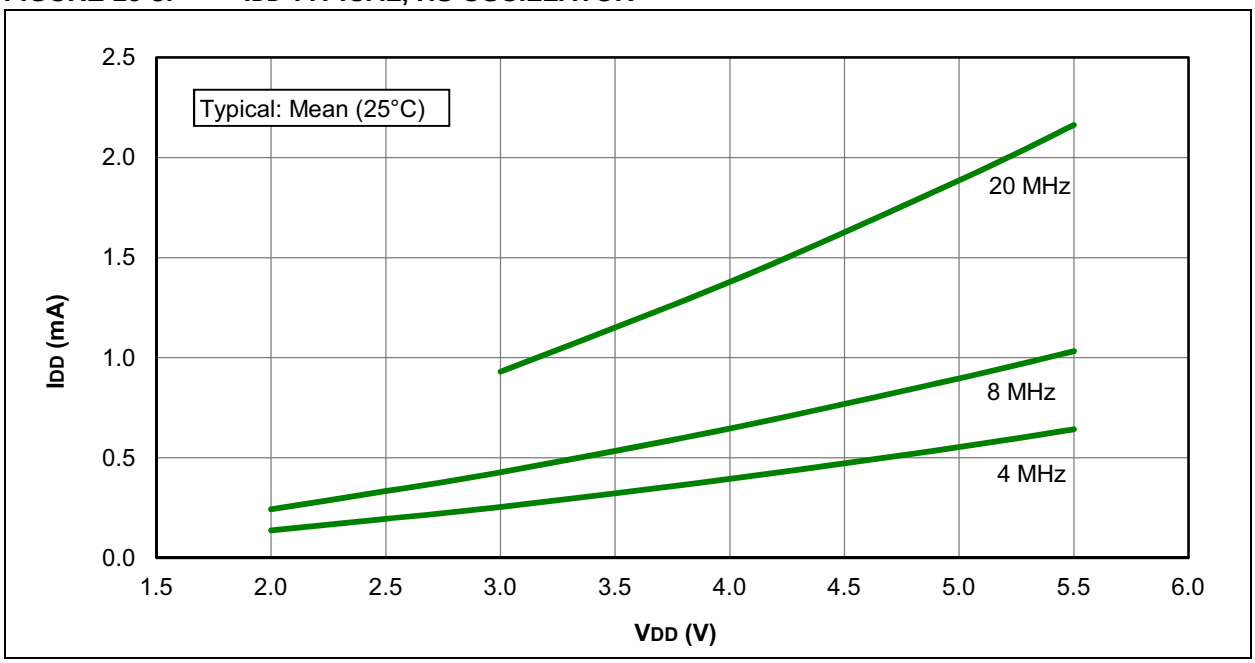



**FIGURE 16-9: IDD MAXIMUM, HS OSCILLATOR**

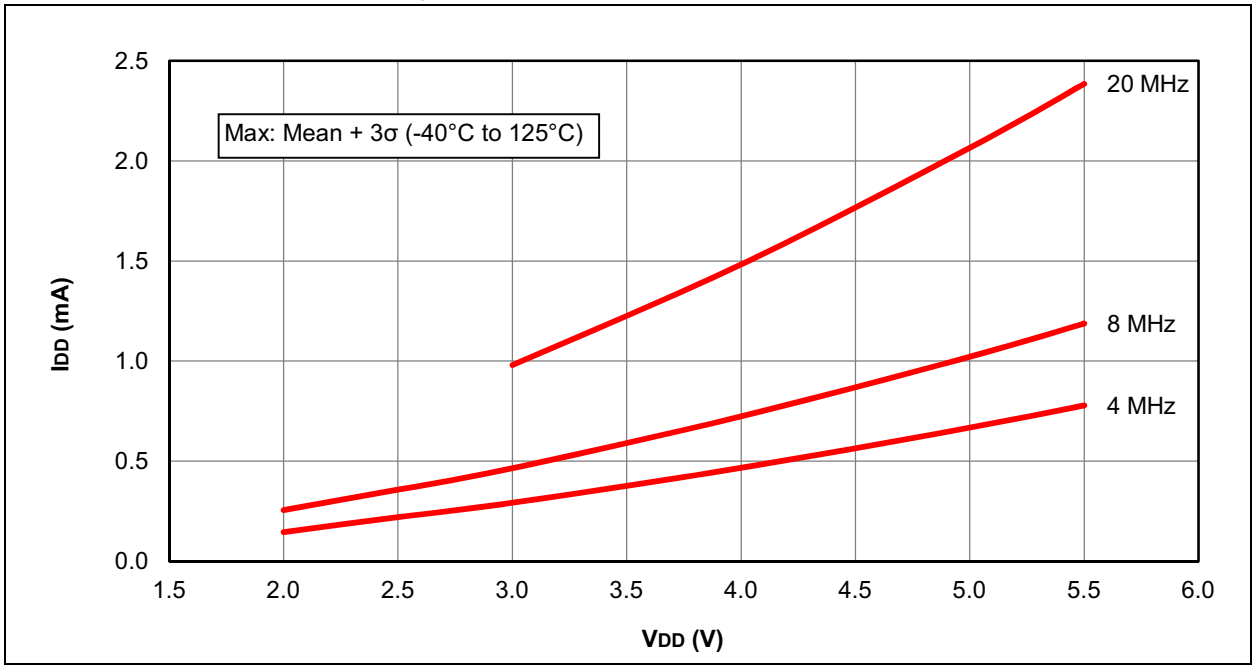


**FIGURE 16-12: IPD, FIXED VOLTAGE REFERENCE (FVR)**

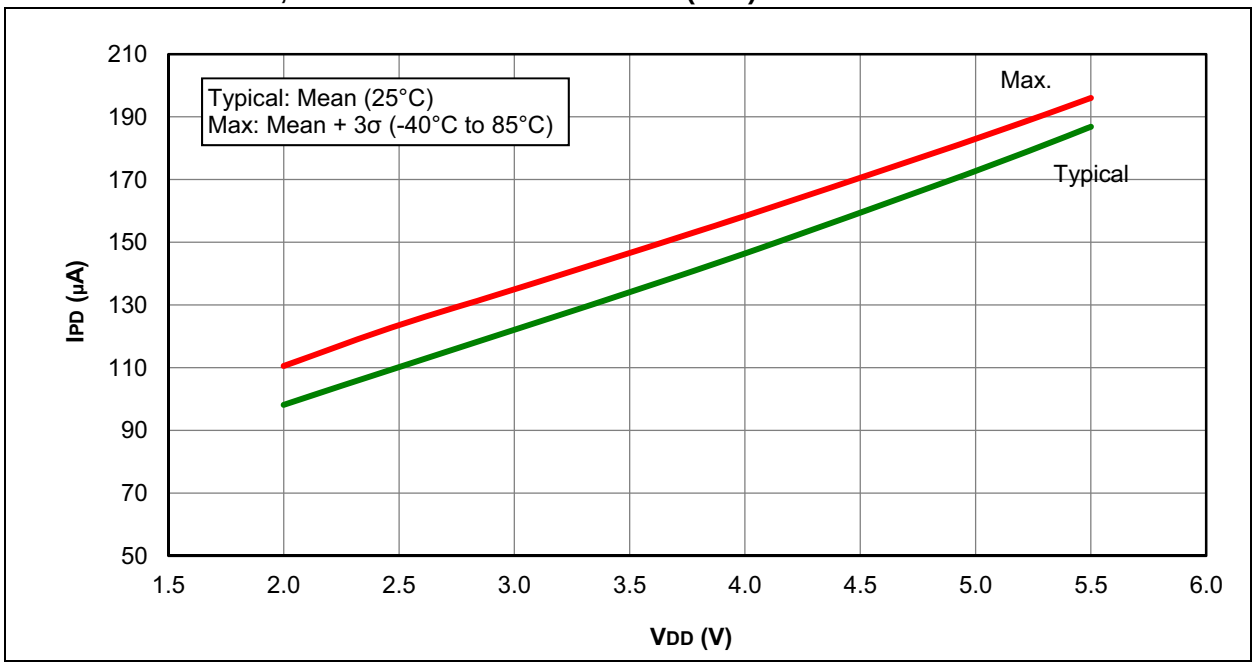
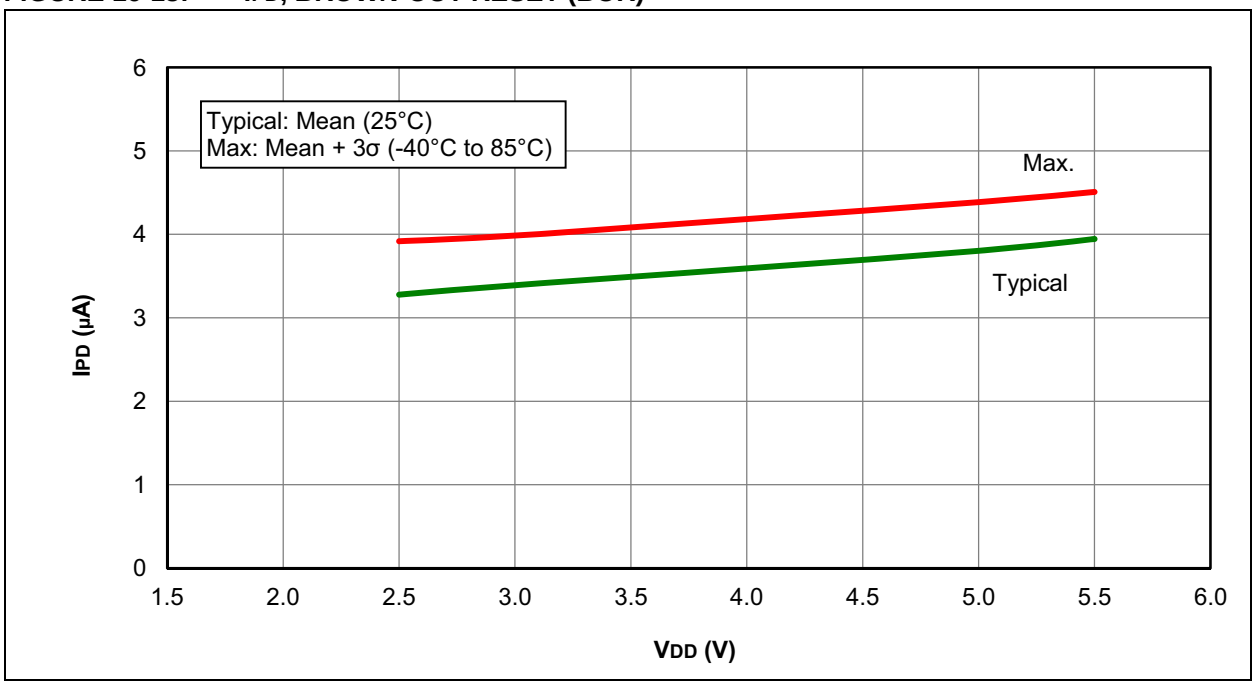
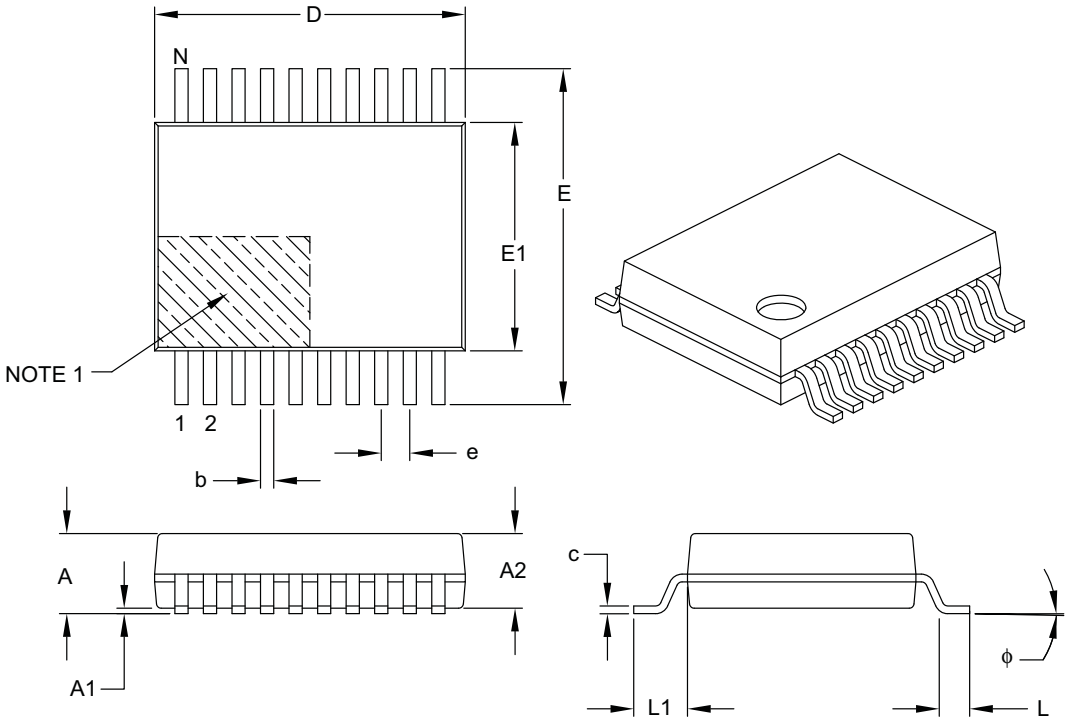



**FIGURE 16-13: IPD, BROWN-OUT RESET (BOR)**



## 20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging




| Units | | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Pins | N | | 20 | |
| Pitch | e | | 0.65 BSC | |
| Overall Height | A | – | – | 2.00 |
| Molded Package Thickness | A2 | 1.65 | 1.75 | 1.85 |
| Standoff | A1 | 0.05 | – | – |
| Overall Width | E | 7.40 | 7.80 | 8.20 |
| Molded Package Width | E1 | 5.00 | 5.30 | 5.60 |
| Overall Length | D | 6.90 | 7.20 | 7.50 |
| Foot Length | L | 0.55 | 0.75 | 0.95 |
| Footprint | L1 | | 1.25 REF | |
| Lead Thickness | c | 0.09 | – | 0.25 |
| Foot Angle | ϕ | 0° | 4° | 8° |
| Lead Width | b | 0.22 | – | 0.38 |

**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B