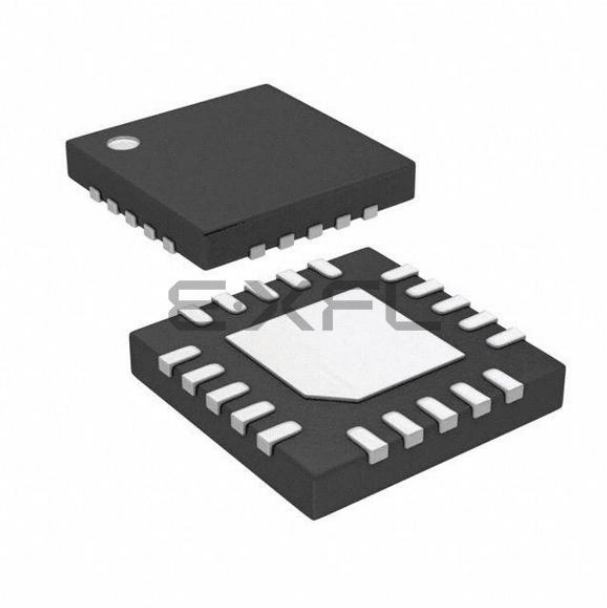

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	17
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-UQFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f527-i-gz

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3.0 ARCHITECTURAL OVERVIEW

The high performance of the PIC16F527 device can be attributed to a number of architectural features commonly found in RISC microprocessors. To begin with, the PIC16F527 device uses a Harvard architecture in which program and data are accessed on separate buses. This improves bandwidth over traditional von Neumann architectures where program and data are fetched on the same bus. Separating program and data memory further allows instructions to be sized differently than the 8-bit wide data word. Instruction opcodes are 12 bits wide, making it possible to have all single-word instructions. A 12-bit wide program memory access bus fetches a 12-bit instruction in a single cycle. A two-stage pipeline overlaps fetch and execution of instructions. Consequently, all instructions execute in a single cycle (200 ns @ 20 MHz, 1 μs @ 4 MHz) except for program branches.

Table 3-1 below lists memory supported by the PIC16F527 device.

TABLE 3-1: PIC16F527 MEMORY

Device	Program Memory	Data Memory	
	Flash (words)	SRAM (bytes)	Flash (bytes)
PIC16F527	1024	68	64

The PIC16F527 device can directly or indirectly address its register files and data memory. All Special Function Registers (SFR), including the PC, are mapped in the data memory. The PIC16F527 device has a highly orthogonal (symmetrical) instruction set that makes it possible to carry out any operation, on any register, using any Addressing mode. This symmetrical nature and lack of “special optimal situations” make programming with the PIC16F527 device simple, yet efficient. In addition, the learning curve is reduced significantly.

The PIC16F527 device contains an 8-bit ALU and working register. The ALU is a general purpose arithmetic unit. It performs arithmetic and Boolean functions between data in the working register and any register file.

The ALU is eight bits wide and capable of addition, subtraction, shift and logical operations. Unless otherwise mentioned, arithmetic operations are two’s complement in nature. In two-operand instructions, one operand is typically the W (working) register. The other operand is either a file register or an immediate constant. In single operand instructions, the operand is either the W register or a file register.

The W register is an 8-bit working register used for ALU operations. It is not an addressable register.

Depending on the instruction executed, the ALU may affect the values of the Carry (C), Digit Carry (DC) and Zero (Z) bits in the STATUS register. The C and DC bits operate as a borrow and digit borrow out bit, respectively, in subtraction. See the `SUBWF` and `ADDWF` instructions for examples.

A simplified block diagram is shown in Figure 3-2, with the corresponding device pins described in Table 3-2.

6.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

6.1 PORTA

PORTA is a 6-bit I/O register. Only the low-order six bits are used (RA<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that RA3 is an input-only pin. The Configuration Word can set several I/Os to alternate functions. When acting as alternate functions, the pins will read as '0' during a port read. Pins RA0, RA1, RA3 and RA4 can be configured with weak pull-ups and also for wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If RA3/MCLR is configured as MCLR, weak pull-up is always on and wake-up on change for this pin is not enabled.

6.2 PORTB

PORTB is a 4-bit I/O register. Only the high-order four bits are used (RB<7:4>). Bits 0 through 3 are unimplemented and read as '0's.

6.3 PORTC

PORTC is an 8-bit I/O register.

6.4 TRIS Register

The Output Driver Control register is loaded with the contents of the W register by executing the `TRIS` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a High-Impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are RA3, which is input-only and the T0CKI pin, which may be controlled by the OPTION register (see Register 4-2).

TRIS registers are "write-only". Active bits in these registers are set (output drivers disabled) upon Reset.

7.0 TIMER0 MODULE AND TMR0 REGISTER

The Timer0 module has the following features:

- 8-bit timer/counter register, TMR0
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select:
  - Edge select for external clock

Figure 7-1 is a simplified block diagram of the Timer0 module.

Timer mode is selected by clearing the T0CS bit of the OPTION register. In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 register is written, the increment is inhibited for the following two cycles (see Figure 7-2 and Figure 7-3). The user can work around this by writing an adjusted value to the TMR0 register.

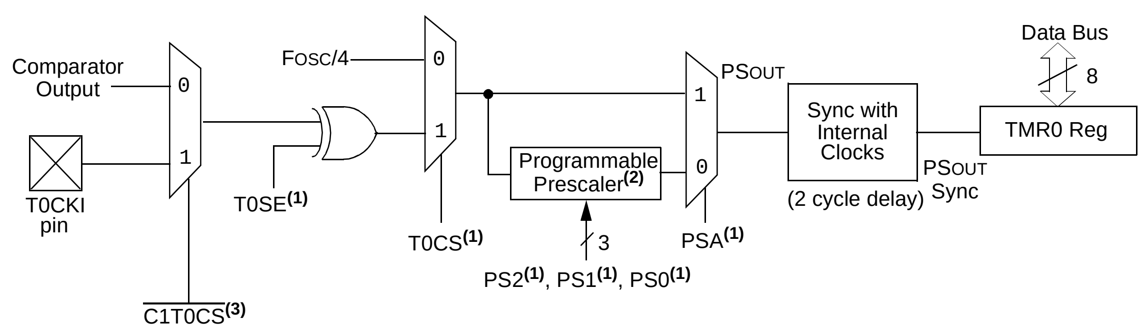
There are two types of Counter mode. The first Counter mode uses the T0CKI pin to increment Timer0. It is selected by setting the T0CS bit of the OPTION register, setting the C1T0CS bit of the CM1CON0 register and setting the C1OUTEN bit of the CM1CON0 register. In this mode, Timer0 will increment either on every rising or falling edge of pin T0CKI. The T0SE bit of the OPTION register determines the source edge. Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed in detail in **Section 7.1 "Using Timer0 with an External Clock"**.

The second Counter mode uses the output of the comparator to increment Timer0. It can be entered in by setting the T0CS bit of the OPTION register, and clearing the C1T0CS bit of the CM1CON0 register (C1OUTEN [CM1CON0<6>] does not affect this mode of operation). This enables an internal connection between the comparator and the Timer0.

The prescaler may be used by either the Timer0 module or the Watchdog Timer, but not both. The prescaler assignment is controlled in software by the control bit, PSA of the OPTION register. Clearing the PSA bit will assign the prescaler to Timer0. The prescaler is not readable or writable. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable. **Section 7.2 "Prescaler"** details the operation of the prescaler.

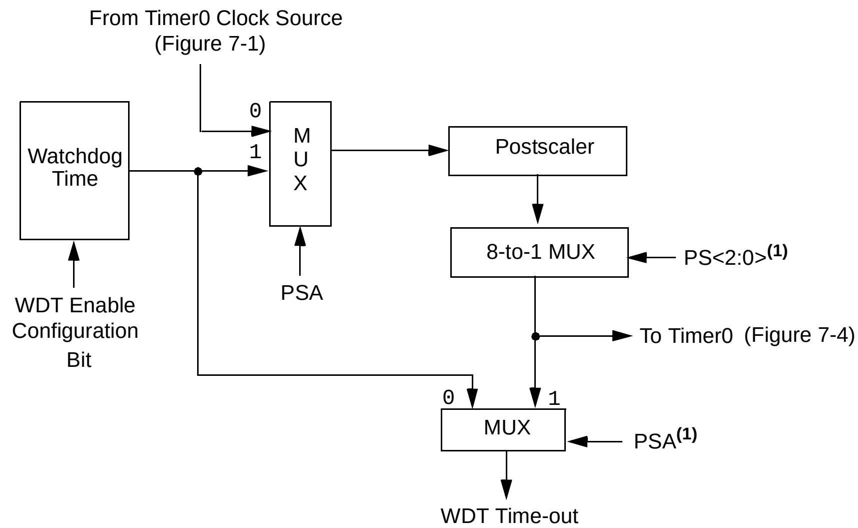
A summary of registers associated with the Timer0 module is found in Table 7-1.

FIGURE 7-1: TIMER0 BLOCK DIAGRAM



Note 1: Bits T0CS, T0SE, PSA, PS2, PS1 and PS0 are located in the OPTION register (see Register 4-2).
2: The prescaler is shared with the Watchdog Timer.
3: The C1T0CS bit is in the CM1CON0 register.

FIGURE 8-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: PSA, PS<2:0> are bits in the OPTION register.

TABLE 8-5: REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
OPTION	$\overline{\text{RAWU}}$	$\overline{\text{RAPU}}$	T0SC	T0SE	PSA	PS2	PS1	PS0	17

Legend: Shaded boxes = Not used by Watchdog Timer.

8.8 Time-out Sequence ($\overline{\text{TO}}$) and Power-down ($\overline{\text{PD}}$) Reset Status

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{\text{MCLR}}$ or Watchdog Timer (WDT) Reset.

TABLE 8-6: $\overline{\text{TO}}$/$\overline{\text{PD}}$ STATUS AFTER RESET

$\overline{\text{TO}}$	$\overline{\text{PD}}$	Reset Caused By
0	0	WDT wake-up from Sleep
0	u	WDT time-out (not from Sleep)
1	0	$\overline{\text{MCLR}}$ wake-up from Sleep
1	1	Power-up or Brown-out Reset
u	u	$\overline{\text{MCLR}}$ not during Sleep

Legend: u = unchanged

Note 1: The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits maintain their status (u) until a Reset occurs. A low pulse on the $\overline{\text{MCLR}}$ input does not change the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ Status bits.

8.11 Interrupts

The interrupt feature allows certain events to preempt normal program flow. Firmware is used to determine the source of the interrupt and act accordingly. Some interrupts can be configured to wake the MCU from Sleep mode.

These following interrupt sources are available on the PIC16F527 device:

- Timer0 Overflow
- ADC Completion
- Comparator Output Change
- Interrupt-on-change pin

Refer to the corresponding chapters for details.

8.11.1 OPERATION

Interrupts are disabled upon any device Reset. They are enabled by setting the following bits:

- GIE bit of the INTCON register
- Interrupt Enable bit(s) for the specific interrupt event(s)

The enable bits for specific interrupts can be found in the INTCON1 register. An interrupt is recorded for a specific interrupt via flag bits found in the INTCON0 register.

The ADC Conversion flag and the Timer0 Overflow flags will be set regardless of the status of the GIE and individual interrupt enable bits.

The Comparator and Interrupt-on-change flags must be enabled for use. One or both of the comparator outputs can be enabled to affect the interrupt flag by clearing the $\overline{\text{C1WU}}$ bit in the CM1CON0 register and the $\overline{\text{C2WU}}$ bit in the CM2CON0 register. The Interrupt-on-change flag is enabled by clearing the $\overline{\text{RAWU}}$ bit in the OPTION register.

The following events happen when an interrupt event occurs while the GIE bit is set:

- Current prefetched instruction is flushed
- GIE bit is cleared
- Current Program Counter (PC) is pushed onto the stack
- Several registers are automatically switched to a secondary set of registers to store critical data. (See **Section 8.12 "Automatic Context Switching"**)
- PC is loaded with the interrupt vector 0004h

The firmware within the Interrupt Service Routine (ISR) should determine the source of the interrupt by polling the interrupt flag bits. The interrupt flag bits must be cleared before exiting the ISR to avoid repeated interrupts. Because the GIE bit is cleared, any interrupt that occurs while executing the ISR will be recorded through its interrupt flag, but will not cause the processor to redirect to the interrupt vector.

8.12 Automatic Context Switching

While the device is executing from the ISR, a secondary set of W, STATUS, FSR and BSR registers are used by the CPU. These registers are still addressed at the same location, but hold persistent, independent values for use inside the ISR. This allows the contents of the primary set of registers to be unaffected by interrupts in the main line execution. The contents of the secondary set of context registers are visible in the SFR map as the IW, ISTATUS, IFSR and IBSR registers. When executing code from within the ISR, these registers will read back the main line context, and vice versa.

The `RETFIE` instruction exits the ISR by popping the previous address from the stack, switching back to the original set of critical registers and setting the GIE bit.

For additional information on a specific interrupt's operation, refer to its peripheral chapter.

Note 1:	Individual interrupt flag bits may be set, regardless of the state of any other enable bits.
2:	All interrupts will be ignored while the GIE bit is cleared. Any interrupt occurring while the GIE bit is clear will be serviced when the GIE bit is set again.
3:	All interrupts should be disabled prior to executing writes or row erases in the self-writable Flash data memory.
4:	The user must manage the contents of the context registers if they are using interrupts that will vector to the Interrupt Service Routine (ISR). The context registers (IW, ISTATUS, IFSR and IBSR) power up in unknown states following POR and BOR events.

8.13 Interrupts during Sleep

Any of the interrupt sources can be used to wake from Sleep. To wake from Sleep, the peripheral must be operating without the system clock. The interrupt source must have the appropriate Interrupt Enable bit(s) set prior to entering Sleep.

On waking from Sleep, if the GIE bit is also set, the processor will branch to the interrupt vector. Otherwise, the processor will continue executing instructions after the `SLEEP` instruction. The instruction directly after the `SLEEP` instruction will always be executed before branching to the ISR. Refer to the **Section 8.10 "Power-down Mode (Sleep)"** for more details.

REGISTER 8-3: INTCON1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
ADIE	CWIE	T0IE	RAIE	—	—	—	WUR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADIE:** A/D Converter (ADC) Interrupt Enable bit
1 = Enables the ADC interrupt
0 = Disables the ADC interrupt

bit 6 **CWIE:** Comparator 1 and 2 Interrupt Enable bit
1 = Enables the Comparator 1 and 2 Interrupt
0 = Disables the Comparator 1 and 2 Interrupt

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt

bit 4 **RAIE:** Port A on Pin Change Interrupt Enable bit
1 = Interrupt-on-change pin enabled
0 = Interrupt-on-change pin disabled

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **WUR:** Wake-up Reset Enable bit
1 = Interrupt source causes device Reset on wake-up
0 = Interrupt source wakes up device from Sleep (Vector to ISR or inline execution)

9.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D Converter allows conversion of an analog signal into an 8-bit digital signal.

9.1 Clock Divisors

The ADC has four clock source settings ADCS<1:0>. There are three divisor values 16, 8 and 4. The fourth setting is INTOSC with a divisor of four. These settings will allow a proper conversion when using an external oscillator at speeds from 20 MHz to 350 kHz. Using an external oscillator at a frequency below 350 kHz requires the ADC oscillator setting to be INTOSC/4 (ADCS<1:0> = 11) for valid ADC results.

The ADC requires 13 T_{AD} periods to complete a conversion. The divisor values do not affect the number of T_{AD} periods required to perform a conversion. The divisor values determine the length of the T_{AD} period.

When the ADCS<1:0> bits are changed while an ADC conversion is in process, the new ADC clock source will not be selected until the next conversion is started. This clock source selection will be lost when the device enters Sleep.

Note:	The ADC clock is derived from the instruction clock. The ADCS divisors are then applied to create the ADC clock

9.1.1 VOLTAGE REFERENCE

There is no external voltage reference for the ADC. The ADC reference voltage will always be V_{DD}.

9.1.2 ANALOG MODE SELECTION

The ANS<7:0> bits are used to configure pins for analog input. Upon any Reset, ANS<7:0> defaults to FF. This configures the affected pins as analog inputs. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

9.1.3 ADC CHANNEL SELECTION

The CHS bits are used to select the analog channel to be sampled by the ADC. The CHS<3:0> bits can be changed at any time without adversely effecting a conversion. To acquire an external analog signal, the CHS<3:0> selection must match one of the pin(s) selected by the ANS<7:0> bits. When the ADC is on (ADON = 1) and a channel is selected that is also being used by the comparator, then both the comparator and the ADC will see the analog voltage on the pin.

Note:	It is the user's responsibility to ensure that the use of the ADC and op amp simultaneously on the same pin does not adversely affect the signal being monitored or adversely effect device operation.

When the CHS<3:0> bits are changed during an ADC conversion, the new channel will not be selected until the current conversion is completed. This allows the current conversion to complete with valid results. All channel selection information will be lost when the device enters Sleep.

9.1.4 THE GO/$\overline{\text{DONE}}$ BIT

The GO/$\overline{\text{DONE}}$ bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/$\overline{\text{DONE}}$ bit starts a conversion. When the conversion is complete, the ADC module clears the GO/$\overline{\text{DONE}}$ bit and sets the ADIF bit in the INTCON0 register.

A conversion can be terminated by manually clearing the GO/$\overline{\text{DONE}}$ bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

The GO/$\overline{\text{DONE}}$ bit is cleared when the device enters Sleep, stopping the current conversion. The ADC does not have a dedicated oscillator, it runs off of the instruction clock. Therefore, no conversion can occur in Sleep.

The GO/$\overline{\text{DONE}}$ bit cannot be set when ADON is clear.

9.1.5 A/D ACQUISITION REQUIREMENTS

For the ADC to meet its specified accuracy, the charge holding capacitor (C_{HOLD}) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-1. The source impedance (R_S) and the internal sampling switch (R_{SS}) impedance directly affect the time required to charge the capacitor C_{HOLD}. The sampling switch (R_{SS}) impedance varies over the device voltage (V_{DD}), see Figure 9-1. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSb error is used (256 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

REGISTER 12-1: OPACON: OP AMP CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0
—	—	—	—	—	—	OPA2ON	OPA1ON
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-2 **Unimplemented:** Read as '0'

bit 1 **OPA2ON:** Op Amp Enable bit
1 = Op amp 2 is enabled
0 = Op amp 2 is disabled

bit 0 **OPA1ON:** Op Amp Enable bit
1 = Op amp 1 is enabled
0 = Op amp 1 is disabled

12.2 Effects of a Reset

A device Reset forces all registers to their Reset state. This disables both op amps.

12.3 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product (GBWP)

Common mode voltage range is the specified voltage range for the OP+ and OP- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between 0 and V_{DD}-1.5V. Behavior for common mode voltages greater than V_{DD}-1.5V, or below 0V, are beyond the normal operating range.

Leakage current is a measure of the small source or sink currents on the OP+ and OP- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OP+ and OP- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OP+ and OP- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the common mode voltage.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OP+) - (OP-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB.

12.4 Effects of Sleep

When enabled, the op amps continue to operate and consume current while the processor is in Sleep mode.

TABLE 12-1: REGISTERS ASSOCIATED WITH THE OPA MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
ANSEL	ANS7	ANS6	ANS5	ANS4	ANS3	ANS2	ANS1	ANS0	29
OPACON	—	—	—	—	—	—	OPA2ON	OPA1ON	67
TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								—

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for the OPA module.

TABLE 15-2: COMPARATOR SPECIFICATIONS

Comparator Specifications	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to 125°C					
Characteristics	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Input offset voltage	VOS	—	± 5.0	±10.0	mV	
Input common mode voltage*	VCM	0	—	VDD – 1.5	V	
CMRR*	CMRR	55	—	—	db	
Response Time(1)*	TRT	—	150	—	ns	
Comparator Mode Change to Output Valid*	TMC2COV	—	—	10	µs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD – 1.5)/2 while the other input transitions from VSS to VDD – 1.5V.

TABLE 15-3: COMPARATOR VOLTAGE REFERENCE (CVREF) SPECIFICATIONS

Sym.	Characteristics	Min.	Typ.	Max.	Units	Comments
CVRES	Resolution	— —	VDD/24* VDD/32	— —	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Absolute Accuracy(2)	— —	— —	±1/2* ±1/2*	LSb LSb	Low Range (VRR = 1) High Range (VRR = 0)
	Unit Resistor Value (R)	— —	2K*	—	Ω	
	Settling Time(1)	—	—	10*	µs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

2: Do not use reference externally when VDD < 2.7V. Under this condition, reference should only be used with comparator Voltage Common mode observed.

TABLE 15-4: FIXED INPUT REFERENCE SPECIFICATION

Input Reference Specifications	Standard Operating Conditions (unless otherwise stated) Operating temperature -40°C to 125°C					
Characteristics	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
Absolute Accuracy	VFIR	0.5	0.60	0.7	V	

FIGURE 15-8: TIMER0 CLOCK TIMINGS

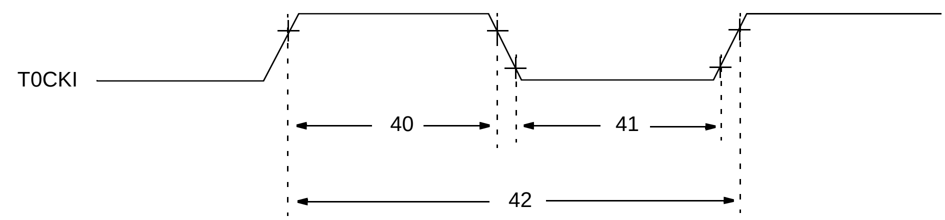


TABLE 15-12: TIMER0 CLOCK REQUIREMENTS

<table>
<tr><td colspan="3">AC Characteristics</td><td colspan="6">Standard Operating Conditions (unless otherwise specified)
Operating Temperature -40°C ≤ TA ≤ +85°C (industrial)
-40°C ≤ TA ≤ +125°C (extended)
Operating voltage VDD range is described in Section 15.1 “DC Characteristics: PIC16F527 (Industrial)”.</td></tr>
<tr><td>Param. No.</td><td>Sym.</td><td colspan="2">Characteristic</td><td>Min.</td><td>Typ.(1)</td><td>Max.</td><td>Units</td><td>Conditions</td></tr>
<tr><td rowspan="2">40</td><td rowspan="2">Tt0H</td><td rowspan="2">T0CKI High Pulse Width</td><td>No Prescaler</td><td>0.5 TCY + 20*</td><td>—</td><td>—</td><td>ns</td><td rowspan="2"></td></tr>
<tr><td>With Prescaler</td><td>10*</td><td>—</td><td>—</td><td>ns</td></tr>
<tr><td rowspan="2">41</td><td rowspan="2">Tt0L</td><td rowspan="2">T0CKI Low Pulse Width</td><td>No Prescaler</td><td>0.5 TCY + 20*</td><td>—</td><td>—</td><td>ns</td><td rowspan="2"></td></tr>
<tr><td>With Prescaler</td><td>10*</td><td>—</td><td>—</td><td>ns</td></tr>
<tr><td>42</td><td>Tt0P</td><td colspan="2">T0CKI Period</td><td>20 or TCY + 40* N</td><td>—</td><td>—</td><td>ns</td><td>Whichever is greater.
N = Prescale Value (1, 2, 4,..., 256)</td></tr>
</table>

* These parameters are characterized but not tested.

Note 1: Data in the Typical (“Typ”) column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

16.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "MAXIMUM", "Max.", "MINIMUM" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

FIGURE 16-2: IDD TYPICAL, XT AND EXTRC OSCILLATOR

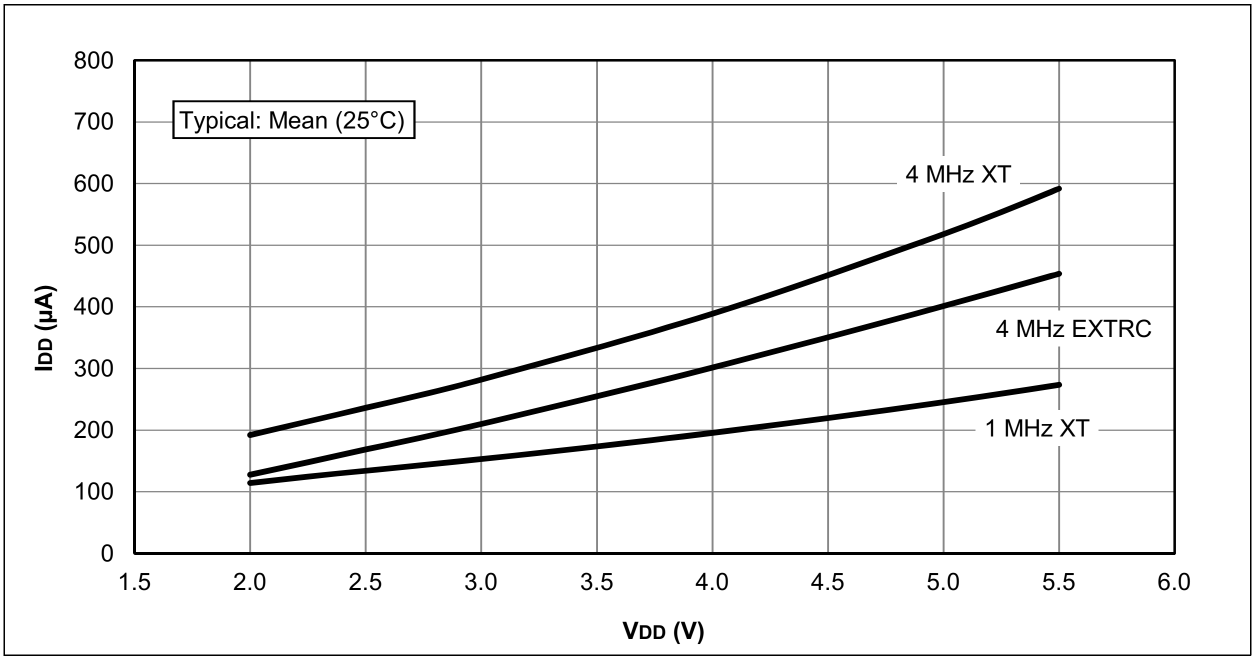


FIGURE 16-3: IDD MAXIMUM, XT AND EXTRC OSCILLATOR

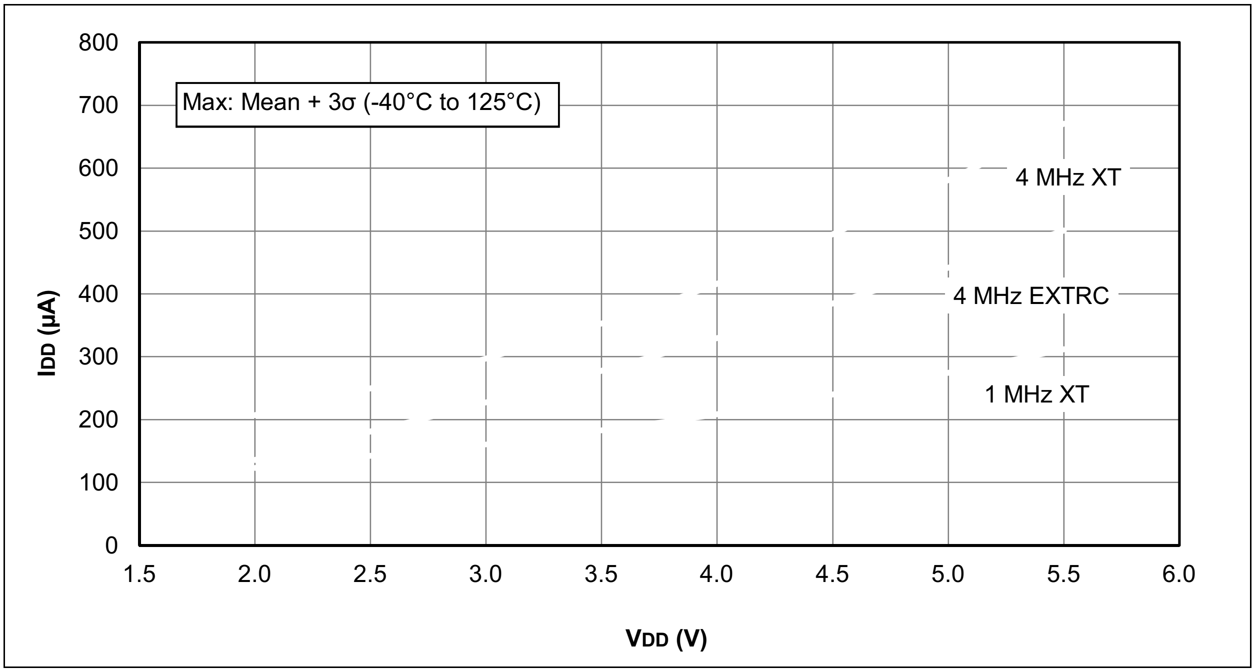


FIGURE 16-14: IPD, SINGLE COMPARATOR

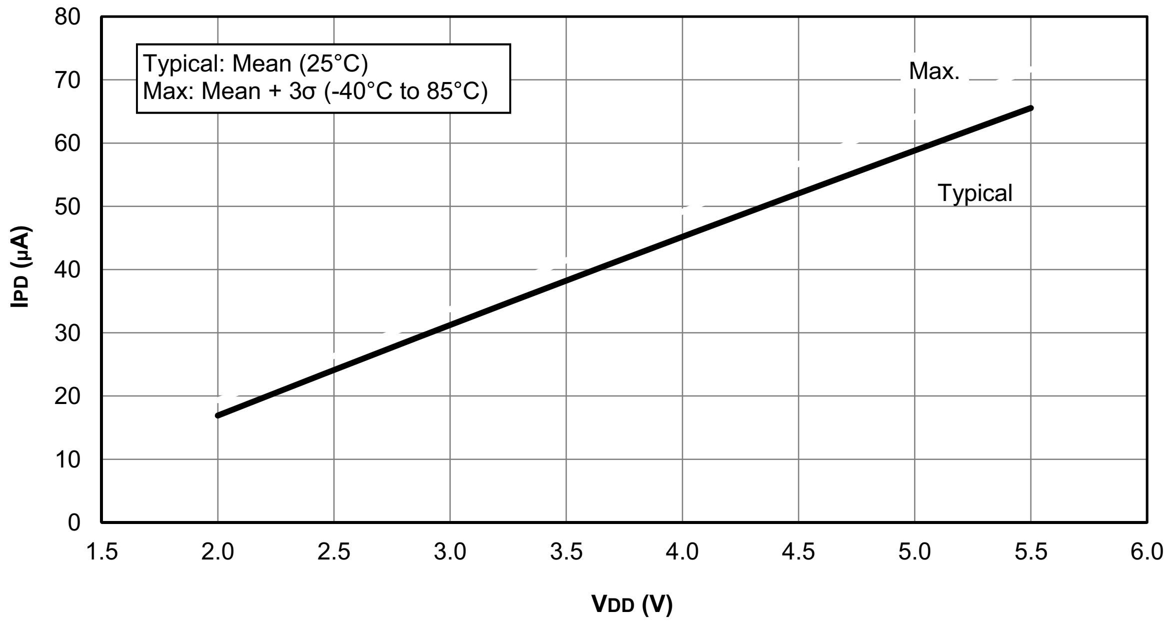


FIGURE 16-15: IPD, CVREF

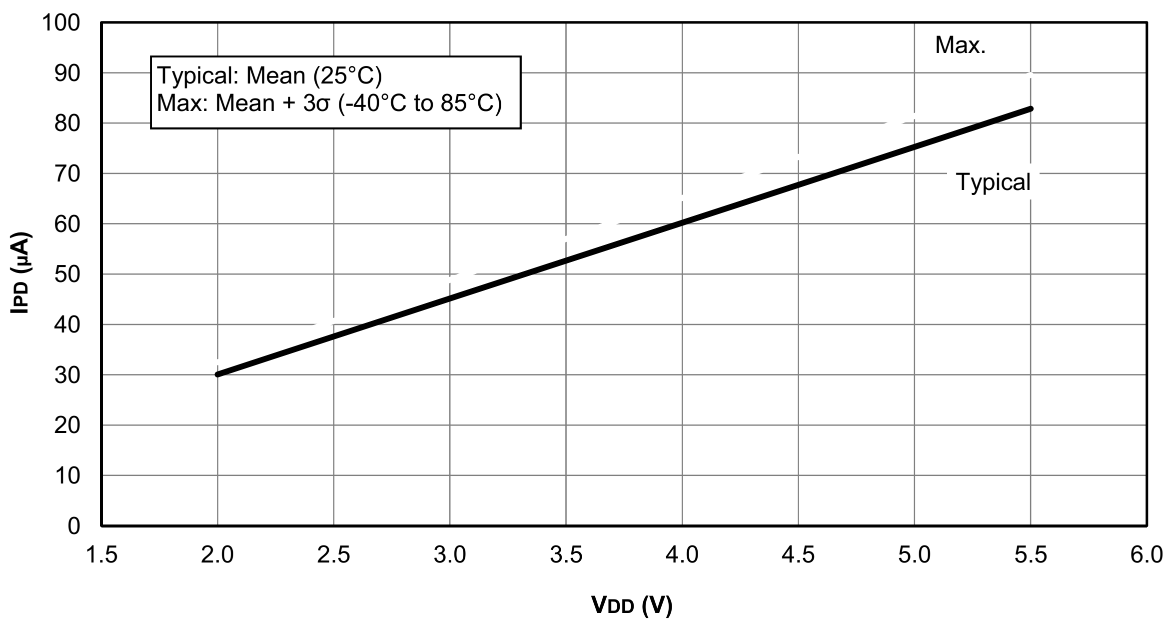


FIGURE 16-23: BROWN-OUT RESET VOLTAGE

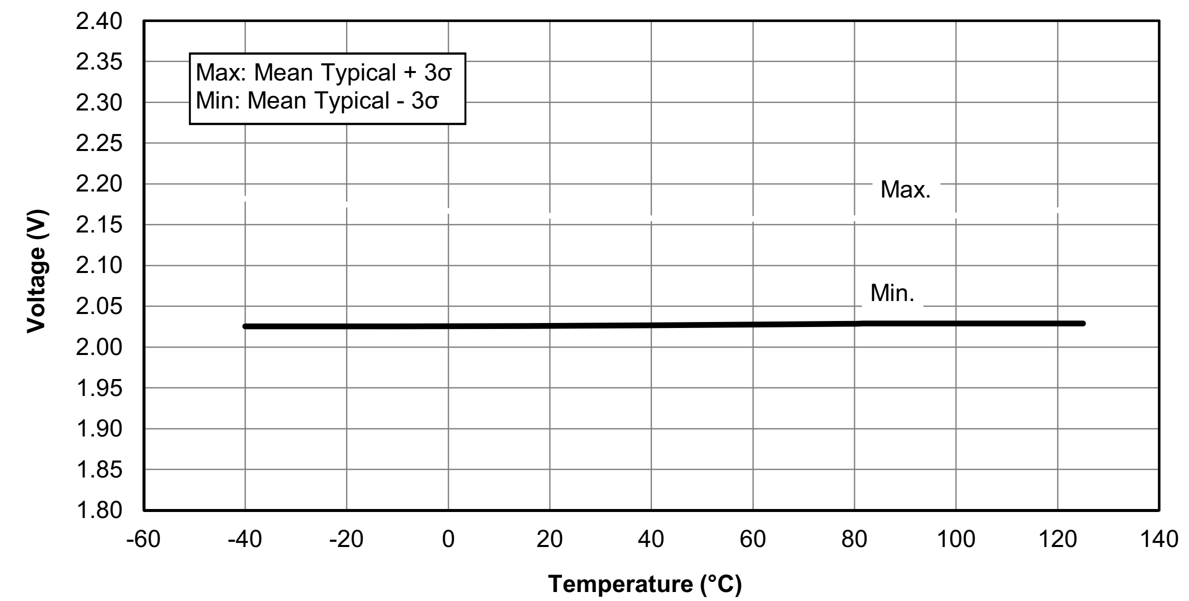
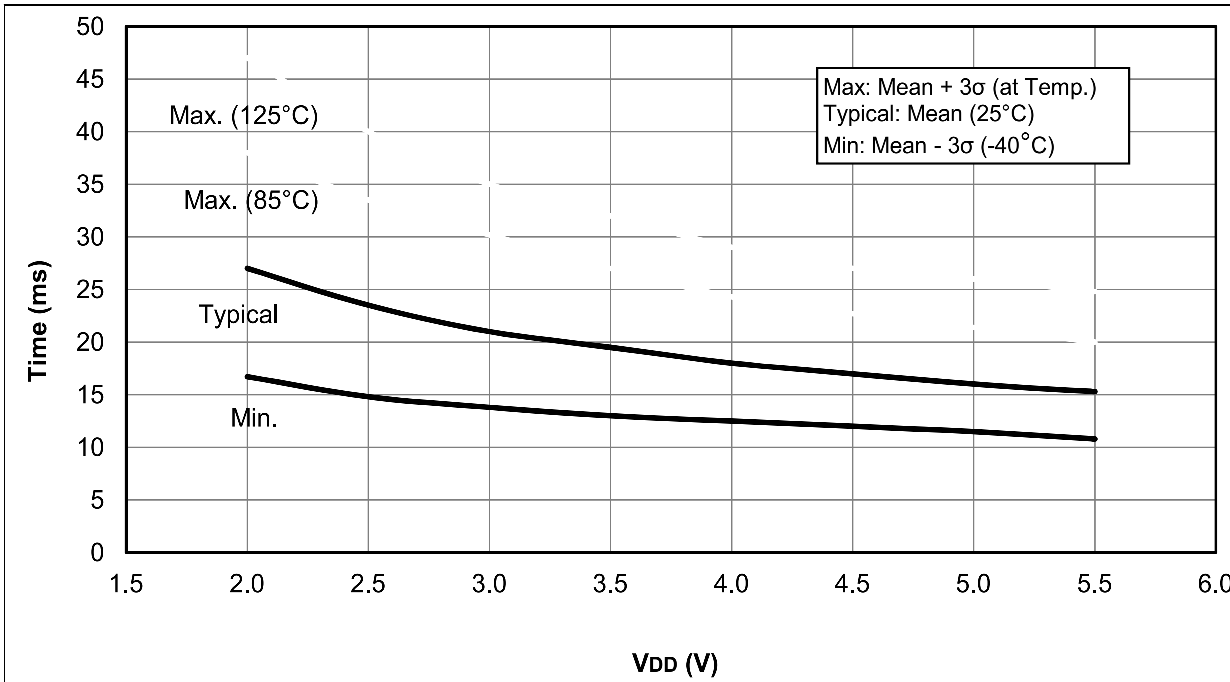
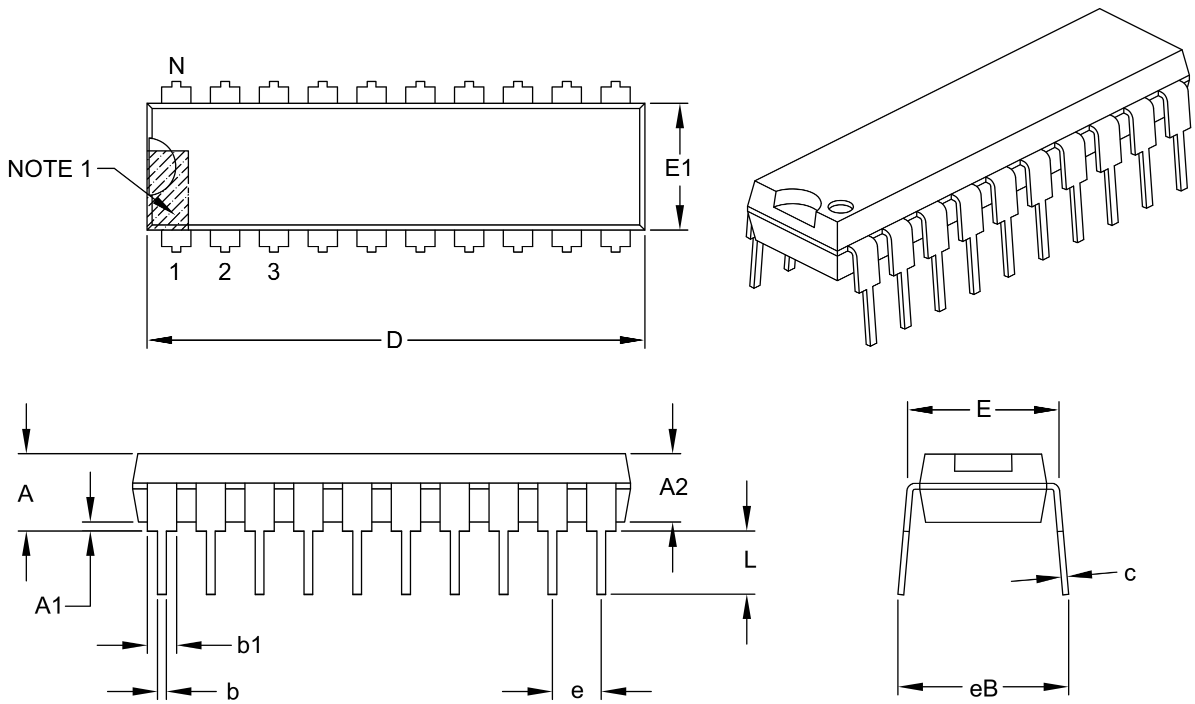


FIGURE 16-24: WDT TIME-OUT PERIOD



20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

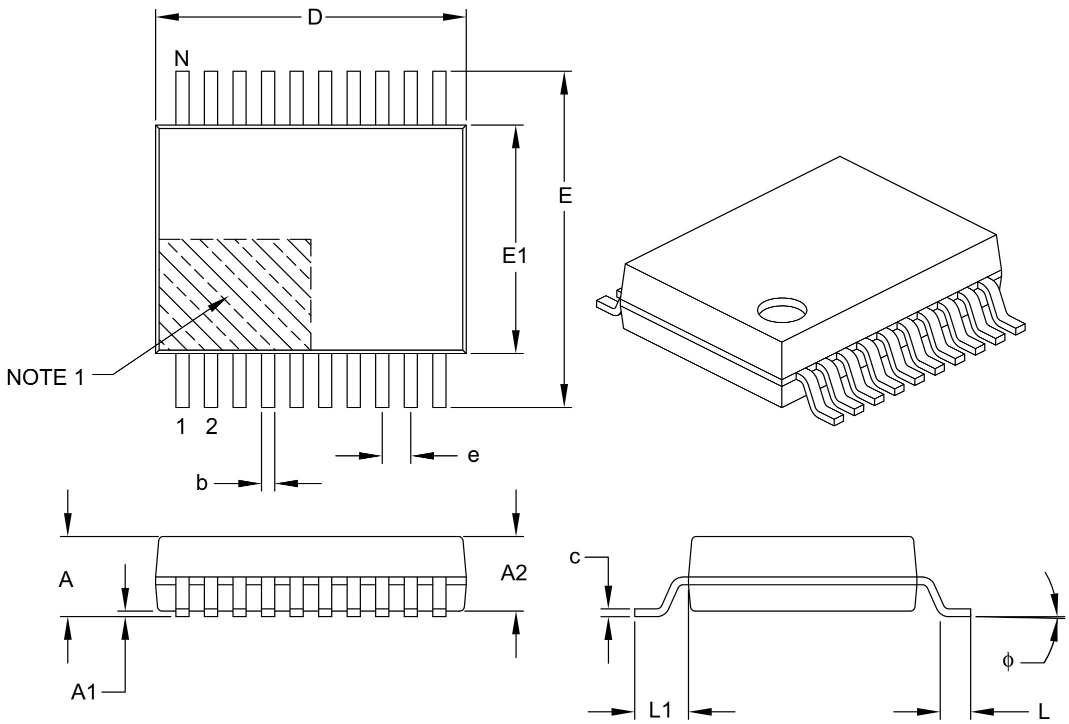
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

20-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



		Units	MILLIMETERS		
		Dimension Limits	MIN	NOM	MAX
Number of Pins	N		20		
Pitch	e		0.65 BSC		
Overall Height	A		–	–	2.00
Molded Package Thickness	A2		1.65	1.75	1.85
Standoff	A1		0.05	–	–
Overall Width	E		7.40	7.80	8.20
Molded Package Width	E1		5.00	5.30	5.60
Overall Length	D		6.90	7.20	7.50
Foot Length	L		0.55	0.75	0.95
Footprint	L1		1.25 REF		
Lead Thickness	c		0.09	–	0.25
Foot Angle	φ		0°	4°	8°
Lead Width	b		0.22	–	0.38

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.

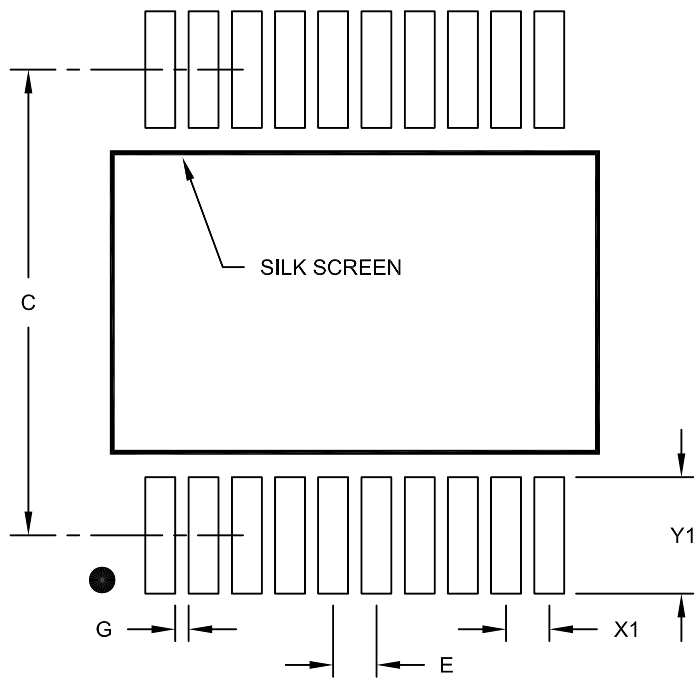
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-072B

20-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X20)	X1			0.45
Contact Pad Length (X20)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

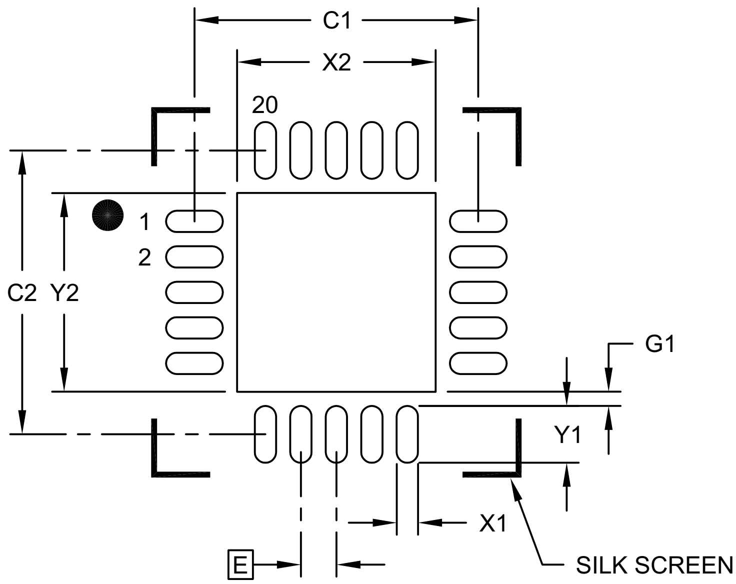
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2072A

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

	Units	MILLIMETERS		
	Dimension Limits	MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.20		

Notes:

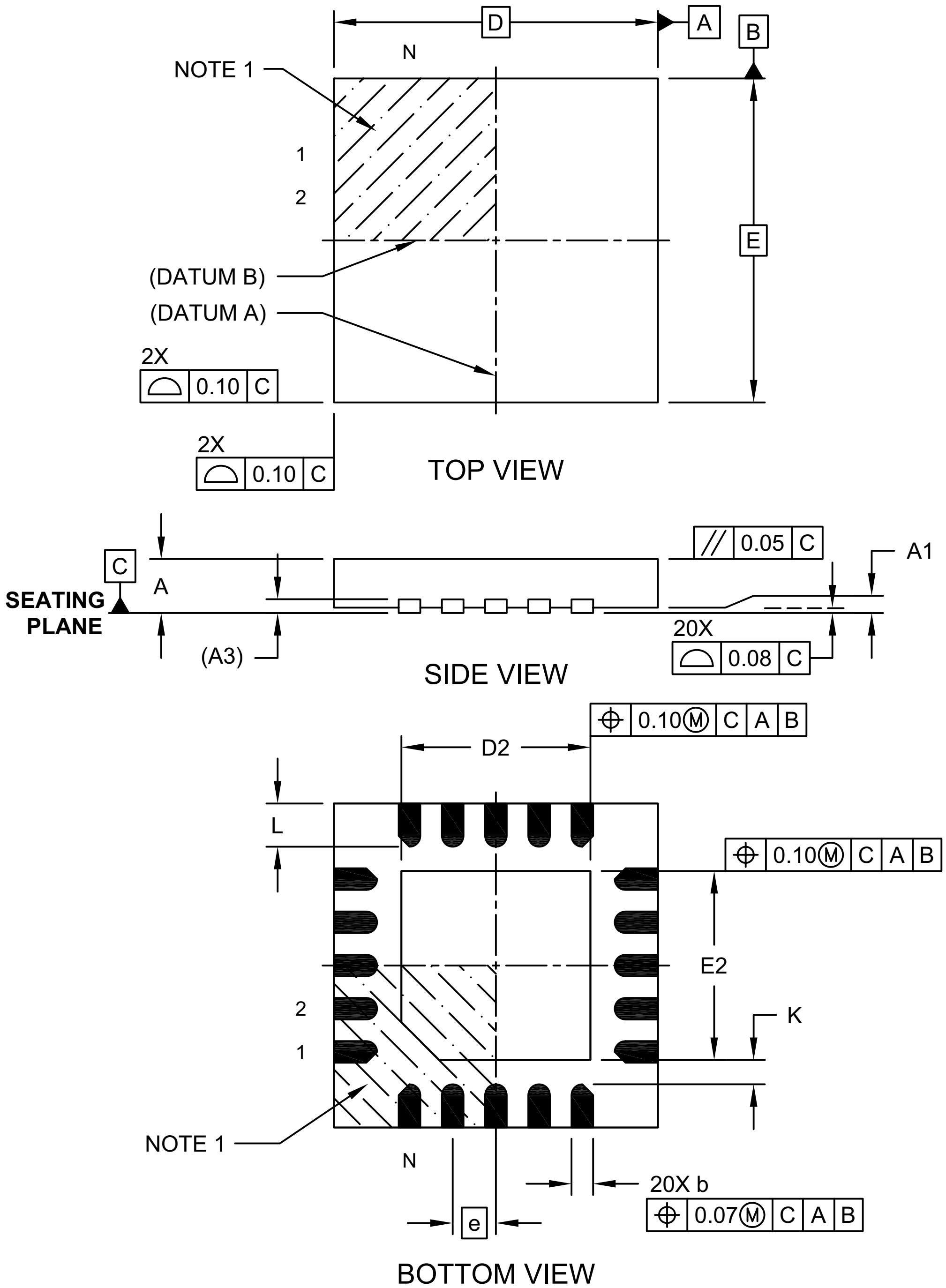
1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2255A

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JP) - 3x3x0.50 mm Body [UQFN]

Note:	For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-256A Sheet 1 of 2