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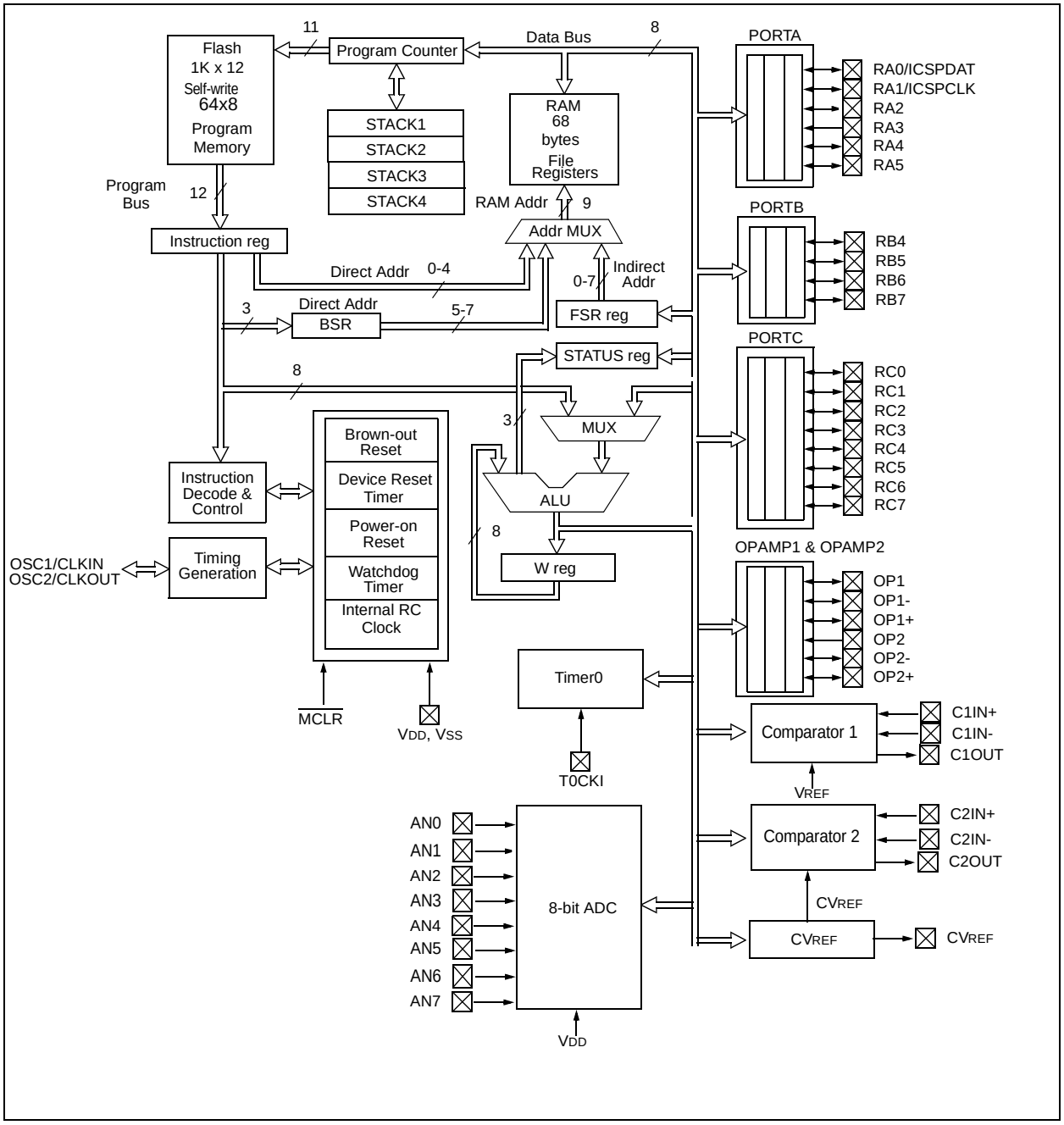
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	17
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-UQFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f527-i-jp

FIGURE 3-1: PIC16F527 BLOCK DIAGRAM



4.5 OSCCAL Register

The Oscillator Calibration (OSCCAL) register is used to calibrate the 8 MHz internal oscillator macro. It contains seven bits of calibration that uses a two's complement scheme for controlling the oscillator speed. See Register 4-3 for details.

REGISTER 4-3: OSCCAL: OSCILLATOR CALIBRATION REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	U-0
CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-1 **CAL<6:0>**: Oscillator Calibration bits

0111111 = Maximum frequency
•
•
•
0000001
0000000 = Center frequency
1111111
•
•
•
1000000 = Minimum frequency

bit 0 **Unimplemented**: Read as '0'

6.6 Register Definitions — PORT Control

TABLE 6-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **RA<5:0>**: PORTA I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

TABLE 6-2: PORTA PINS ORDER OF PRECEDENCE

Priority	RA5	RA4	RA3	RA2	RA1	RA0
1	OSC1	OSC2	RA3/$\overline{\text{MCLR}}$	AN2	CVREF	AN0
2	CLKIN	CLKOUT	—	C1OUT	AN1	C1IN+
3	TRISA5	AN3	—	T0CKI	C1IN-	TRISA0
4	—	TRISA4	—	TRISA2	TRISA1	—

TABLE 6-3: WEAK PULL-UP ENABLED PINS

Device	RA0 Weak Pull-up	RA1 Weak Pull-up	RA3 Weak Pull-up(1)	RA4 Weak Pull-up
PIC16F527	Yes	Yes	Yes	Yes

Note 1: When MCLRE = 1, the weak pull-up on $\overline{\text{MCLR}}$ is always enabled.

REGISTER 6-1: PORTB: PORTB REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	U-0	U-0	U-0	U-0
RB7	RB6	RB5	RB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **RB<7:4>**: PORTB I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

bit 3-0 **Unimplemented**: Read as ‘0’

TABLE 6-4: PORTB PINS ORDER OF PRECEDENCE

Priority	RB7	RB6	RB5	RB4
1	TRISB7	TRISB6	OP2+	OP2-
2	—	—	TRISB5	TRISB4

)

TABLE 8-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR(2

Osc Type	Resonator Freq.	Cap. Range C1	Cap. Range C2
LP	32 kHz(1)	15 pF	15 pF
XT	200 kHz 1 MHz 4 MHz	47-68 pF 15 pF 15 pF	47-68 pF 15 pF 15 pF
HS	20 MHz	15-47 pF	15-47 pF

Note 1: For V_{DD} > 4.5V, C1 = C2 ≈ 30 pF is recommended.

2: These values are for design guidance only. Rs may be required to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

8.3.3 EXTERNAL CRYSTAL OSCILLATOR CIRCUIT

Either a prepackaged oscillator or a simple oscillator circuit with TTL gates can be used as an external crystal oscillator circuit. Prepackaged oscillators provide a wide operating range and better stability. A well-designed crystal oscillator will provide good performance with TTL gates. Two types of crystal oscillator circuits can be used: one with parallel resonance, or one with series resonance.

Figure 8-3 shows implementation of a parallel resonant oscillator circuit. The circuit is designed to use the fundamental frequency of the crystal. The 74AS04 inverter performs the 180-degree phase shift that a parallel oscillator requires. The 4.7 kΩ resistor provides the negative feedback for stability. The 10 kΩ potentiometers bias the 74AS04 in the linear region. This circuit could be used for external oscillator designs.

FIGURE 8-3: EXTERNAL PARALLEL RESONANT CRYSTAL OSCILLATOR CIRCUIT

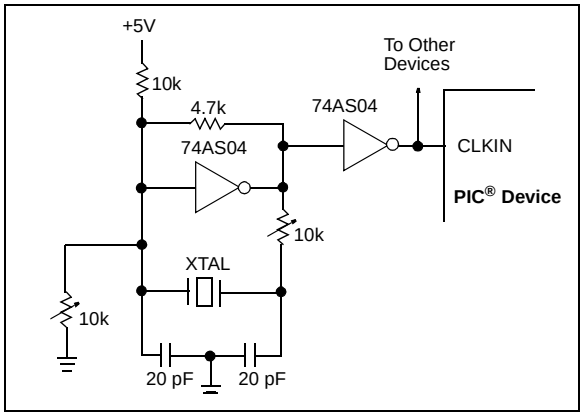
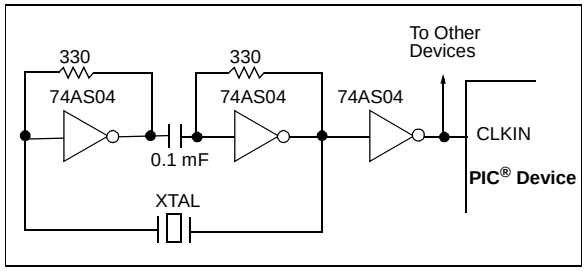


Figure 8-4 shows a series resonant oscillator circuit. This circuit is also designed to use the fundamental frequency of the crystal. The inverter performs a 180-degree phase shift in a series resonant oscillator circuit. The 330Ω resistors provide the negative feedback to bias the inverters in their linear region.

FIGURE 8-4: EXTERNAL SERIES RESONANT CRYSTAL OSCILLATOR CIRCUIT



8.3.4 EXTERNAL RC OSCILLATOR

For timing insensitive applications, the RC device option offers additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values, and the operating temperature. In addition to this, the oscillator frequency will vary from unit-to-unit due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to take into account variation due to tolerance of external R and C components used.

Figure 8-5 shows how the R/C combination is connected to the PIC16F527 device. For R_{EXT} values below 3.0 kΩ, the oscillator operation may become unstable, or stop completely. For very high R_{EXT} values (e.g., 1 MΩ), the oscillator becomes sensitive to noise, humidity and leakage. Thus, we recommend keeping R_{EXT} between 5.0 kΩ and 100 kΩ.

8.4 Reset

The device differentiates between various kinds of Reset:

- Power-on Reset (POR)
- Brown-out Reset (BOR)
- $\overline{\text{MCLR}}$ Reset during normal operation
- $\overline{\text{MCLR}}$ Reset during Sleep
- WDT Time-out Reset during normal operation
- WDT Time-out Reset during Sleep
- Wake-up from Sleep on pin change

Some registers are not reset in any way, they are unknown on POR/BOR and unchanged in any other Reset. Most other registers are reset to “Reset state” on Power-on Reset (POR)/Brown-out Reset (BOR), $\overline{\text{MCLR}}$, WDT or Wake-up on pin change Reset during normal operation. They are not affected by a WDT Reset during Sleep or $\overline{\text{MCLR}}$ Reset during Sleep, since these Resets are viewed as resumption of normal operation. The exceptions to this are the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits. They are set or cleared differently in different Reset situations. These bits are used in software to determine the nature of Reset. See Table 4-1 for a full description of Reset states of all registers.

TABLE 8-3: RESET CONDITION FOR SPECIAL REGISTERS

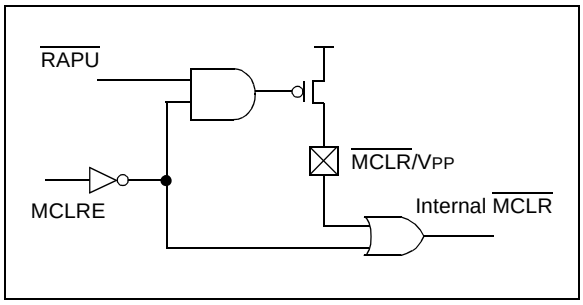
	STATUS Addr: 03h
Power-on Reset (POR) or Brown-out Reset (BOR)	0001 1xxx
$\overline{\text{MCLR}}$ Reset during normal operation	000u uuuu
$\overline{\text{MCLR}}$ Reset during Sleep	0001 0uuu
WDT Reset during Sleep	0000 0uuu
WDT Reset normal operation	0000 uuuu
Wake-up from Sleep on pin change	1001 0uuu
Wake-up from Sleep on comparator change	0101 0uuu

Legend: u = unchanged, x = unknown, – = unimplemented bit, read as ‘0’.

8.4.1 $\overline{\text{MCLR}}$ ENABLE

This Configuration bit, when set to a '1', enables the external $\overline{\text{MCLR}}$ Reset function. When cleared to '0', the $\overline{\text{MCLR}}$ function is tied to the internal VDD and the pin is assigned to be an input-only pin function. See Figure 8-6.

FIGURE 8-6: $\overline{\text{MCLR}}$ SELECT



8.5 Power-on Reset (POR)

The PIC16F527 device incorporates an on-chip Power-on Reset (POR) circuitry, which provides an internal chip Reset for most power-up situations.

The on-chip POR circuit holds the chip in Reset until VDD has reached a high enough level for proper operation. To take advantage of the internal POR, program the $\overline{\text{MCLR}}$/VPP pin as $\overline{\text{MCLR}}$ and tie through a resistor to VDD, or program the pin as an input pin. An internal weak pull-up resistor is implemented using a transistor (refer to Table 15-8 for the pull-up resistor ranges). This will eliminate external RC components usually needed to create a Power-on Reset. A maximum rise time for VDD is specified. See **Section 15.0 "Electrical Characteristics"** for details.

When the device starts normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature,...) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating parameters are met.

A simplified block diagram of the on-chip Power-on Reset circuit is shown in Figure 8-7.

The Power-on Reset circuit and the Device Reset Timer (see **Section 8.6 "Device Reset Timer (DRT)"**) circuit are closely related. On power-up, the Reset latch is set and the DRT is reset. The DRT timer begins counting once it detects $\overline{\text{MCLR}}$ to be high. After the time-out period, it will reset the Reset latch and thus end the on-chip Reset signal.

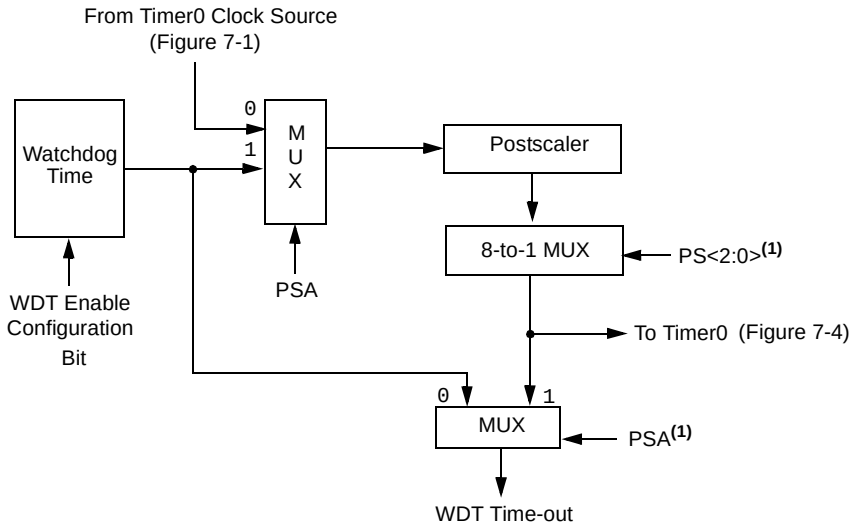
A power-up example where $\overline{\text{MCLR}}$ is held low is shown in Figure 8-8. VDD is allowed to rise and stabilize before bringing $\overline{\text{MCLR}}$ high. The chip will actually come out of Reset TDRT msec after $\overline{\text{MCLR}}$ goes high.

In Figure 8-9, the on-chip Power-on Reset feature is being used ($\overline{\text{MCLR}}$ and VDD are tied together or the pin is programmed to be an input pin). The VDD is stable before the start-up timer times out and there is no problem in getting a proper Reset. However, Figure 8-10 depicts a problem situation where VDD rises too slowly. The time between when the DRT senses that $\overline{\text{MCLR}}$ is high and when $\overline{\text{MCLR}}$ and VDD actually reach their full value, is too long. In this situation, when the start-up timer times out, VDD has not reached the VDD (min) value and the chip may not function correctly. For such situations, we recommend that external RC circuits be used to achieve longer POR delay times (see Figure 8-9).

Note:	When the device starts normal operation (exit the Reset condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in Reset until the operating conditions are met.

For additional information, refer to Application Notes *AN522, Power-Up Considerations* (DS00522) and *AN607, Power-up Trouble Shooting* (DS00607).

FIGURE 8-11: WATCHDOG TIMER BLOCK DIAGRAM



Note 1: PSA, PS<2:0> are bits in the OPTION register.

TABLE 8-5: REGISTERS ASSOCIATED WITH THE WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
OPTION	$\overline{\text{RAWU}}$	$\overline{\text{RAPU}}$	T0SC	T0SE	PSA	PS2	PS1	PS0	17

Legend: Shaded boxes = Not used by Watchdog Timer.

8.8 Time-out Sequence ($\overline{\text{TO}}$) and Power-down ($\overline{\text{PD}}$) Reset Status

The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits in the STATUS register can be tested to determine if a Reset condition has been caused by a power-up condition, a $\overline{\text{MCLR}}$ or Watchdog Timer (WDT) Reset.

TABLE 8-6: $\overline{\text{TO}}$/$\overline{\text{PD}}$ STATUS AFTER RESET

$\overline{\text{TO}}$	$\overline{\text{PD}}$	Reset Caused By
0	0	WDT wake-up from Sleep
0	u	WDT time-out (not from Sleep)
1	0	$\overline{\text{MCLR}}$ wake-up from Sleep
1	1	Power-up or Brown-out Reset
u	u	$\overline{\text{MCLR}}$ not during Sleep

Legend: u = unchanged

Note 1: The $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits maintain their status (u) until a Reset occurs. A low pulse on the $\overline{\text{MCLR}}$ input does not change the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ Status bits.

8.9 Brown-out Reset (BOR)

A brown-out is a condition where device power (V_{DD}) dips below its minimum value, but not to zero, and then recovers. The device should be reset in the event of a brown-out. The Brown-out Reset feature is enabled by the BOREN Configuration bit.

If V_{DD} falls below V_{BOR} for greater than parameter (T_{BOR}) (see Figure 8-12), the brown-out situation will reset the device. This will occur regardless of V_{DD} slew rate. A Reset is not insured to occur if V_{DD} falls below V_{BOR} for less than parameter (T_{BOR}).

Please see **Section 15.0 "Electrical Characteristics"** for the V_{BOR} specification and other parameters shown in Figure 8-12.

On any Reset (Power-on, Brown-out Reset, Watchdog Timer, etc.), the chip will remain in Reset until V_{DD} rises above V_{BOR} (see Figure 8-12). If enabled, the Device Reset Timer will now be invoked, and will keep the chip in Reset an additional 18 ms.

Note:	The Device Reset Timer is enabled by the DRTEN bit in the Configuration Word register.

If V_{DD} drops below V_{BOR} while the Device Reset Timer is running, the chip will go back into a Brown-out Reset and the Device Reset Timer will be re-initialized. Once V_{DD} rises above V_{BOR}, the Device Reset Timer will execute a 18 ms Reset.

FIGURE 8-12: BROWN-OUT RESET TIMING AND CHARACTERISTICS

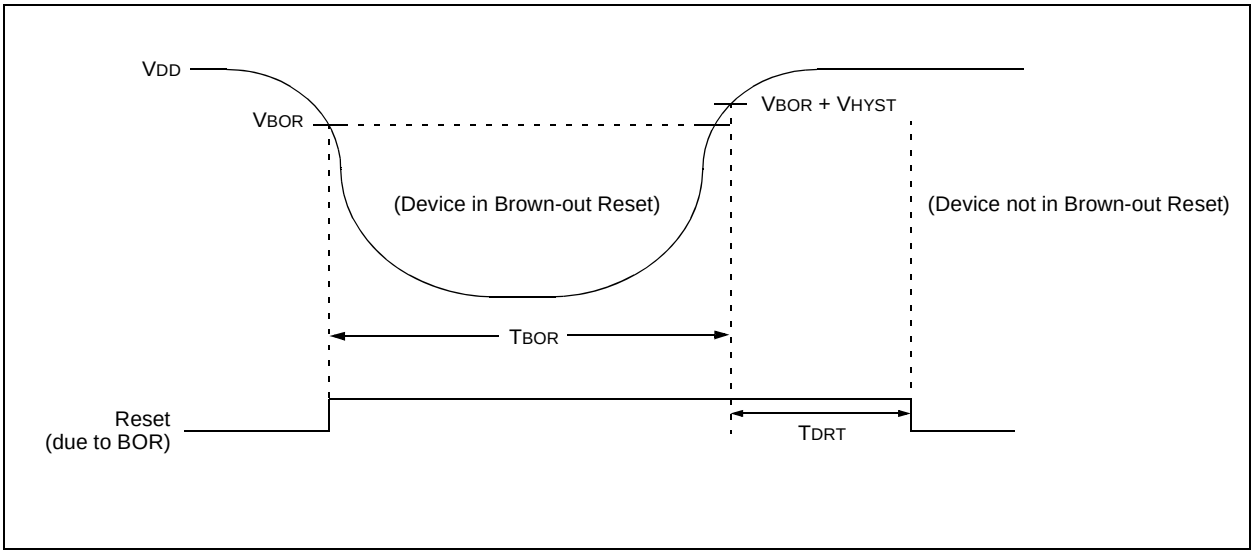
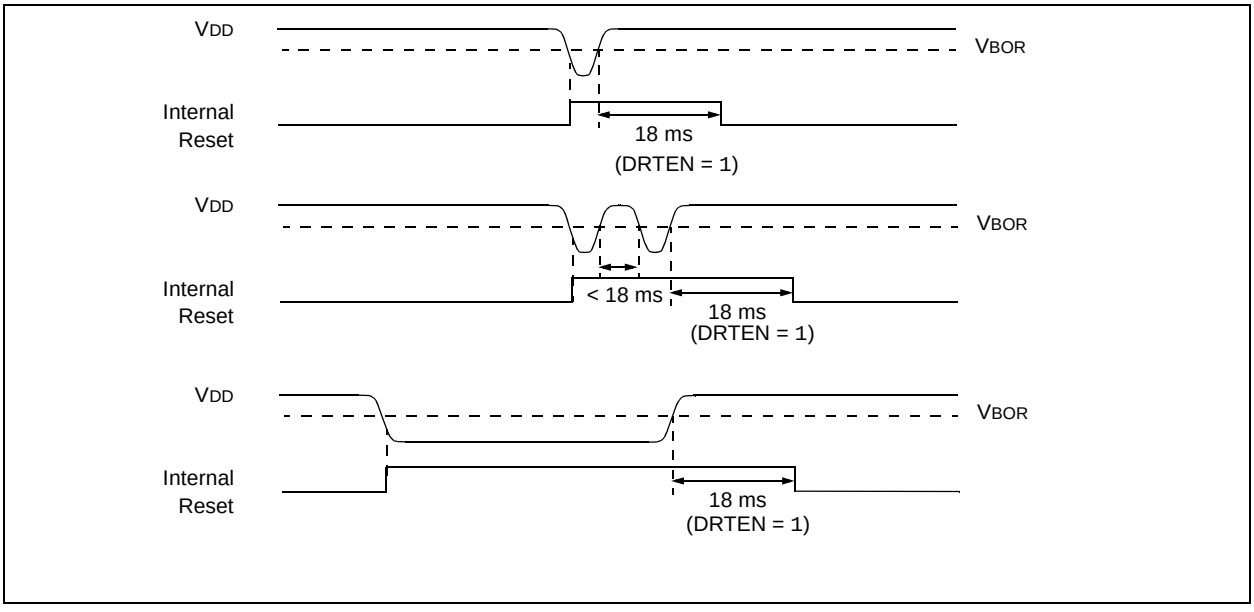


FIGURE 8-13: BROWN-OUT SITUATIONS



8.10 Power-down Mode (Sleep)

A device may be powered down (Sleep) and later powered up (wake-up from Sleep).

8.10.1 SLEEP

The Power-Down mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{TO}$ bit of the STATUS register is set, the $\overline{PD}$ bit of the STATUS register is cleared and the oscillator driver is turned off. The I/O ports maintain the status they had before the SLEEP instruction was executed (driving high, driving low or high-impedance).

Note:	A Reset generated by a WDT time-out does not drive the $\overline{MCLR}$ pin low.

For lowest current consumption while powered down, the T0CKI input should be at V_{DD} or V_{SS} and the $\overline{MCLR}/V_{PP}$ pin must be at a logic high level if $\overline{MCLR}$ is enabled.

8.10.2 WAKE-UP FROM SLEEP

The device can wake-up from Sleep through one of the following events:

1. An external Reset input on RB3/$\overline{MCLR}/V_{PP}$ pin, when configured as $\overline{MCLR}$.
2. A Watchdog Timer Time-out Reset (if WDT was enabled).
3. From an interrupt source, see **Section 8.11 "Interrupts"** for more information.

On waking from Sleep, the processor will continue to execute the instruction immediately following the SLEEP instruction. If the WUR bit is also set, upon waking from Sleep, the device will reset. If the GIE bit is also set, upon waking from Sleep, the processor will branch to the interrupt vector. Please see **Section 8.11 "Interrupts"** for more information.

The $\overline{TO}$ and $\overline{PD}$ bits can be used to determine the cause of the device Reset. The $\overline{TO}$ bit is cleared if a WDT time-out occurred and subsequently caused a wake-up. The $\overline{PD}$ bit, which is set on power-up, is cleared when SLEEP is invoked.

.

Note:	**Caution:** Right before entering Sleep, read the input pins. When in Sleep, wake-up occurs when the values at the pins change from the state they were in at the last reading. If a wake-up on change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately even if no pins change while in Sleep mode.

The WDT is cleared when the device wakes from Sleep, regardless of the wake-up source.

Note:	**Caution:** Right before entering Sleep, read the comparator Configuration register(s) CM1CON0 and CM2CON0. When in Sleep, wake-up occurs when the comparator output bit C1OUT and C2OUT change from the state they were in at the last reading. If a wake-up on comparator change occurs and the pins are not read before re-entering Sleep, a wake-up will occur immediately, even if no pins change while in Sleep mode.

8.14 Register Definitions — Interrupt Control

REGISTER 8-2: INTCON0 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
ADIF	CWIF	T0IF	RAIF	—	—	—	GIE
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADIF:** A/D Converter Interrupt Flag bit
- 1 = A/D conversion complete (must be cleared by software)
- 0 = A/D conversion has not completed or has not been started

bit 6 **CWIF:** Comparator 1 or 2 Interrupt Flag bit
- 1 = Comparator interrupt-on-change has occurred**(1)**
- 0 = No change in Comparator 1 or 2 output

bit 5 **T0IF:** Timer0 Overflow Interrupt Flag bit
- 1 = TMR0 register has overflowed (must be cleared by software)
- 0 = TMR0 register did not overflow

bit 4 **RAIF:** Port A Interrupt-on-change Flag bit
- 1 = Wake-up or interrupt has occurred (cleared in software)**(2)**
- 0 = Wake-up or interrupt has not occurred

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **GIE:** Global Interrupt Enable bit
- 1 = Interrupt sets PC to address 0x004 (Vector to ISR)
- 0 = Interrupt causes wake-up and inline code execution

Note 1: This bit only functions when the $\overline{C1WU}$ or $\overline{C2WU}$ bits are cleared (see Register 10-1 and Register 10-2).
2: The $\overline{RAWU}$ bit of the OPTION register must be cleared to enable this function (see Register 4-2).

REGISTER 8-3: INTCON1 REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	U-0	U-0	R/W-0
ADIE	CWIE	T0IE	RAIE	—	—	—	WUR
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **ADIE:** A/D Converter (ADC) Interrupt Enable bit
- 1 = Enables the ADC interrupt
- 0 = Disables the ADC interrupt

bit 6 **CWIE:** Comparator 1 and 2 Interrupt Enable bit
- 1 = Enables the Comparator 1 and 2 Interrupt
- 0 = Disables the Comparator 1 and 2 Interrupt

bit 5 **T0IE:** Timer0 Overflow Interrupt Enable bit
- 1 = Enables the Timer0 interrupt
- 0 = Disables the Timer0 interrupt

bit 4 **RAIE:** Port A on Pin Change Interrupt Enable bit
- 1 = Interrupt-on-change pin enabled
- 0 = Interrupt-on-change pin disabled

bit 3-1 **Unimplemented:** Read as '0'

bit 0 **WUR:** Wake-up Reset Enable bit
- 1 = Interrupt source causes device Reset on wake-up
- 0 = Interrupt source wakes up device from Sleep (Vector to ISR or inline execution)

11.0 COMPARATOR VOLTAGE REFERENCE MODULE

The Comparator Voltage Reference module also allows the selection of an internally generated voltage reference for one of the C2 comparator inputs. The VRCON register (see Register 11-1) controls the voltage reference module shown in Figure 11-1.

11.1 Configuring The Voltage Reference

The voltage reference can output 32 voltage levels; 16 in a high range and 16 in a low range.

Equation 11-1 determines the output voltages:

EQUATION 11-1:

VRR = 1 (low range):

$$CV_{REF} = (VR<3:0>/24) \times V_{DD}$$

VRR = 0 (high range):

$$CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

11.2 Voltage Reference Accuracy

The full range of V_{SS} to V_{DD} cannot be realized due to construction of the module. The transistors on the top and bottom of the resistor ladder network (see Figure 11-1) keep CV_{REF} from approaching V_{SS} or V_{DD}. The exception is when the module is disabled by clearing the VREN bit of the VRCON register. When disabled, the reference voltage is V_{SS} when VR<3:0> is '0000' and the VRR bit of the VRCON register is set. This allows the comparator to detect a zero crossing and not consume the CV_{REF} module current.

The voltage reference is V_{DD} derived and, therefore, the CV_{REF} output changes with fluctuations in V_{DD}. The tested absolute accuracy of the comparator voltage reference can be found in **Section 15.0 "Electrical Characteristics"**.

REGISTER 11-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **VREN:** CV_{REF} Enable bit
1 = CV_{REF} is powered on
0 = CV_{REF} is powered down, no current is drawn

bit 6 **VROE:** CV_{REF} Output Enable bit(1)
1 = CV_{REF} output is enabled
0 = CV_{REF} output is disabled

bit 5 **VRR:** CV_{REF} Range Selection bit
1 = Low range
0 = High range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR<3:0>** CV_{REF} Value Selection bits
When V_{RR} = 1: CV_{REF}= (VR<3:0>/24)*V_{DD}
When V_{RR} = 0: CV_{REF}= V_{DD}/4+(VR<3:0>/32)*V_{DD}

Note 1: When this bit is set, the TRIS for the CV_{REF} pin is overridden and the analog voltage is placed on the CV_{REF} pin.

FIGURE 11-1: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM

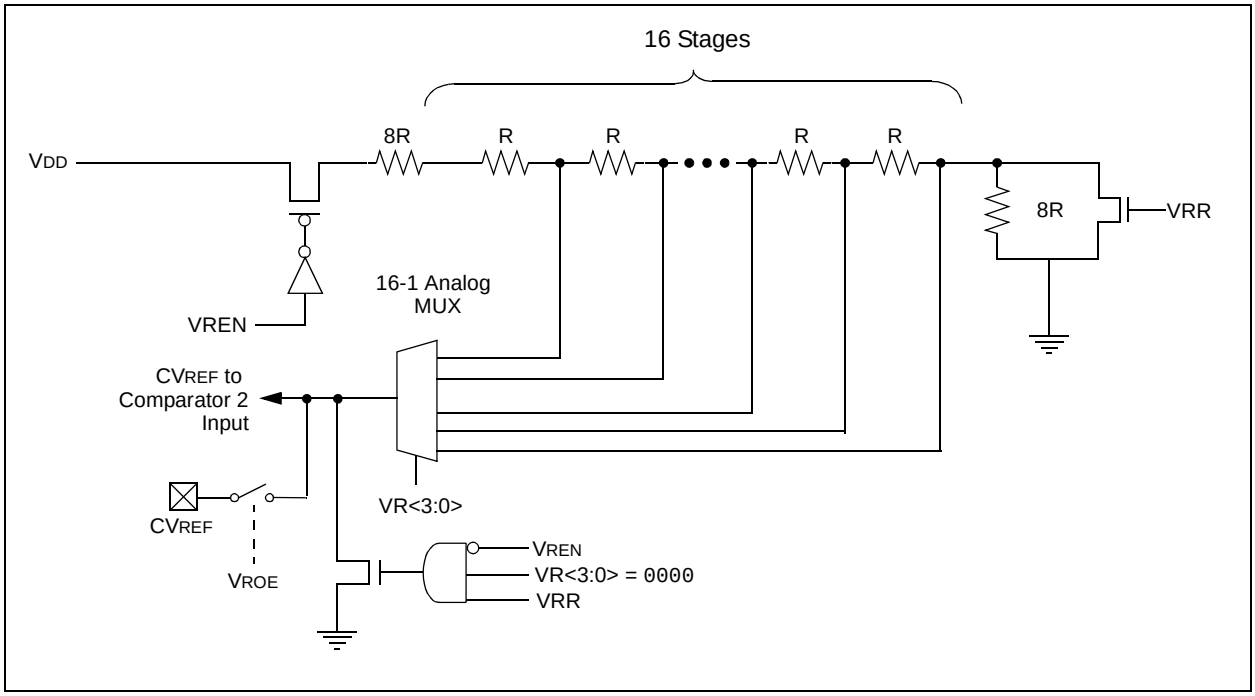


TABLE 11-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on page
VRCON	VREN	VROE	VRR	—	VR3	VR2	VR1	VR0	64
CM1CON0	C1OUT	$\overline{\text{C1OUTEN}}$	C1POL	$\overline{\text{C1T0CS}}$	C1ON	C1NREF	C1PREF	$\overline{\text{C1WU}}$	62
CM2CON0	C2OUT	$\overline{\text{C2OUTEN}}$	C2POL	$\overline{\text{C2PREF2}}$	C2ON	C2NREF	C2PREF1	$\overline{\text{C2WU}}$	63

Legend: x = unknown, u = unchanged, – = unimplemented, read as '0', q = value depends on condition.

13.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

For **byte-oriented** instructions, ‘f’ represents a file register designator and ‘d’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If ‘d’ is ‘0’, the result is placed in the W register. If ‘d’ is ‘1’, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘b’ represents a bit field designator which selects the number of the bit affected by the operation, while ‘f’ represents the number of the file in which the bit is located.

For **literal and control** operations, ‘k’ represents an 8 or 9-bit constant or literal value.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don’t care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register ‘f’) Default is d = 1
label	Label name
TOS	Top-of-Stack
PC	Program Counter
WDT	Watchdog Timer counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
Æ	Assigned to
< >	Register bit field
Œ	In the set of
italics	User defined term (font is courier)

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 μs.

Figure 13-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where ‘h’ signifies a hexadecimal digit.

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

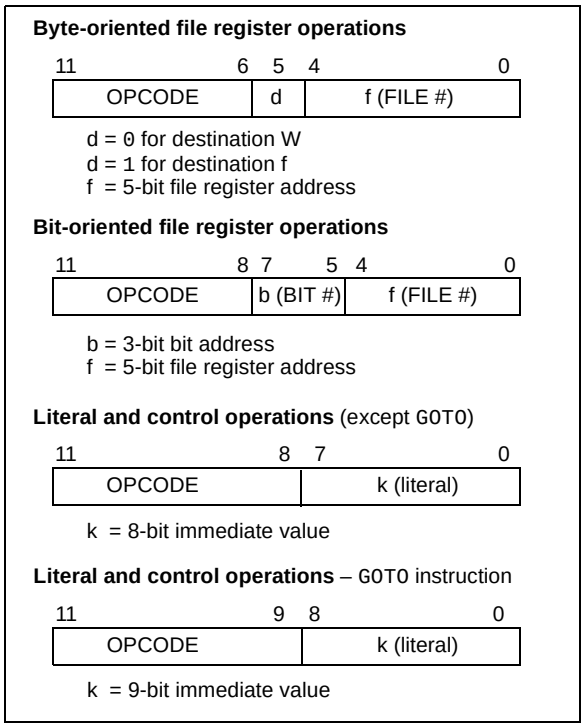


TABLE 15-1: DC CHARACTERISTICS: PIC16F527 (INDUSTRIAL, EXTENDED) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
		Capacitive Loading Specs on Output Pins					
D100	COSC2	OSC2 pin	—	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1.
D101	CIO	All I/O pins and OSC2	—	—	50	pF	
		Flash Data Memory					
D120	ED	Byte endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for read/write	VMIN	—	5.5	V	

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

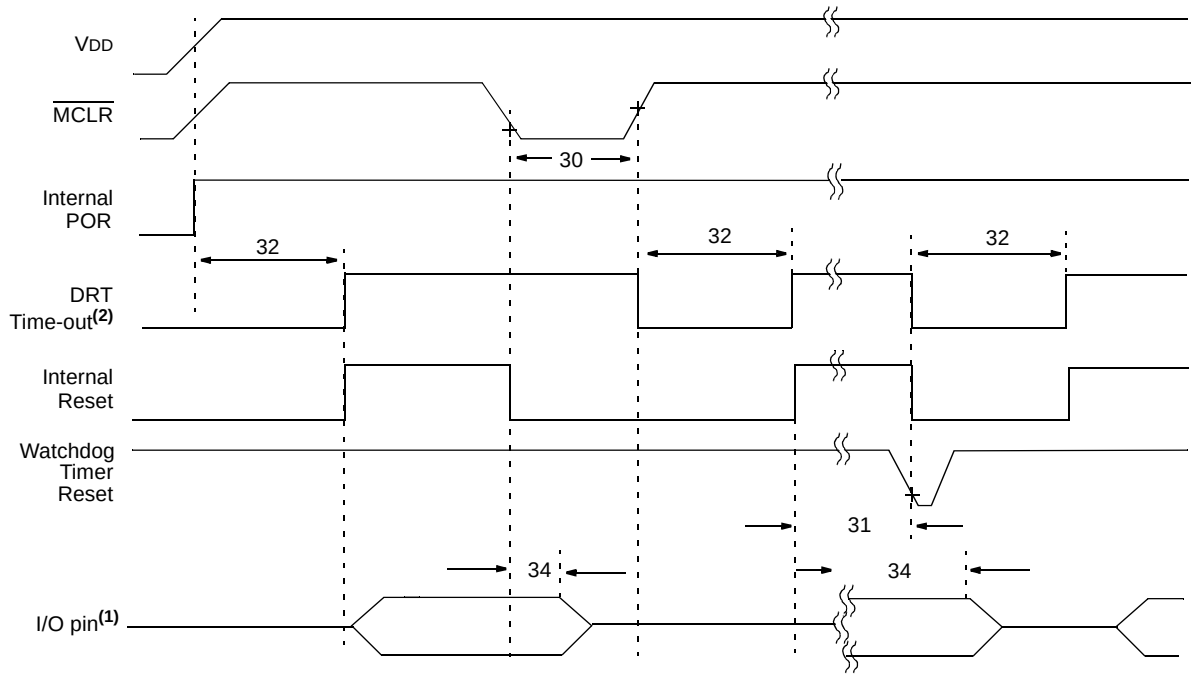
Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F527 be driven with external clock in RC mode.

2: The leakage current on the $\overline{\text{MCLR}}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: This spec applies to all weak pull-up devices, including the weak pull-up found on $\overline{\text{MCLR}}$.

FIGURE 15-6: RESET, WATCHDOG TIMER AND DEVICE RESET TIMER TIMING



Note 1: I/O pins must be taken out of High-Impedance mode by enabling the output drivers in software.
2: Runs in $\overline{MCLR}$ or WDT Reset only in XT, LP and HS modes.

FIGURE 15-7: BROWN-OUT RESET TIMING AND CHARACTERISTICS

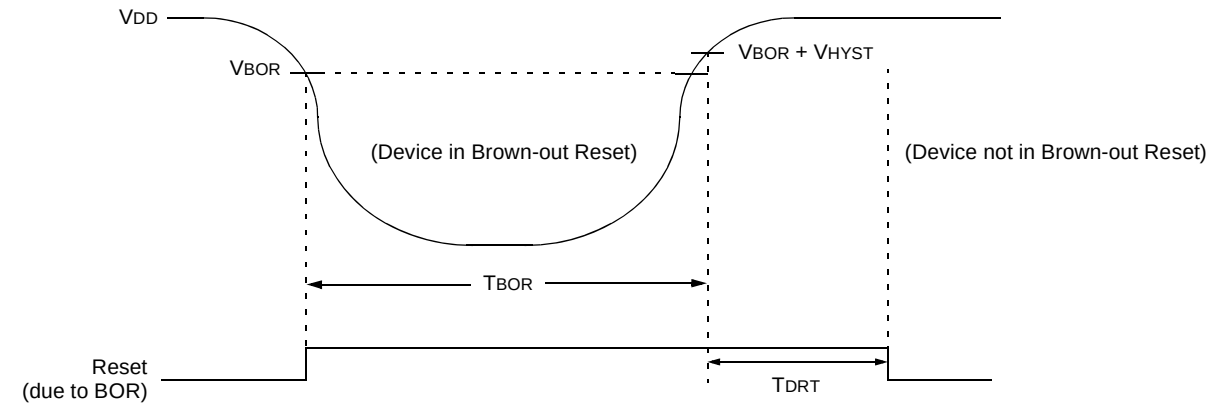


FIGURE 16-2: IDD TYPICAL, XT AND EXTRC OSCILLATOR

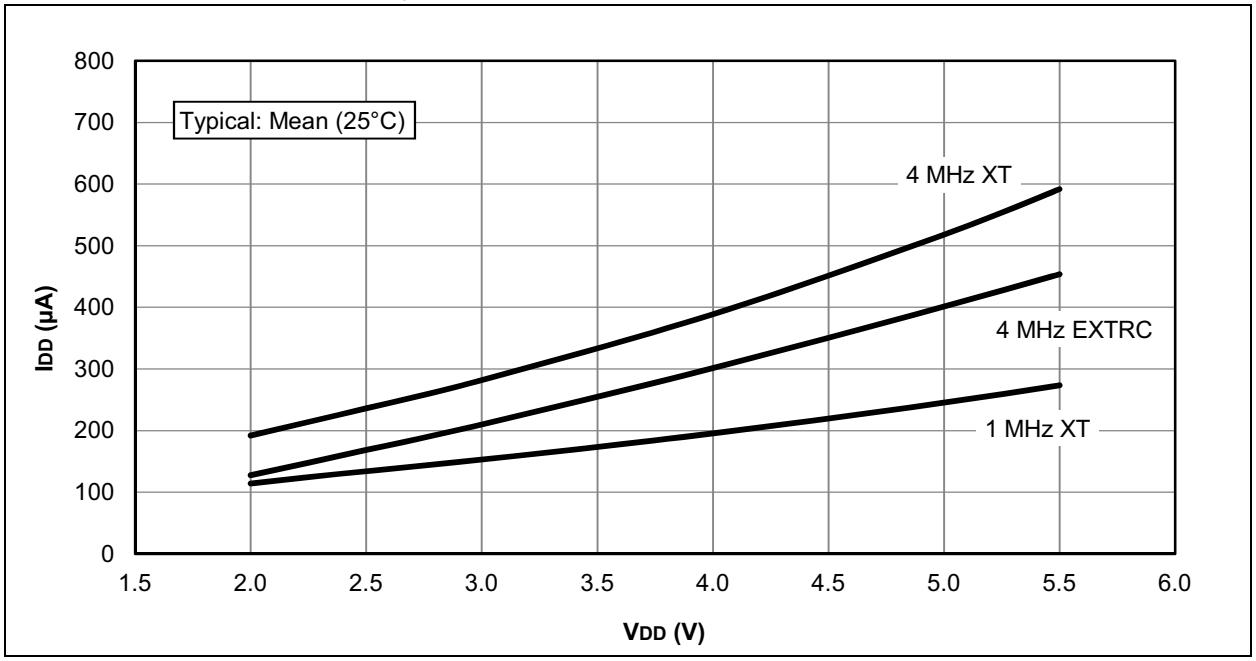


FIGURE 16-3: IDD MAXIMUM, XT AND EXTRC OSCILLATOR

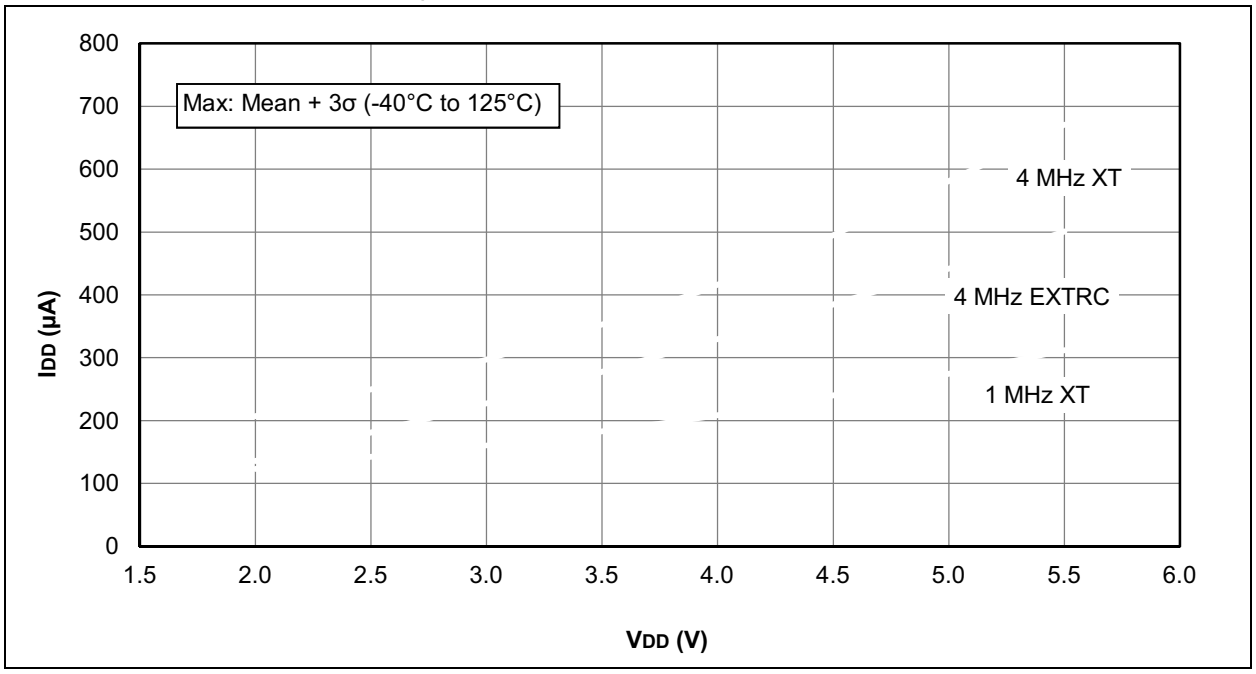


FIGURE 16-19: VOH vs. IOH OVER TEMPERATURE, VDD = 3.0 V

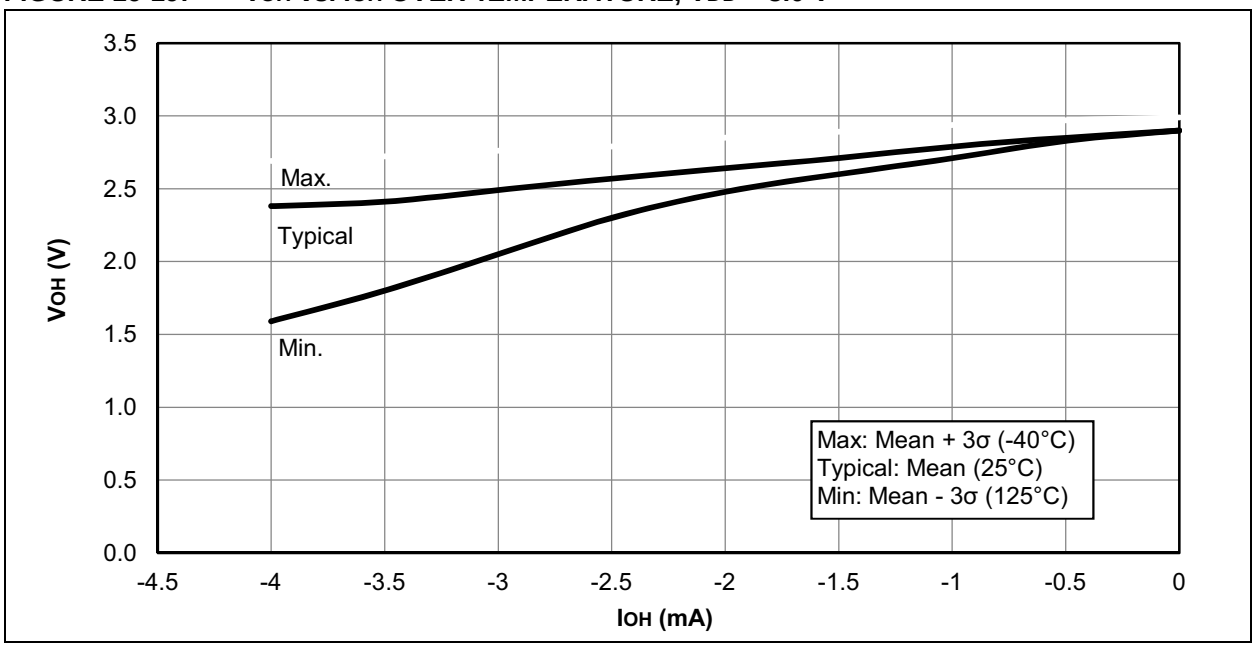
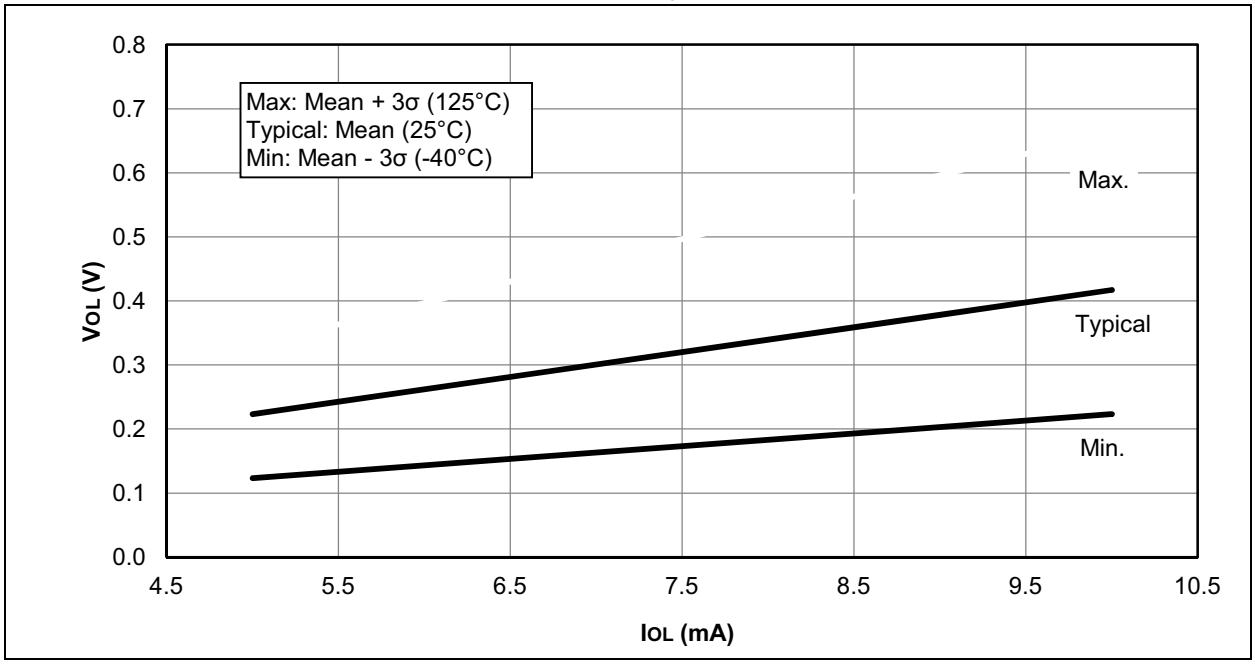
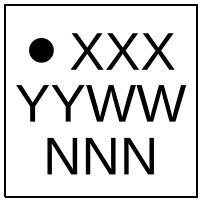


FIGURE 16-20: VOL vs. IOL OVER TEMPERATURE, VDD = 3.0V



Package Marking Information (Continued)

20-Lead UQFN (3x3x0.5 mm)



Example

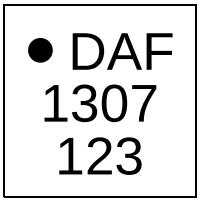
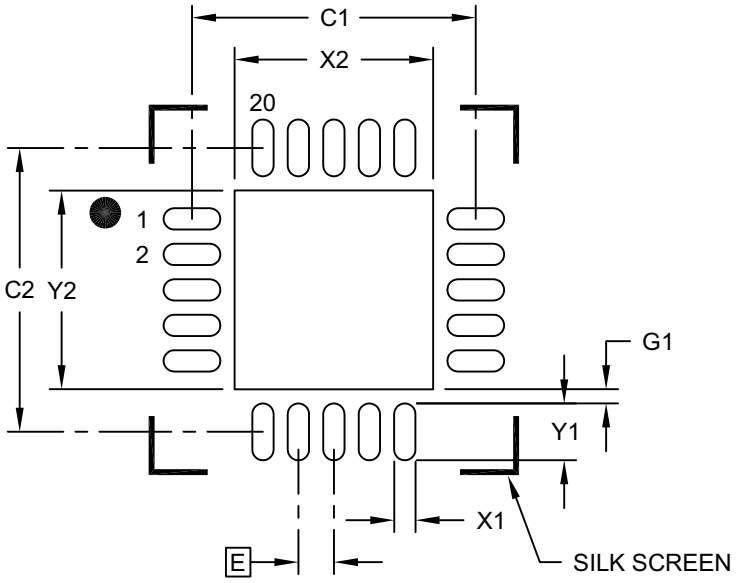


TABLE 17-1: 20-LEAD 3x3x0.5 UQFN (JP) TOP MARKING

Part Number	Marking
PIC16F527T-E/JP	DAF
PIC16F527T-I/JP	DAE

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (GZ) - 4x4x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.50 BSC		
Optional Center Pad Width	X2			2.80
Optional Center Pad Length	Y2			2.80
Contact Pad Spacing	C1		4.00	
Contact Pad Spacing	C2		4.00	
Contact Pad Width (X20)	X1			0.30
Contact Pad Length (X20)	Y1			0.80
Contact Pad to Center Pad (X20)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2255A