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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	20MHz
Connectivity	-
Peripherals	Brown-out Detect/Reset, POR, WDT
Number of I/O	17
Program Memory Size	1.5KB (1K x 12)
Program Memory Type	FLASH
EEPROM Size	64 x 8
RAM Size	68 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 8x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	20-UFQFN Exposed Pad
Supplier Device Package	20-UQFN (3x3)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f527t-i-jp

1.0 GENERAL DESCRIPTION

The PIC16F527 device from Microchip Technology is a low-cost, high-performance, 8-bit, fully-static, Flash-based CMOS microcontroller. It employs a RISC architecture with only 36 single-word/single-cycle instructions. All instructions are single cycle except for program branches, which take two cycles. The PIC16F527 device delivers performance an order of magnitude higher than its competitors in the same price category. The 12-bit wide instructions are highly symmetrical, resulting in a typical 2:1 code compression over other 8-bit microcontrollers in its class. The easy-to-use and easy to remember instruction set reduces development time significantly.

The PIC16F527 product is equipped with special features that reduce system cost and power requirements. The Power-on Reset (POR) and Device Reset Timer (DRT) eliminate the need for external Reset circuitry. There are several oscillator configurations to choose from, including INTRC Internal Oscillator mode and the power-saving LP (Low-Power) Oscillator mode. Power-Saving Sleep mode, Watchdog Timer and code protection features improve system cost, power and reliability.

The PIC16F527 device is available in the cost-effective Flash programmable version, which is suitable for production in any volume. The customer can take full advantage of Microchip's price leadership in Flash programmable microcontrollers, while benefiting from the Flash programmable flexibility.

The PIC16F527 product is supported by a full-featured macro assembler, a software simulator, an in-circuit emulator, a 'C' compiler, a low-cost development programmer and a full-featured programmer. All the tools are supported on IBM® PC and compatible machines.

1.1 Applications

The PIC16F527 device fits in applications ranging from personal care appliances and security systems to low-power remote transmitters/receivers. The Flash technology makes customizing application programs (transmitter codes, appliance settings, receiver frequencies, etc.) extremely fast and convenient. The small footprint packages, for through hole or surface mounting, make these microcontrollers perfect for applications with space limitations. Low cost, low power, high performance, ease of use and I/O flexibility make the PIC16F527 device very versatile, even in areas where no microcontroller use has been considered before (e.g., timer functions, logic and PLDs in larger systems and coprocessor applications).

TABLE 1-1: FEATURES AND MEMORY OF PIC16F527

		PIC16F527
Clock	Maximum Frequency of Operation (MHz)	20
Memory	Flash Program Memory	1024
	SRAM Data Memory (bytes)	68
	Flash Data Memory (bytes)	64
Peripherals	Timer Module(s)	TMR0
	Wake-up from Sleep on Pin Change	Yes
Features	I/O Pins	17
	Input Pins	1
	Internal Pull-ups	Yes
	In-Circuit Serial Programming™	Yes
	Number of Instructions	36
	Packages	20-pin PDIP, SOIC, SSOP, QFN, UQFN
	Interrupts	Yes

TABLE 3-2: PIC16F527 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
RA0/AN0/C1IN+/ICSPDAT	RA0	TTL	CMOS	Bidirectional I/O pin. It can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPDAT	ST	CMOS	ICSP™ mode Schmitt Trigger.
	C1IN+	AN	—	Comparator 1 input.
	AN0	AN	—	ADC channel input.
RA1/AN1/C1IN-/CVREF/ ICSPCLK	RA1	TTL	CMOS	Bidirectional I/O pin. It can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	ICSPCLK	ST	—	ICSP™ mode Schmitt Trigger.
	C1IN-	AN	—	Comparator 1 input.
	CVREF	—	AN	Programmable Voltage Reference output.
	AN1	AN	—	ADC channel input.
RA2/AN2/C1OUT/T0CKI	RA2	TTL	CMOS	Bidirectional I/O port.
	C1OUT	—	CMOS	Comparator 1 output.
	AN2	AN	—	ADC channel input.
	T0CKI	ST	—	Timer0 Schmitt Trigger input pin.
RA3/$\overline{\text{MCLR}}$/VPP	RA3	TTL	—	Standard TTL input with weak pull-up.
	$\overline{\text{MCLR}}$	ST	—	Master Clear (Reset). When configured as $\overline{\text{MCLR}}$, this pin is an active-low Reset to the device. Voltage on $\overline{\text{MCLR}}$/VPP must not exceed VDD during normal device operation or the device will enter Programming mode. Weak pull-up is always on if configured as $\overline{\text{MCLR}}$.
	VPP	HV	—	Test mode high-voltage pin.
RA4/AN3/OSC2/CLKOUT	RA4	TTL	CMOS	Bidirectional I/O pin. It can be software programmed for internal weak pull-up and wake-up from Sleep on pin change.
	OSC2	—	XTAL	Oscillator crystal output. Connections to crystal or resonator in Crystal Oscillator mode (XT, HS and LP modes only, PORTB in other modes).
	CLKOUT	—	CMOS	EXTRC/INTRC CLKOUT pin (FOSC/4).
	AN3	AN	—	ADC channel input.
RA5/OSC1/CLKIN	RA5	TTL	CMOS	Bidirectional I/O port.
	OSC1	XTAL	—	XTAL oscillator input pin.
	CLKIN	ST	—	EXTRC Schmitt Trigger input.
RB4/OP2-	RB4	TTL	CMOS	Bidirectional I/O port.
	OP2-	AN	—	Op amp 2 inverting input.
RB5/OP2+	RB5	TTL	CMOS	Bidirectional I/O port.
	OP2+	AN	—	Op amp 2 non-inverting input.
RB6	RB6	TTL	CMOS	Bidirectional I/O port.
RB7	RB7	TTL	CMOS	Bidirectional I/O port.
RC0/AN4/C2IN+	RC0	ST	CMOS	Bidirectional I/O port.
	AN4	AN	—	ADC channel input.
	C2IN+	AN	—	Comparator 2 input.
RC1/AN5/C2IN-	RC1	ST	CMOS	Bidirectional I/O port.
	AN5	AN	—	ADC channel input.
	C2IN-	AN	—	Comparator 2 input.

Legend: I = Input, O = Output, I/O = Input/Output, P = Power, — = Not Used, TTL = TTL input, ST = Schmitt Trigger input, HV = High Voltage, AN = Analog Voltage

TABLE 4-1: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR/BOR	Value on all other Resets
Bank 2											
N/A	W(2)	Working Register (W)								xxxx xxxx	xxxx xxxx
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								1111 1111	1111 1111
N/A	BSR(2)	—	—	—	—	—	—	BSR1	BSR0	---- -000	---- -0uu
40h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
41h	TMR0	Timer0 module Register								xxxx xxxx	uuuu uuuu
42h	PCL(1)	Low-order eight bits of PC								1111 1111	1111 1111
43h	STATUS(2)	Reserved	Reserved	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	-001 1xxx	-00q qqqq
44h	FSR(2)	—	Indirect data memory address pointer							0xxx xxxx	0uuu uuuu
45h	OSCCAL	CAL6	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	1111 111-	uuuu uuu-
46h	PORTA	—	—	RA5	RA4	RA3	RA2	RA1	RA0	--xx xxxx	--uu uuuu
47h	PORTB	RB7	RB6	RB5	RB4	—	—	—	—	xxxx ----	uuuu ----
48h	PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
49h	ADCON0	ADCS1	ADCS0	CHS3	CHS2	CHS1	CHS0	GO/$\overline{DONE}$	ADON	1111 1100	1111 1100
4Ah	ADRES	ADC Conversion Result								xxxx xxxx	uuuu uuuu
4Bh	INTCON0	ADIF	CWIF	T0IF	RAIF	—	—	—	GIE	0000 ---0	0000 ---0
Bank 3											
N/A	W(2)	Working Register (W)								xxxx xxxx	xxxx xxxx
N/A	TRIS	I/O Control Registers (TRISA, TRISB, TRISC)								1111 1111	1111 1111
N/A	OPTION	Contains control bits to configure Timer0 and Timer0/WDT prescaler								1111 1111	1111 1111
N/A	BSR(2)	—	—	—	—	—	—	BSR1	BSR0	---- -000	---- -0uu
60h	INDF	Uses contents of FSR to address data memory (not a physical register)								xxxx xxxx	uuuu uuuu
61h	IW(3)	Interrupt Working Register. (Addressed also as W register when within ISR)								xxxx xxxx	xxxx xxxx
62h	PCL(1)	Low-order eight bits of PC								1111 1111	1111 1111
63h	STATUS(2)	Reserved	Reserved	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	-001 1xxx	-00q qqqq
64h	FSR(2)	—	Indirect data memory address pointer							0xxx xxxx	0uuu uuuu
65h	INTCON1	ADIE	CWIE	T0IE	RAIE	—	—	—	WUR	0000 ---0	0000 ---0
66h	ISTATUS(3)	Reserved	Reserved	PA0	$\overline{TO}$	$\overline{PD}$	Z	DC	C	-xxx xxxx	-00q qqqq
67h	IFSR(3)	—	Indirect data memory address pointer							0xxx xxxx	0uuu uuuu
68h	IBSR(3)	—	—	—	—	—	—	BSR1	BSR0	---- -0xx	---- -0uu
69h	OPACON	—	—	—	—	—	—	OPA2ON	OPA1ON	---- --00	---- --00
6Bh	INTCON0	ADIF	CWIF	T0IF	RAIF	—	—	—	GIE	0000 ---0	0000 ---0

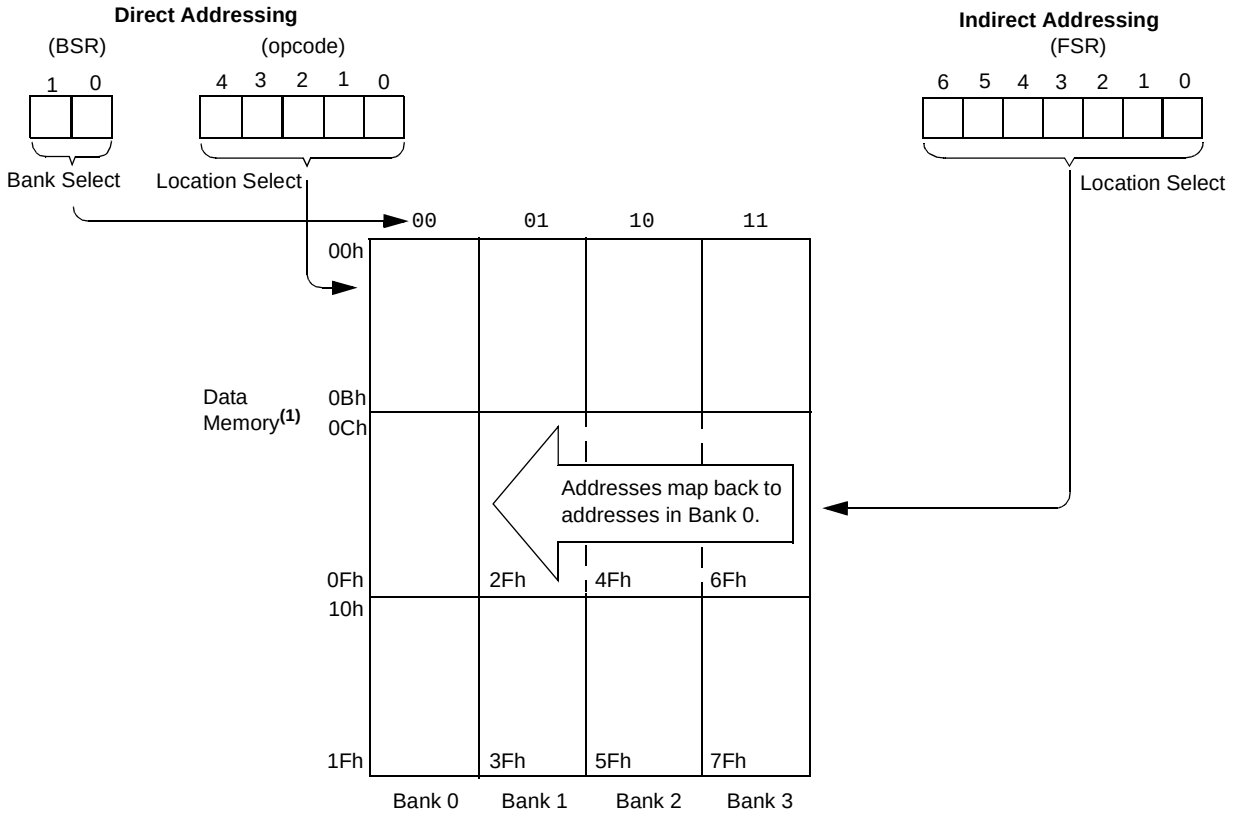
Legend: x = unknown, u = unchanged, – = unimplemented, read as '0' (if applicable), q = value depends on condition.
Shaded cells = unimplemented or unused

Note 1: The upper byte of the Program Counter is not directly accessible. See **Section 4.6 "Program Counter"** for an explanation of how to access these bits.

2: Registers are implemented as two physical registers. When executing from within an ISR, a secondary register is used at the same logical location. Both registers are persistent. See **Section 8.11 "Interrupts"**.

3: These registers show the contents of the registers in the other context: ISR or main line code. See **Section 8.11 "Interrupts"**.

FIGURE 4-4: DIRECT/INDIRECT ADDRESSING



Note 1: For register map detail see Figure 4-2.

6.0 I/O PORT

As with any other register, the I/O register(s) can be written and read under program control. However, read instructions (e.g., `MOVF PORTB,W`) always read the I/O pins independent of the pin's Input/Output modes. On Reset, all I/O ports are defined as input (inputs are at high-impedance) since the I/O control registers are all set.

6.1 PORTA

PORTA is a 6-bit I/O register. Only the low-order six bits are used (RA<5:0>). Bits 7 and 6 are unimplemented and read as '0's. Please note that RA3 is an input-only pin. The Configuration Word can set several I/Os to alternate functions. When acting as alternate functions, the pins will read as '0' during a port read. Pins RA0, RA1, RA3 and RA4 can be configured with weak pull-ups and also for wake-up on change. The wake-up on change and weak pull-up functions are not pin selectable. If RA3/$\overline{\text{MCLR}}$ is configured as $\overline{\text{MCLR}}$, weak pull-up is always on and wake-up on change for this pin is not enabled.

6.2 PORTB

PORTB is a 4-bit I/O register. Only the high-order four bits are used (RB<7:4>). Bits 0 through 3 are unimplemented and read as '0's.

6.3 PORTC

PORTC is an 8-bit I/O register.

6.4 TRIS Register

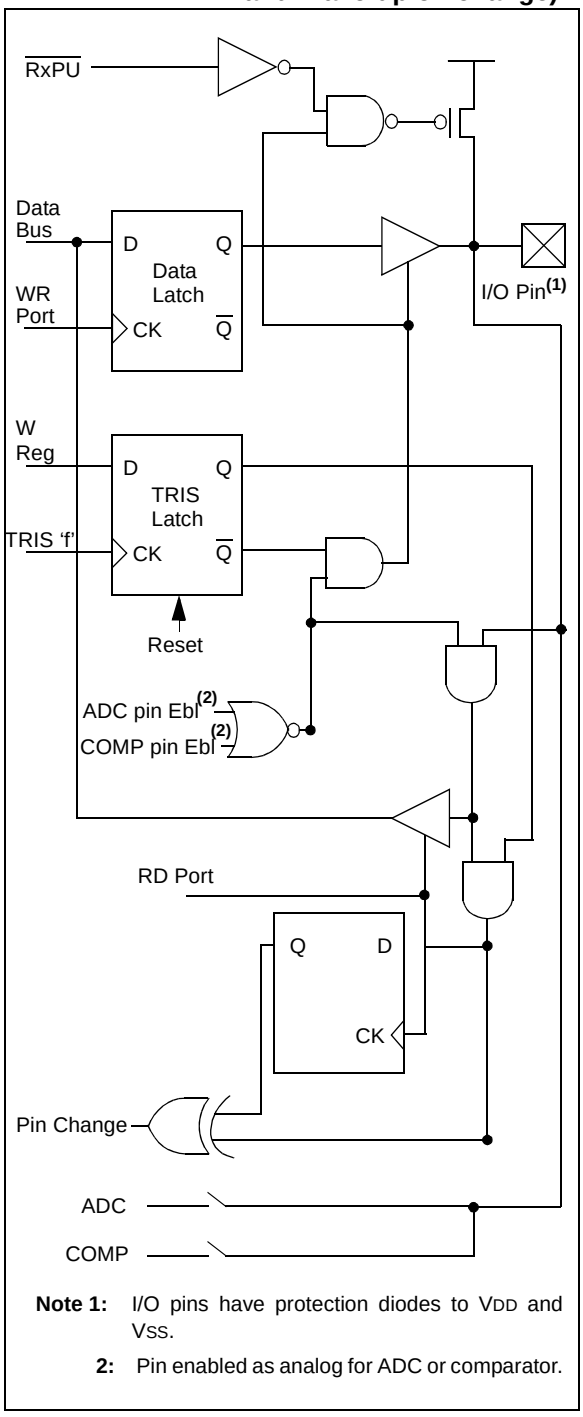
The Output Driver Control register is loaded with the contents of the W register by executing the `TRIS` instruction. A '1' from a TRIS register bit puts the corresponding output driver in a High-Impedance mode. A '0' puts the contents of the output data latch on the selected pins, enabling the output buffer. The exceptions are RA3, which is input-only and the T0CKI pin, which may be controlled by the OPTION register (see Register 4-2).

TRIS registers are "write-only". Active bits in these registers are set (output drivers disabled) upon Reset.

6.5 I/O Interfacing

The equivalent circuit for an I/O port pin is shown in Figure 6-1. All port pins, except the MCLR pin which is input-only, may be used for both input and output operations. For input operations, these ports are non-latching. Any input must be present until read by an input instruction (e.g., `MOVF PORTB, W`). The outputs are latched and remain unchanged until the output latch is rewritten. To use a port pin as output, the corresponding direction control bit in TRIS must be cleared (= `0`). For use as an input, the corresponding TRIS bit must be set. Any I/O pin (except MCLR) can be programmed individually as input or output.

FIGURE 6-1: BLOCK DIAGRAM OF I/O PIN (Example shown of RA2 with Weak Pull-up and Wake-up on change)



Note 1: I/O pins have protection diodes to VDD and VSS.

2: Pin enabled as analog for ADC or comparator.

6.6 Register Definitions — PORT Control

TABLE 6-1: PORTA: PORTA REGISTER

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	RA5	RA4	RA3	RA2	RA1	RA0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented**: Read as ‘0’

bit 5-0 **RA<5:0>**: PORTA I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

TABLE 6-2: PORTA PINS ORDER OF PRECEDENCE

Priority	RA5	RA4	RA3	RA2	RA1	RA0
1	OSC1	OSC2	RA3/$\overline{\text{MCLR}}$	AN2	CVREF	AN0
2	CLKIN	CLKOUT	—	C1OUT	AN1	C1IN+
3	TRISA5	AN3	—	T0CKI	C1IN-	TRISA0
4	—	TRISA4	—	TRISA2	TRISA1	—

TABLE 6-3: WEAK PULL-UP ENABLED PINS

Device	RA0 Weak Pull-up	RA1 Weak Pull-up	RA3 Weak Pull-up(1)	RA4 Weak Pull-up
PIC16F527	Yes	Yes	Yes	Yes

Note 1: When MCLRE = 1, the weak pull-up on $\overline{\text{MCLR}}$ is always enabled.

REGISTER 6-1: PORTB: PORTB REGISTER

R/W-x	R/W-x	R/W-x	R/W-x	U-0	U-0	U-0	U-0
RB7	RB6	RB5	RB4	—	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’	
-n = Value at POR	‘1’ = Bit is set	‘0’ = Bit is cleared	x = Bit is unknown

bit 7-4 **RB<7:4>**: PORTB I/O Pin bits
1 = Port pin is >VIH min.
0 = Port pin is <VIL max.

bit 3-0 **Unimplemented**: Read as ‘0’

TABLE 6-4: PORTB PINS ORDER OF PRECEDENCE

Priority	RB7	RB6	RB5	RB4
1	TRISB7	TRISB6	OP2+	OP2-
2	—	—	TRISB5	TRISB4

8.0 SPECIAL FEATURES OF THE CPU

What sets a microcontroller apart from other processors are special circuits that deal with the needs of real-time applications. The PIC16F527 microcontrollers have a host of such features intended to maximize system reliability, minimize cost through elimination of external components, provide power-saving operating modes and offer code protection. These features are:

- Oscillator Selection
- Reset:
  - Power-on Reset (POR)
  - Brown-out Reset (BOR)
  - Device Reset Timer (DRT)
  - Wake-up from Sleep on Pin Change
- Interrupts
- Automatic Context Saving
- Watchdog Timer (WDT)
- Sleep
- Code Protection
- ID Locations
- In-Circuit Serial Programming™
- Clock Out

The device has a Watchdog Timer, which can be shut off only through Configuration bit WDTE. The Watchdog Timer runs off of its own RC oscillator for added reliability.

There is also a Device Reset Timer (DRT), intended to keep the chip in Reset until the crystal oscillator is stable. The DRT can be enabled with the DRTEN Configuration bit. For the HS, XT or LP oscillator options, the 18 ms (nominal) delay is always provided by the Device Reset Timer and the DRTEN bit is ignored. When using the EC clock, INTRC or EXTRC oscillator options, there is a standard delay of 10 us on power-up, which can be extended to 18 ms with the use of the DRT timer. With the DRT timer on-chip, most applications require no additional external Reset circuitry.

The Sleep mode is designed to offer a very low current Power-Down mode. The user can wake-up from Sleep through a change on input pin or through a Watchdog Timer time-out. Several oscillator options are also made available to allow the part to fit the application, including an internal 4/8 MHz oscillator. The EXTRC oscillator option saves system cost while the LP crystal option saves power. A set of Configuration bits are used to select various options.

8.1 Configuration Bits

The PIC16F527 Configuration Words consist of 12 bits, although some bits may be unimplemented and read as '1'. Configuration bits can be programmed to select various device configurations (see Register 8-1).

Note:	For QTP and SQTP code applications, if the device is configured such that the Internal Oscillator is selected and the MCLRE fuse is cleared, it is possible for code to execute when memory is verified in ICSP™ mode. If customer code writes to Flash data memory, the potential exists for corruption of addresses 400h to 43Fh during code verification. In this configuration, Flash data memory should be erased in code prior to being written in code.

8.2 Register Definitions — Configuration Word

REGISTER 8-1: CONFIG: CONFIGURATION WORD REGISTER

U-1	U-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
—	—	DRTEN	BOREN	$\overline{\text{CPSW}}$	IOSCFS	MCLRE	$\overline{\text{CP}}$	WDTE	FOSC2	FOSC1	FOSC0
bit 11											bit 0

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '1'
'0' = Bit is cleared	'1' = Bit is set	-n = Value when blank or after Bulk Erase

bit 11-10 **Unimplemented:** Read as '1'

bit 9 **DRTEN:** Device Reset Timer Enable bit
- 1 = DRT Enabled (18 ms)
- 0 = DRT Disabled

bit 8 **BOREN:** Brown-out Reset Enable bit
- 1 = BOR Enabled
- 0 = BOR Disabled

bit 7 **$\overline{\text{CPSW}}$:** Code Protection bit – Self-Writable Memory
- 1 = Code protection off
- 0 = Code protection on

bit 6 **IOSCFS:** Internal Oscillator Frequency Select bit
- 1 = 8 MHz INTOSC speed
- 0 = 4 MHz INTOSC speed

bit 5 **MCLRE:** Master Clear Enable bit
- 1 = RA3/$\overline{\text{MCLR}}$ pin functions as $\overline{\text{MCLR}}$
- 0 = RA3/$\overline{\text{MCLR}}$ pin functions as RA3, $\overline{\text{MCLR}}$ tied internally to V_{DD}

bit 4 **$\overline{\text{CP}}$:** Code Protection bit – User Program Memory
- 1 = Code protection off
- 0 = Code protection on

bit 3 **WDTE:** Watchdog Timer Enable bit
- 1 = WDT enabled
- 0 = WDT disabled

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits
- 000 = LP oscillator and automatic 18 ms DRT (DRTEN fuse ignored)
- 001 = XT oscillator and automatic 18 ms DRT (DRTEN fuse ignored)
- 010 = HS oscillator and automatic 18 ms DRT (DRTEN fuse ignored)
- 011 = EC oscillator with RA4 function on RA4/OSC2/CLKOUT and 10 us start-up time(2,3)
- 100 = INTRC with RA4 function on RA4/OSC2/CLKOUT and 10 us start-up time(2,3)
- 101 = INTRC with CLKOUT function on RA4/OSC2/CLKOUT and 10 us start-up time(2,3)
- 110 = EXTRC with RA4 function on RA4/OSC2/CLKOUT and 10 us start-up time(2,3)
- 111 = EXTRC with CLKOUT function on RA4/OSC2/CLKOUT and 10 us start-up time(2,3)

Note 1: Refer to the "*PIC16F527 Memory Programming Specification*" (DS41640) to determine how to access the Configuration Word.

2: DRT length and start-up time are functions of the Clock mode selection. It is the responsibility of the application designer to ensure the use of either will result in acceptable operation. Refer to **Section 15.0 "Electrical Characteristics"** for V_{DD} rise time and stability requirements for this mode of operation.

3: The optional DRTEN fuse can be used to extend the start-up time to 18 ms.

8.3 Oscillator Configurations

8.3.1 OSCILLATOR TYPES

The PIC16F527 device can be operated in up to six different oscillator modes. The user can program up to three Configuration bits (FOSC<2:0>). To select one of these modes:

- LP: Low-Power Crystal
- XT: Crystal/Resonator
- HS: High-Speed Crystal/Resonator
- INTRC: Internal 4/8 MHz Oscillator
- EXTRC: External Resistor/Capacitor
- EC: External High-Speed Clock Input

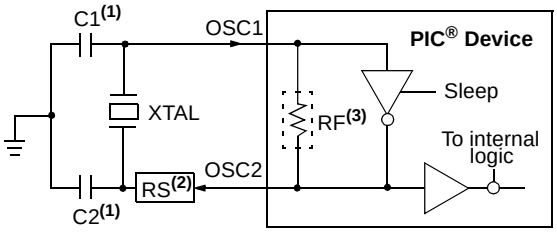
8.3.2 CRYSTAL OSCILLATOR/CERAMIC RESONATORS

In HS, XT or LP modes, a crystal or ceramic resonator is connected to the OSC1/CLKIN and OSC2/CLKOUT pins to establish oscillation (see Figure 8-1). The PIC16F527 oscillator designs require the use of a parallel cut crystal. Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications. When in HS, XT or LP modes, the device can have an external clock source drive the OSC1/CLKIN pin (see Figure 8-2). In this mode, the output drive levels on the OSC2 pin are very weak. If the part is used in this fashion, then this pin should be left open and unloaded. Also when using this mode, the external clock should observe the frequency limits for the Clock mode chosen (HS, XT or LP).

Note 1: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

2: The user should verify that the device oscillator starts and performs as expected. Adjusting the loading capacitor values and/or the Oscillator mode may be required.

FIGURE 8-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) (HS, XT OR LP OSC CONFIGURATION)

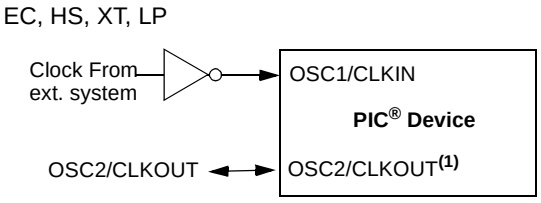


Note 1: See Capacitor Selection tables for recommended values of C1 and C2.

2: A series resistor (RS) may be required for AT strip cut crystals.

3: RF approx. value = 10 MΩ.

FIGURE 8-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT, LP OR EC OSC CONFIGURATION)



Note 1: Available in EC mode only.

TABLE 8-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Osc Type	Resonator Freq.	Cap. Range C1	Cap. Range C2
XT	4.0 MHz	30 pF	30 pF
HS	16 MHz	10-47 pF	10-47 pF

Note 1: These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

8.15 Program Verification/Code Protection

If the code protection bit has not been programmed, the on-chip program memory can be read out for verification purposes.

The first 64 locations and the last location (OSCCAL) can be read, regardless of the code protection bit setting.

8.16 ID Locations

Four memory locations are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution, but are readable and writable during Program/Verify.

Use only the lower four bits of the ID locations and always program the upper eight bits as '0's.

8.17 In-Circuit Serial Programming™

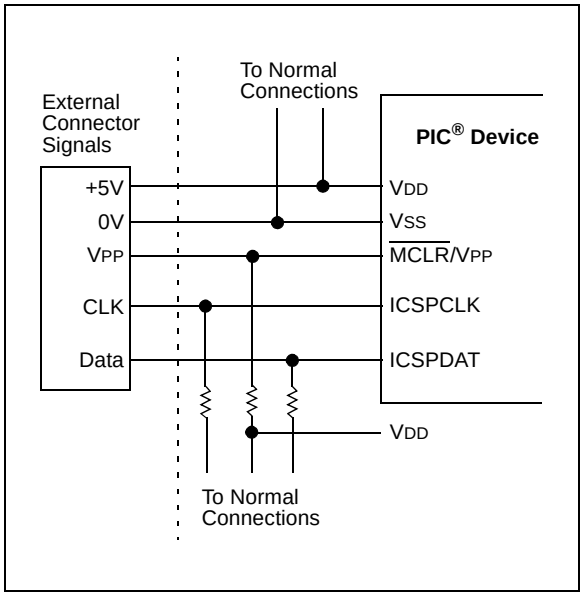
The PIC16F527 microcontroller can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware, or a custom firmware, to be programmed.

The devices are placed into a Program/Verify mode by holding the ICSPCLK and ICSPDAT pins low while raising the $\overline{MCLR}$ (V_{PP}) pin from V_{IL} to V_{IHH} (see programming specification). ICSPCLK becomes the programming clock and ICSPDAT becomes the programming data. Both ICSPCLK and ICSPDAT are Schmitt Trigger inputs in this mode.

After Reset, a 6-bit command is then supplied to the device. Depending on the command, 14 bits of program data are then supplied to or from the device, depending if the command was a load or a read. For complete details of serial programming, please refer to the PIC16F527 Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 8-14.

FIGURE 8-14: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



9.0 ANALOG-TO-DIGITAL (A/D) CONVERTER

The A/D Converter allows conversion of an analog signal into an 8-bit digital signal.

9.1 Clock Divisors

The ADC has four clock source settings ADCS<1:0>. There are three divisor values 16, 8 and 4. The fourth setting is INTOSC with a divisor of four. These settings will allow a proper conversion when using an external oscillator at speeds from 20 MHz to 350 kHz. Using an external oscillator at a frequency below 350 kHz requires the ADC oscillator setting to be INTOSC/4 (ADCS<1:0> = 11) for valid ADC results.

The ADC requires 13 TAD periods to complete a conversion. The divisor values do not affect the number of TAD periods required to perform a conversion. The divisor values determine the length of the TAD period.

When the ADCS<1:0> bits are changed while an ADC conversion is in process, the new ADC clock source will not be selected until the next conversion is started. This clock source selection will be lost when the device enters Sleep.

Note:	The ADC clock is derived from the instruction clock. The ADCS divisors are then applied to create the ADC clock

9.1.1 VOLTAGE REFERENCE

There is no external voltage reference for the ADC. The ADC reference voltage will always be VDD.

9.1.2 ANALOG MODE SELECTION

The ANS<7:0> bits are used to configure pins for analog input. Upon any Reset, ANS<7:0> defaults to FF. This configures the affected pins as analog inputs. Pins configured as analog inputs are not available for digital output. Users should not change the ANS bits while a conversion is in process. ANS bits are active regardless of the condition of ADON.

9.1.3 ADC CHANNEL SELECTION

The CHS bits are used to select the analog channel to be sampled by the ADC. The CHS<3:0> bits can be changed at any time without adversely effecting a conversion. To acquire an external analog signal, the CHS<3:0> selection must match one of the pin(s) selected by the ANS<7:0> bits. When the ADC is on (ADON = 1) and a channel is selected that is also being used by the comparator, then both the comparator and the ADC will see the analog voltage on the pin.

Note:	It is the user's responsibility to ensure that the use of the ADC and op amp simultaneously on the same pin does not adversely affect the signal being monitored or adversely effect device operation.

When the CHS<3:0> bits are changed during an ADC conversion, the new channel will not be selected until the current conversion is completed. This allows the current conversion to complete with valid results. All channel selection information will be lost when the device enters Sleep.

9.1.4 THE GO/$\overline{\text{DONE}}$ BIT

The GO/$\overline{\text{DONE}}$ bit is used to determine the status of a conversion, to start a conversion and to manually halt a conversion in process. Setting the GO/$\overline{\text{DONE}}$ bit starts a conversion. When the conversion is complete, the ADC module clears the GO/$\overline{\text{DONE}}$ bit and sets the ADIF bit in the INTCON0 register.

A conversion can be terminated by manually clearing the GO/$\overline{\text{DONE}}$ bit while a conversion is in process. Manual termination of a conversion may result in a partially converted result in ADRES.

The GO/$\overline{\text{DONE}}$ bit is cleared when the device enters Sleep, stopping the current conversion. The ADC does not have a dedicated oscillator, it runs off of the instruction clock. Therefore, no conversion can occur in Sleep.

The GO/$\overline{\text{DONE}}$ bit cannot be set when ADON is clear.

9.1.5 A/D ACQUISITION REQUIREMENTS

For the ADC to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The Analog Input model is shown in Figure 9-1. The source impedance (RS) and the internal sampling switch (RSS) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (RSS) impedance varies over the device voltage (VDD), see Figure 9-1. **The maximum recommended impedance for analog sources is 10 kΩ.** As the source impedance is decreased, the acquisition time may be decreased. After the analog input channel is selected (or changed), an A/D acquisition must be done before the conversion can be started. To calculate the minimum acquisition time, Equation 9-1 may be used. This equation assumes that 1/2 LSb error is used (256 steps for the ADC). The 1/2 LSb error is the maximum error allowed for the ADC to meet its specified resolution.

REGISTER 9-2: ADRES: A/D CONVERSION RESULTS REGISTER

R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X	R/W-X
ADRES7	ADRES6	ADRES5	ADRES4	ADRES3	ADRES2	ADRES1	ADRES0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-0 **ADRES<7:0>**: ADC Result Register bits

EXAMPLE 9-1: PERFORMING AN ANALOG-TO-DIGITAL CONVERSION

```
;Sample code operates out of BANK0
       MOVLW 0xF1     ;configure A/D
       MOVWF ADCON0
       BSF ADCON0, 1  ;start conversion
loop0  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W  ;read result
       MOVWF result0  ;save result

       BSF ADCON0, 2  ;setup for read of
                      ;channel 1
       BSF ADCON0, 1  ;start conversion
loop1  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W  ;read result
       MOVWF result1  ;save result

       BSF ADCON0, 3  ;setup for read of
       BCF ADCON0, 2  ;channel 2
       BSF ADCON0, 1  ;start conversion
loop2  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W  ;read result
       MOVWF result2  ;save result
```

EXAMPLE 9-2: CHANNEL SELECTION CHANGE DURING CONVERSION

```
       MOVLW 0xF1     ;configure A/D
       MOVWF ADCON0
       BSF ADCON0, 1  ;start conversion
       BSF ADCON0, 2  ;setup for read of
                      ;channel 1
loop0  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop0
       MOVF ADRES, W  ;read result
       MOVWF result0  ;save result

       BSF ADCON0, 1  ;start conversion
       BSF ADCON0, 3  ;setup for read of
       BCF ADCON0, 2  ;channel 2
loop1  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop1
       MOVF ADRES, W  ;read result
       MOVWF result1  ;save result

       BSF ADCON0, 1  ;start conversion
loop2  BTFSC ADCON0, 1;wait for 'DONE'
       GOTO loop2
       MOVF ADRES, W  ;read result
       MOVWF result2  ;save result
       CLRF ADCON0    ;optional: returns
       ;pins to Digital mode and turns off
       ;the ADC module
```

11.0 COMPARATOR VOLTAGE REFERENCE MODULE

The Comparator Voltage Reference module also allows the selection of an internally generated voltage reference for one of the C2 comparator inputs. The VRCON register (see Register 11-1) controls the voltage reference module shown in Figure 11-1.

11.1 Configuring The Voltage Reference

The voltage reference can output 32 voltage levels; 16 in a high range and 16 in a low range.

Equation 11-1 determines the output voltages:

EQUATION 11-1:

VRR = 1 (low range):

$$CV_{REF} = (VR<3:0>/24) \times V_{DD}$$

VRR = 0 (high range):

$$CV_{REF} = (V_{DD}/4) + (VR<3:0> \times V_{DD}/32)$$

11.2 Voltage Reference Accuracy

The full range of VSS to VDD cannot be realized due to construction of the module. The transistors on the top and bottom of the resistor ladder network (see Figure 11-1) keep CVREF from approaching VSS or VDD. The exception is when the module is disabled by clearing the VREN bit of the VRCON register. When disabled, the reference voltage is VSS when VR<3:0> is '0000' and the VRR bit of the VRCON register is set. This allows the comparator to detect a zero crossing and not consume the CVREF module current.

The voltage reference is VDD derived and, therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the comparator voltage reference can be found in **Section 15.0 "Electrical Characteristics"**.

REGISTER 11-1: VRCON: VOLTAGE REFERENCE CONTROL REGISTER

R/W-0	R/W-0	R/W-1	U-0	R/W-0	R/W-0	R/W-0	R/W-0
VREN	VROE	VRR	—	VR3	VR2	VR1	VR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **VREN:** CVREF Enable bit
1 = CVREF is powered on
0 = CVREF is powered down, no current is drawn

bit 6 **VROE:** CVREF Output Enable bit(1)
1 = CVREF output is enabled
0 = CVREF output is disabled

bit 5 **VRR:** CVREF Range Selection bit
1 = Low range
0 = High range

bit 4 **Unimplemented:** Read as '0'

bit 3-0 **VR<3:0>** CVREF Value Selection bits
When VRR = 1: CVREF= (VR<3:0>/24)*VDD
When VRR = 0: CVREF= VDD/4+(VR<3:0>/32)*VDD

Note 1: When this bit is set, the TRIS for the CVREF pin is overridden and the analog voltage is placed on the CVREF pin.

13.0 INSTRUCTION SET SUMMARY

The PIC16 instruction set is highly orthogonal and is comprised of three basic categories.

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC16 instruction is a 12-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands** which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 13-1, while the various opcode fields are summarized in Table 13-1.

For **byte-oriented** instructions, 'f' represents a file register designator and 'd' represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, 'b' represents a bit field designator which selects the number of the bit affected by the operation, while 'f' represents the number of the file in which the bit is located.

For **literal and control** operations, 'k' represents an 8 or 9-bit constant or literal value.

TABLE 13-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
W	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0 (store result in W) d = 1 (store result in file register 'f') Default is d = 1
label	Label name
TOS	Top-of-Stack
PC	Program Counter
WDT	Watchdog Timer counter
$\overline{TO}$	Time-out bit
$\overline{PD}$	Power-down bit
dest	Destination, either the W register or the specified register file location
[ ]	Options
( )	Contents
Æ	Assigned to
< >	Register bit field
Œ	In the set of
italics	User defined term (font is courier)

All instructions are executed within a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of an instruction. In this case, the execution takes two instruction cycles. One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 µs. If a conditional test is true or the program counter is changed as a result of an instruction, the instruction execution time is 2 µs.

Figure 13-1 shows the three general formats that the instructions can have. All examples in the figure use the following format to represent a hexadecimal number:

0xhhh

where 'h' signifies a hexadecimal digit.

FIGURE 13-1: GENERAL FORMAT FOR INSTRUCTIONS

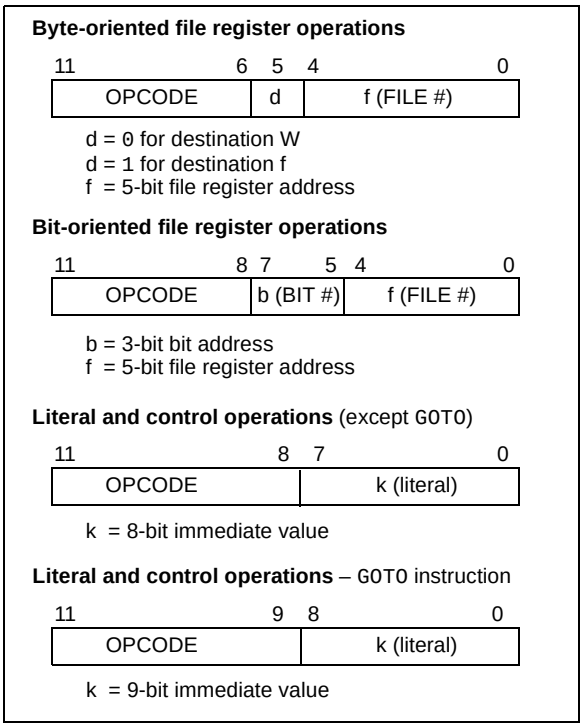


TABLE 15-1: DC CHARACTERISTICS: PIC16F527 (INDUSTRIAL, EXTENDED) (CONTINUED)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise specified) Operating temperature -40°C ≤ TA ≤ +85°C (industrial) -40°C ≤ TA ≤ +125°C (extended)				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.†**	**Max.**	**Units**	**Conditions**
	VOH	**Output High Voltage**					
D090		I/O ports/CLKOUT	VDD – 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V, -40°C to +85°C
D090A			VDD – 0.7	—	—	V	IOH = -2.5 mA, VDD = 4.5V, -40°C to +125°C
D092		OSC2	VDD – 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V, -40°C to +85°C
D092A			VDD – 0.7	—	—	V	IOH = -1.0 mA, VDD = 4.5V, -40°C to +125°C

† Data in “Typ” column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: In EXTRC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PIC16F527 be driven with external clock in RC mode.

2: The leakage current on the $\overline{MCLR}$ pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as coming out of the pin.

4: This spec applies to all weak pull-up devices, including the weak pull-up found on $\overline{MCLR}$.

TABLE 15-6: EXTERNAL CLOCK TIMING REQUIREMENTS

AC Characteristics			Standard Operating Conditions (unless otherwise specified) Operating Temperature -40°C ≤ TA ≤ +85°C (industrial), -40°C ≤ TA ≤ +125°C (extended) Operating voltage VDD range is described in **Section 15.1 "DC Characteristics: PIC16F527 (Industrial)"**.				
Param. No.	**Sym.**	**Characteristic**	**Min.**	**Typ.(1)**	**Max.**	**Units**	**Conditions**
1A	FOSC	External CLKIN Frequency(2)	DC	—	4	MHz	XT Oscillator
			DC	—	20	MHz	HS/EC Oscillator
			DC	—	200	kHz	LP Oscillator
		Oscillator Frequency(2)	DC	—	4	MHz	EXTRC Oscillator
			0.1	—	4	MHz	XT Oscillator
			4	—	20	MHz	HS/EC Oscillator
			DC	—	200	kHz	LP Oscillator
1	TOSC	External CLKIN Period(2)	250	—	—	ns	XT Oscillator
			50	—	—	ns	HS/EC Oscillator
			5	—	—	µs	LP Oscillator
		Oscillator Period(2)	250	—	—	ns	EXTRC Oscillator
			250	—	10,000	ns	XT Oscillator
			50	—	250	ns	HS/EC Oscillator
			5	—	—	µs	LP Oscillator
2	TCY	Instruction Cycle Time	200	4/FOSC	DC	ns	
3	TosL, TosH	Clock in (OSC1) Low or High Time	50*	—	—	ns	XT Oscillator
			2*	—	—	µs	LP Oscillator
			10*	—	—	ns	HS/EC Oscillator
4	TosR, TosF	Clock in (OSC1) Rise or Fall Time	—	—	25*	ns	XT Oscillator
			—	—	50*	ns	LP Oscillator
			—	—	15*	ns	HS/EC Oscillator

* These parameters are characterized but not tested.

Note 1: Data in the Typical ("Typ") column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

2: All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

FIGURE 16-4: IDD TYPICAL, EXTERNAL CLOCK MODE

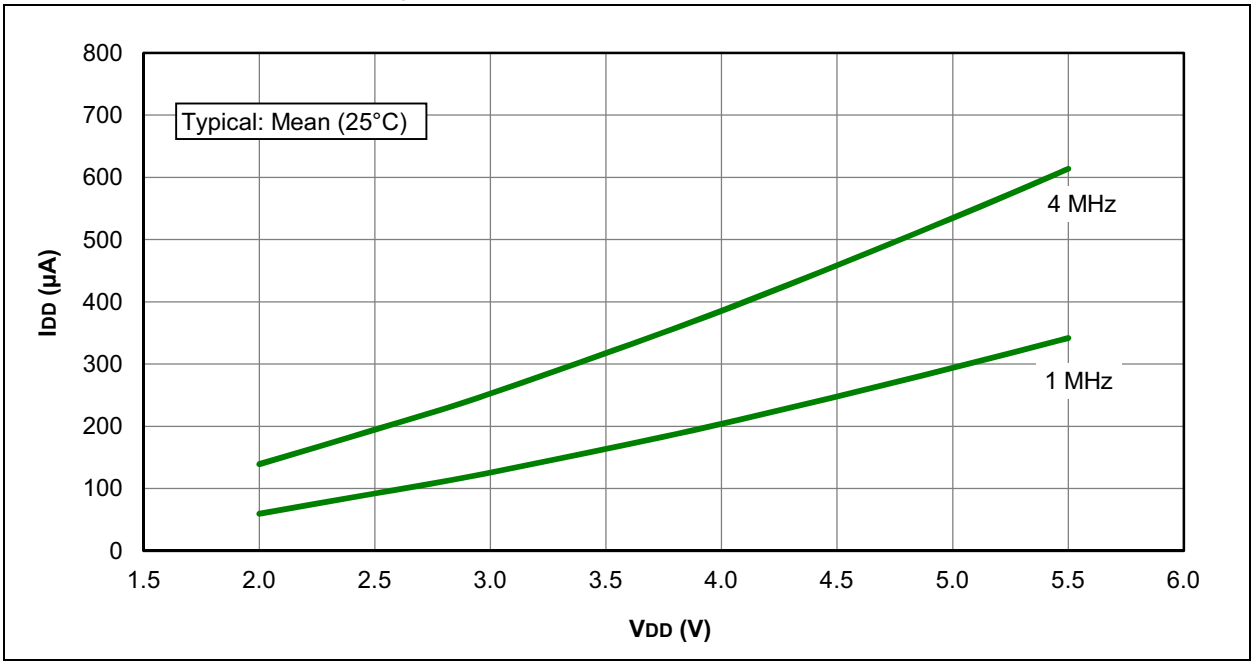
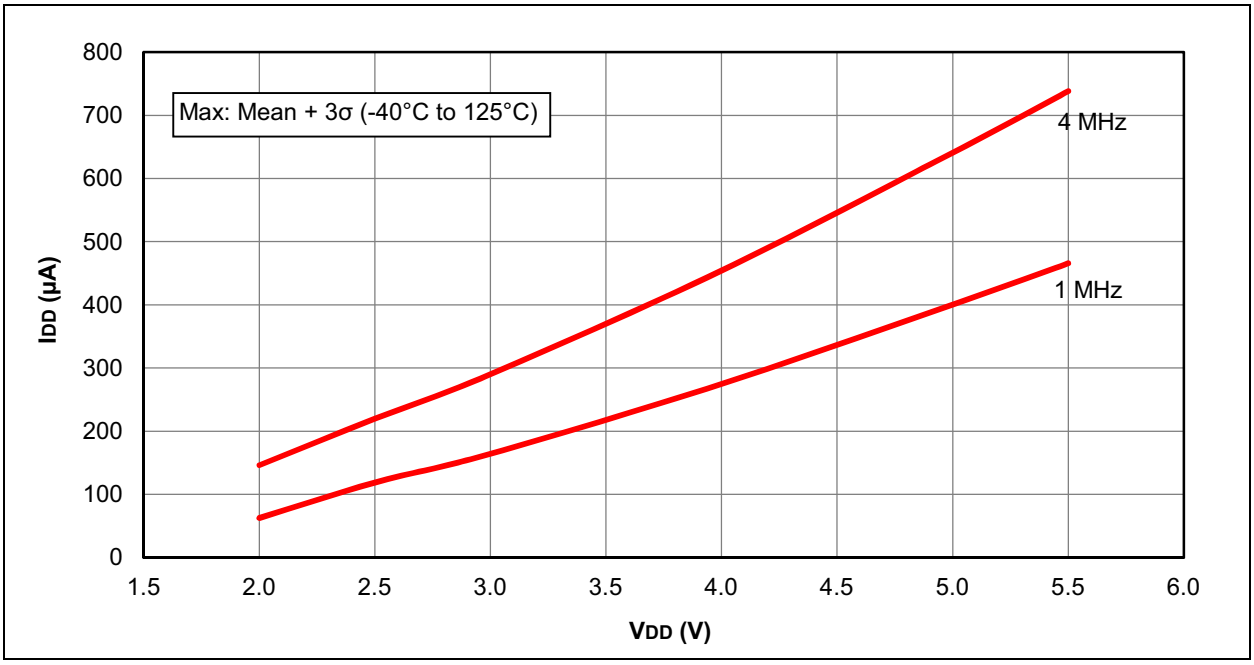
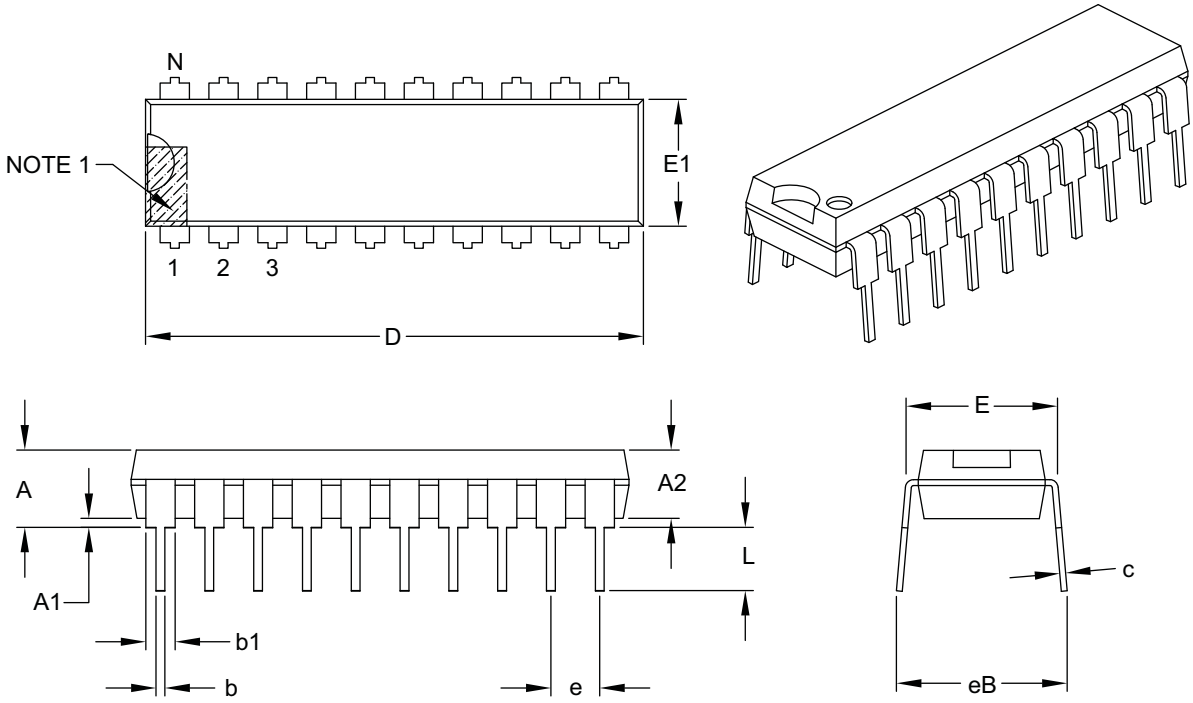


FIGURE 16-5: IDD MAXIMUM, EXTERNAL CLOCK MODE



20-Lead Plastic Dual In-Line (P) – 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		20	
Pitch	e		.100 BSC	
Top to Seating Plane	A	–	–	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.300	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.980	1.030	1.060
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.045	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	–	–	.430

Notes:

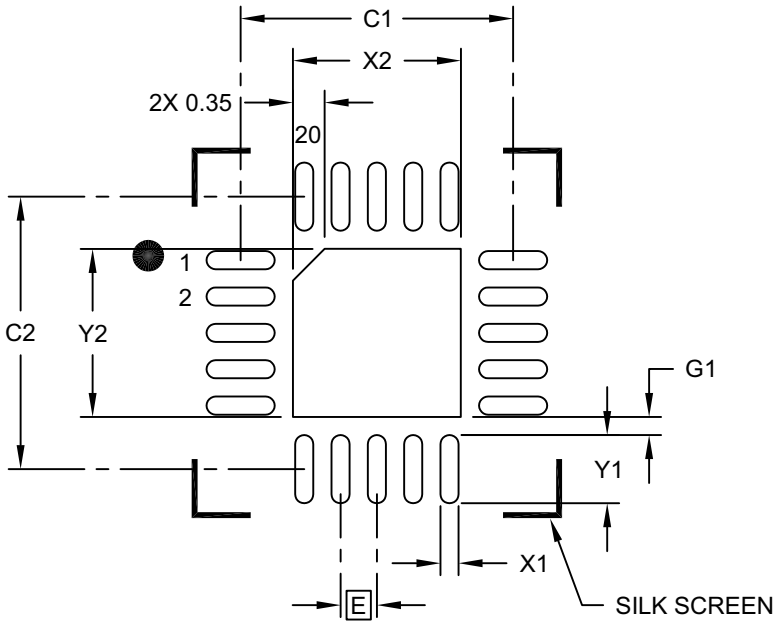
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic.
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-019B

20-Lead Ultra Thin Plastic Quad Flat, No Lead Package (JP) - 3x3x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	X2			1.85
Optional Center Pad Length	Y2			1.85
Contact Pad Spacing	C1		3.00	
Contact Pad Spacing	C2		3.00	
Contact Pad Width (X20)	X1			0.20
Contact Pad Length (X20)	Y1			0.75
Contact Pad to Center Pad (X20)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2256A