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### What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

### Applications of "[Embedded - Microcontrollers](#)"

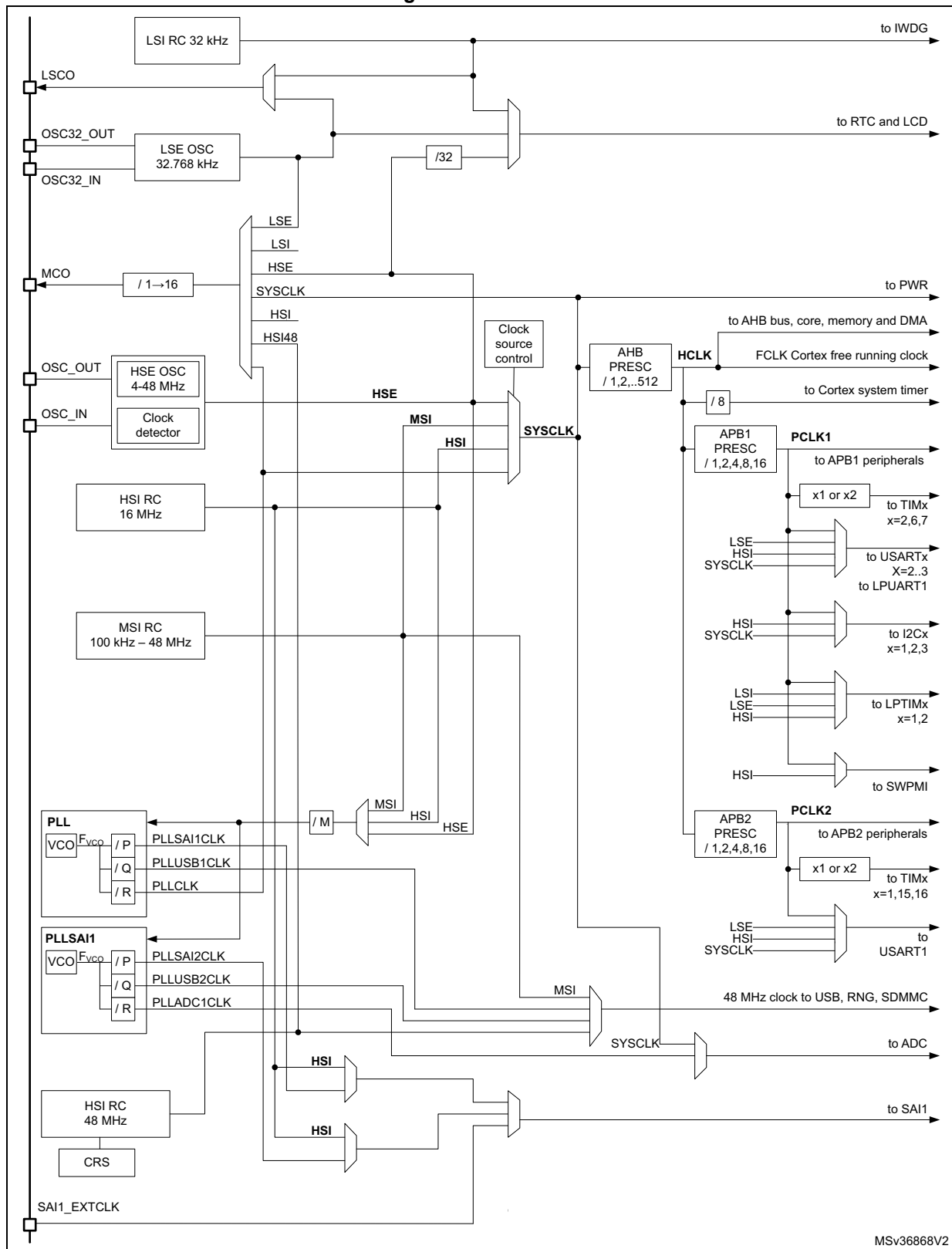
#### Details

Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I <sup>2</sup> C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l443cct6">https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l443cct6</a>

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Figure 3. Clock tree



### 3.15 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

#### 3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage  $V_{TS}$  that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1\_IN17 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 6. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C ( $\pm 5$ °C), $V_{DDA} = V_{REF+} = 3.0$ V ( $\pm 10$ mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C ( $\pm 5$ °C), $V_{DDA} = V_{REF+} = 3.0$ V ( $\pm 10$ mV)	0x1FFF 75CA - 0x1FFF 75CB

### 3.15.2 Internal voltage reference ( $V_{REFINT}$ )

The internal voltage reference ( $V_{REFINT}$ ) provides a stable (bandgap) voltage output for the ADC and Comparators.  $V_{REFINT}$  is internally connected to the ADC1\_IN0 input channel. The precise voltage of  $V_{REFINT}$  is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 7. Internal voltage reference calibration values

Calibration value name	Description	Memory address
$V_{REFINT}$	Raw data acquired at a temperature of 30 °C ( $\pm 5$ °C), $V_{DDA} = V_{REF+} = 3.0$ V ( $\pm 10$ mV)	0x1FFF 75AA - 0x1FFF 75AB

### 3.15.3 $V_{BAT}$ battery voltage monitoring

This embedded hardware feature allows the application to measure the  $V_{BAT}$  battery voltage using the internal ADC channel ADC1\_IN18. As the  $V_{BAT}$  voltage may be higher than  $V_{DDA}$ , and thus outside the ADC input range, the  $V_{BAT}$  pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third the  $V_{BAT}$  voltage.

## 3.16 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

### 3.17 Voltage reference buffer (VREFBUF)

The STM32L443xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

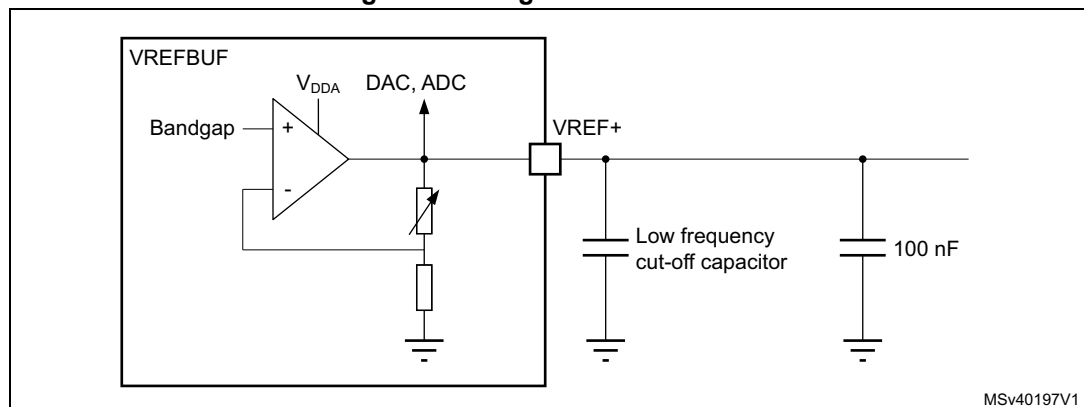
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 4. Voltage reference buffer



### 3.18 Comparators (COMP)

The STM32L443xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

### 3.26 Inter-integrated circuit interface (I2C)

The device embeds 3 I2C. Refer to [Table 9: I2C implementation](#) for the features implementation.

The I<sup>2</sup>C bus interface handles communications between the microcontroller and the serial I<sup>2</sup>C bus. It controls all I<sup>2</sup>C bus-specific sequencing, protocol, arbitration and timing.

The I2C peripheral supports:

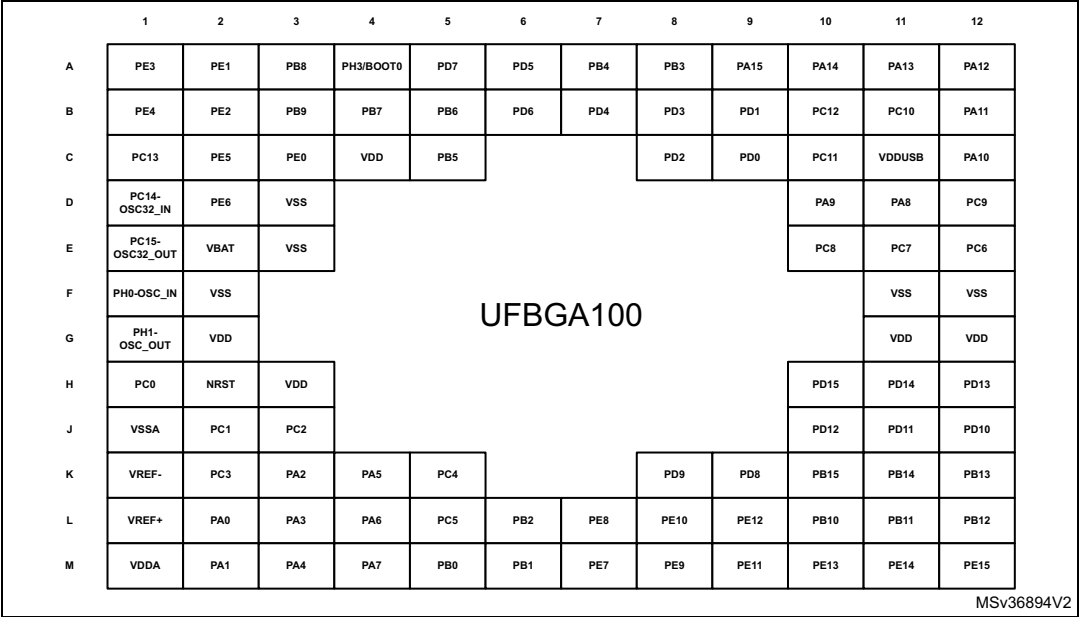
- I<sup>2</sup>C-bus specification and user manual rev. 5 compatibility:
  - Slave and master modes, multimaster capability
  - Standard-mode (Sm), with a bitrate up to 100 kbit/s
  - Fast-mode (Fm), with a bitrate up to 400 kbit/s
  - Fast-mode Plus (Fm+), with a bitrate up to 1 Mbit/s and 20 mA output drive I/Os
  - 7-bit and 10-bit addressing mode, multiple 7-bit slave addresses
  - Programmable setup and hold times
  - Optional clock stretching
- System Management Bus (SMBus) specification rev 2.0 compatibility:
  - Hardware PEC (Packet Error Checking) generation and verification with ACK control
  - Address resolution protocol (ARP) support
  - SMBus alert
- Power System Management Protocol (PMBus™) specification rev 1.1 compatibility
- Independent clock: a choice of independent clock sources allowing the I2C communication speed to be independent from the PCLK reprogramming. Refer to [Figure 3: Clock tree](#).
- Wakeup from Stop mode on address match
- Programmable analog and digital noise filters
- 1-byte buffer with DMA capability

**Table 9. I2C implementation**

I2C features <sup>(1)</sup>	I2C1	I2C2	I2C3
Standard-mode (up to 100 kbit/s)	X	X	X
Fast-mode (up to 400 kbit/s)	X	X	X
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)	X	X	X
Programmable analog and digital noise filters	X	X	X
SMBus/PMBus hardware support	X	X	X
Independent clock	X	X	X
Wakeup from Stop 0 / Stop 1 mode on address match	X	X	X
Wakeup from Stop 2 mode on address match	-	-	X

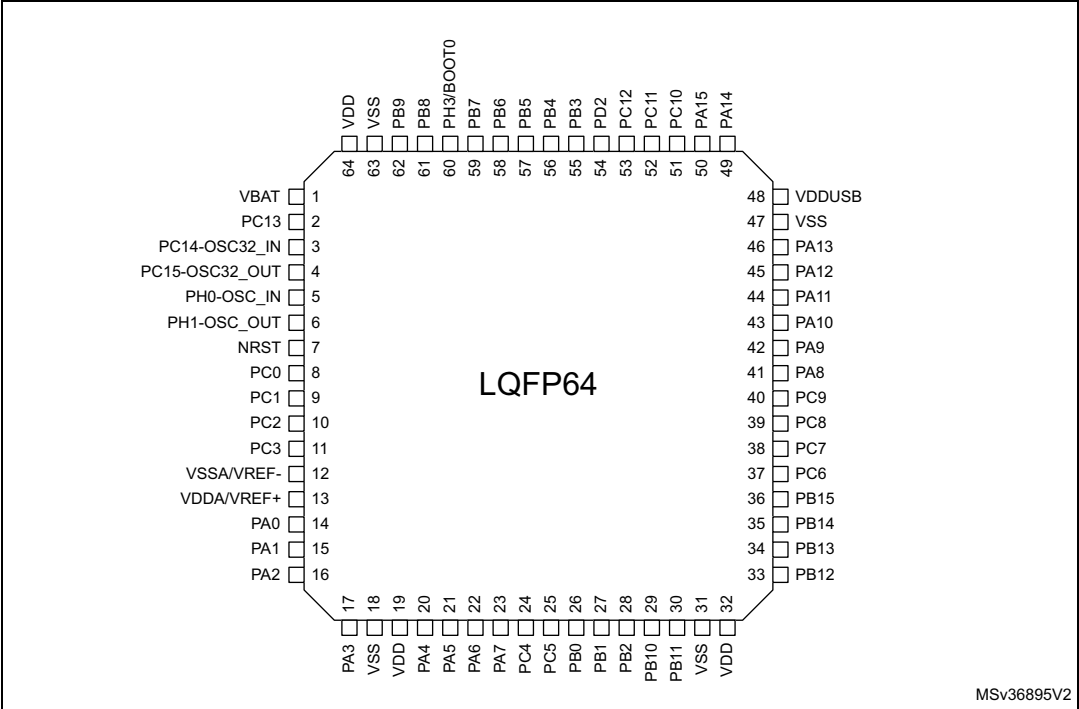
1. X: supported

Figure 6. STM32L443Vx UFBGA100 ballout<sup>(1)</sup>



1. The above figure shows the package top view.

Figure 7. STM32L443Rx LQFP64 pinout<sup>(1)</sup>



1. The above figure shows the package top view.

Table 13. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WL CSP49	WL CSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
25	25	F1	G3	33	H8	51	L12	PB12	I/O	FT_I	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, SWPMI1_IO, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
26	26	E2	G2	34	G8	52	K12	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SWPMI1_TX, SAI1_SCK_A, TIM15_CH1N, EVENTOUT	-
27	27	E1	G1	35	F8	53	K11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C2_SDA, SPI2_MISO, USART3_RTS_DE, TSC_G1_IO3, LCD_SEG14, SWPMI1_RX, SAI1_MCLK_A, TIM15_CH1, EVENTOUT	-
28	28	D3	F2	36	F7	54	K10	PB15	I/O	FT_I	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SWPMI1_SUSPEND, SAI1_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	-	55	K9	PD8	I/O	FT_I	-	USART3_TX, LCD_SEG28, EVENTOUT	-
-	-	-	-	-	-	56	K8	PD9	I/O	FT_I	-	USART3_RX, LCD_SEG29, EVENTOUT	-
-	-	-	-	-	-	57	J12	PD10	I/O	FT_I	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, EVENTOUT	-

Table 13. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLSP49	WLSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	97	C3	PE0	I/O	FT_I	-	LCD_SEG36, TIM16_CH1, EVENTOUT	-
-	-	-	-	-	-	98	A2	PE1	I/O	FT_I	-	LCD_SEG37, EVENTOUT	-
47	47	A6	A7	63	D4	99	D3	VSS	S	-	-	-	-
48	48	A7	A8	64	E4	100	C4	VDD	S	-	-	-	-

1. PC13, PC14 and PC15 are supplied through the power switch. Since the switch only sinks a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited:
  - The speed should not exceed 2 MHz with a maximum load of 30 pF
  - These GPIOs must not be used as current sources (e.g. to drive an LED).
2. After a Backup domain power-up, PC13, PC14 and PC15 operate as GPIOs. Their function then depends on the content of the RTC registers which are not reset by the system reset. For details on how to manage these GPIOs, refer to the Backup domain and RTC register descriptions in the RM0394 reference manual.
3. After reset, these pins are configured as JTAG/SW debug alternate functions, and the internal pull-up on PA15, PA13, PB4 pins and the internal pull-down on PA14 pin are activated.

Table 16. STM32L443xx memory map and peripheral register boundary addresses <sup>(1)</sup>

Bus	Boundary address	Size(bytes)	Peripheral
AHB2	0x5006 0800 - 0x5006 0BFF	1 KB	RNG
	0x5006 0400 - 0x5006 07FF	158 KB	Reserved
	0x5006 0000 - 0x5006 03FF	1 KB	AES
	0x5004 0400 - 0x5005 FFFF	158 KB	Reserved
	0x5004 0000 - 0x5004 03FF	1 KB	ADC
	0x5000 0000 - 0x5003 FFFF	16 KB	Reserved
	0x4800 2000 - 0x4FFF FFFF	~127 MB	Reserved
	0x4800 1C00 - 0x4800 1FFF	1 KB	GPIOH
	0x4800 1400 - 0x4800 1BFF	2 KB	Reserved
	0x4800 1000 - 0x4800 13FF	1 KB	GPIOE
	0x4800 0C00 - 0x4800 0FFF	1 KB	GPIOD
	0x4800 0800 - 0x4800 0BFF	1 KB	GPIOC
	0x4800 0400 - 0x4800 07FF	1 KB	GPIOB
	0x4800 0000 - 0x4800 03FF	1 KB	GPIOA
-	0x4002 4400 - 0x47FF FFFF	~127 MB	Reserved
AHB1	0x4002 4000 - 0x4002 43FF	1 KB	TSC
	0x4002 3400 - 0x4002 3FFF	1 KB	Reserved
	0x4002 3000 - 0x4002 33FF	1 KB	CRC
	0x4002 2400 - 0x4002 2FFF	3 KB	Reserved
	0x4002 2000 - 0x4002 23FF	1 KB	FLASH registers
	0x4002 1400 - 0x4002 1FFF	3 KB	Reserved
	0x4002 1000 - 0x4002 13FF	1 KB	RCC
	0x4002 0800 - 0x4002 0FFF	2 KB	Reserved
	0x4002 0400 - 0x4002 07FF	1 KB	DMA2
	0x4002 0000 - 0x4002 03FF	1 KB	DMA1
APB2	0x4001 5800 - 0x4001 FFFF	42 KB	Reserved
	0x4001 5400 - 0x4000 57FF	1 KB	SAI1
	0x4001 4800 - 0x4000 53FF	3 KB	Reserved
	0x4001 4400 - 0x4001 47FF	1 KB	TIM16
	0x4001 4000 - 0x4001 43FF	1 KB	TIM15
	0x4001 3C00 - 0x4001 3FFF	1 KB	Reserved
	0x4001 3800 - 0x4001 3BFF	1 KB	USART1
	0x4001 3400 - 0x4001 37FF	1 KB	Reserved
	0x4001 3000 - 0x4001 33FF	1 KB	SPI1
	0x4001 2C00 - 0x4001 2FFF	1 KB	TIM1

Table 20. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T <sub>A</sub>	Ambient temperature for the suffix 6 version	Maximum power dissipation	−40	85	°C
		Low-power dissipation <sup>(5)</sup>	−40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	−40	105	
		Low-power dissipation <sup>(5)</sup>	−40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	−40	125	
		Low-power dissipation <sup>(5)</sup>	−40	130	
T <sub>J</sub>	Junction temperature range	Suffix 6 version	−40	105	°C
		Suffix 7 version	−40	125	
		Suffix 3 version	−40	130	

- When RESET is released functionality is guaranteed down to V<sub>BOR0</sub> Min.
- This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V<sub>DD</sub>, V<sub>DDA</sub>, V<sub>DDUSB</sub>, V<sub>LCD</sub>)+3.6 V and 5.5V.
- For operation with voltage higher than Min (V<sub>DD</sub>, V<sub>DDA</sub>, V<sub>DDUSB</sub>, V<sub>LCD</sub>) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.
- If T<sub>A</sub> is lower, higher P<sub>D</sub> values are allowed as long as T<sub>J</sub> does not exceed T<sub>Jmax</sub> (see [Section 7.9: Thermal characteristics](#)).
- In low-power dissipation state, T<sub>A</sub> can be extended to this range as long as T<sub>J</sub> does not exceed T<sub>Jmax</sub> (see [Section 7.9: Thermal characteristics](#)).

### 6.3.2 Operating conditions at power-up / power-down

The parameters given in [Table 21](#) are derived from tests performed under the ambient temperature condition summarized in [Table 20](#).

Table 21. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t <sub>VDD</sub>	V <sub>DD</sub> rise time rate	-	0	∞	μs/V
	V <sub>DD</sub> fall time rate		10	∞	
t <sub>VDDA</sub>	V <sub>DDA</sub> rise time rate	-	0	∞	
	V <sub>DDA</sub> fall time rate		10	∞	
t <sub>VDDUSB</sub>	V <sub>DDUSB</sub> rise time rate	-	0	∞	
	V <sub>DDUSB</sub> fall time rate		10	∞	

### 6.3.3 Embedded reset and power control block characteristics

The parameters given in [Table 22](#) are derived from tests performed under the ambient temperature conditions summarized in [Table 20: General operating conditions](#).

Figure 18.  $V_{REFINT}$  versus temperature

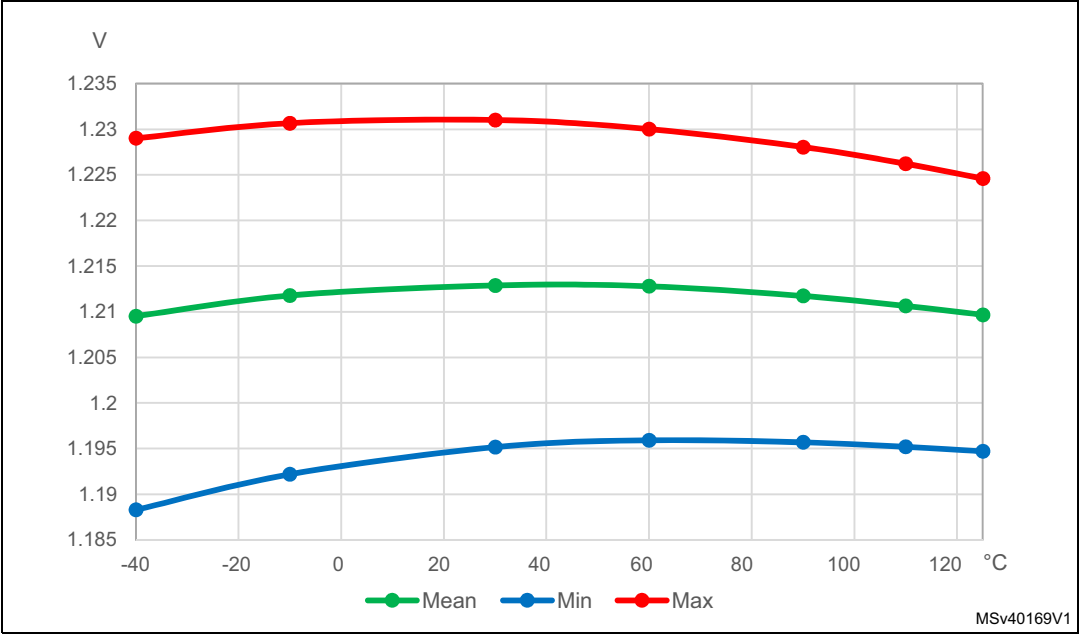


Table 34. Current consumption in Stop 0

Symbol	Parameter	Conditions	TYP					MAX <sup>(1)</sup>					Unit
		V <sub>DD</sub>	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I <sub>DD</sub> (Stop 0)	Supply current in Stop 0 mode, RTC disabled	1.8 V	108	119	158	221	347	133	158	244	395	704	μA
		2.4 V	110	121	160	223	349	136	161	248	399	710	
		3 V	111	123	161	224	352	139	164	251	403	716	
		3.6 V	114	125	163	227	355	142	167	254	408	722 <sup>(2)</sup>	

1. Guaranteed by characterization results, unless otherwise specified.
2. Guaranteed by test in production.



### On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in [Table 38](#). The MCU is placed under the following conditions:

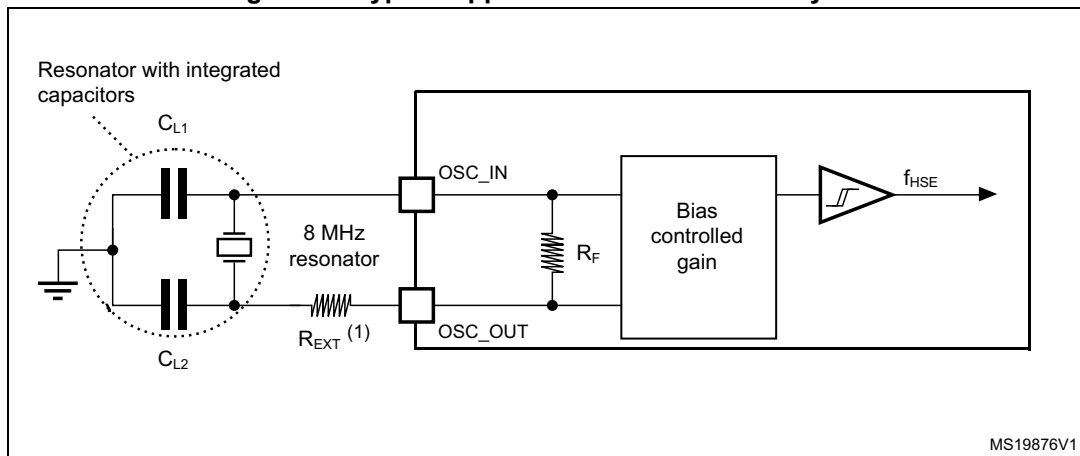
- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in [Table 17: Voltage characteristics](#)
- The power consumption of the digital part of the on-chip peripherals is given in [Table 38](#). The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

**Table 38. Peripheral current consumption**

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix <sup>(1)</sup>	3.2	2.9	3.1	μA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	AES	1.7	1.5	1.6	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA <sup>(2)</sup>	1.7	1.4	1.6	
	GPIOB <sup>(2)</sup>	1.6	1.3	1.6	
	GPIOC <sup>(2)</sup>	1.7	1.5	1.6	
	GPIOD <sup>(2)</sup>	1.8	1.6	1.7	
	GPIOE <sup>(2)</sup>	1.7	1.6	1.6	
	GPIOH <sup>(2)</sup>	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	NA	NA	
	RNG clock domain	0.5	NA	NA	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge <sup>(3)</sup>	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	

**Note:** For information on selecting the crystal, refer to the application note AN2867 “Oscillator design guide for ST microcontrollers” available from the ST website [www.st.com](http://www.st.com).

**Figure 21. Typical application with an 8 MHz crystal**



1. R<sub>EXT</sub> value depends on the crystal characteristics.

### Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in [Table 45](#). In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

**Table 45. LSE oscillator characteristics (f<sub>LSE</sub> = 32.768 kHz)<sup>(1)</sup>**

Symbol	Parameter	Conditions <sup>(2)</sup>	Min	Typ	Max	Unit
I <sub>DD(LSE)</sub>	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
G <sub>m</sub> <sub>critmax</sub>	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	μA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
t <sub>SU(LSE)</sub> <sup>(3)</sup>	Startup time	V <sub>DD</sub> is stabilized	-	2	-	s

Table 47. MSI oscillator characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$I_{DD}(MSI)^{(6)}$	MSI oscillator power consumption	MSI and PLL mode	Range 0	-	-	0.6	1
			Range 1	-	-	0.8	1.2
			Range 2	-	-	1.2	1.7
			Range 3	-	-	1.9	2.5
			Range 4	-	-	4.7	6
			Range 5	-	-	6.5	9
			Range 6	-	-	11	15
			Range 7	-	-	18.5	25
			Range 8	-	-	62	80
			Range 9	-	-	85	110
			Range 10	-	-	110	130
			Range 11	-	-	155	190

1. Guaranteed by characterization results.
2. This is a deviation for an individual part once the initial frequency has been measured.
3. Sampling mode means Low-power run/Low-power sleep modes with Temperature sensor disable.
4. Average period of MSI @48 MHz is compared to a real 48 MHz clock over 28 cycles. It includes frequency tolerance + jitter of MSI @48 MHz clock.
5. Only accumulated jitter of MSI @48 MHz is extracted over 28 cycles.  
For next transition: min. and max. jitter of 2 consecutive frame of 28 cycles of the MSI @48 MHz, for 1000 captures over 28 cycles.  
For paired transitions: min. and max. jitter of 2 consecutive frame of 56 cycles of the MSI @48 MHz, for 1000 captures over 56 cycles.
6. Guaranteed by design.

### Static latch-up

Two complementary static tests are required on six parts to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin.
- A current injection is applied to each input, output and configurable I/O pin.

These tests are compliant with EIA/JESD 78A IC latch-up standard.

**Table 56. Electrical sensitivities**

Symbol	Parameter	Conditions	Class
LU	Static latch-up class	$T_A = +105\text{ }^{\circ}\text{C}$ conforming to JESD78A	II

### 6.3.13 I/O current injection characteristics

As a general rule, current injection to the I/O pins, due to external voltage below  $V_{SS}$  or above  $V_{DDIOx}$  (for standard, 3.3 V-capable I/O pins) should be avoided during normal product operation. However, in order to give an indication of the robustness of the microcontroller in cases when abnormal injection accidentally happens, susceptibility tests are performed on a sample basis during device characterization.

#### Functional susceptibility to I/O current injection

While a simple application is executed on the device, the device is stressed by injecting current into the I/O pins programmed in floating input mode. While current is injected into the I/O pin, one at a time, the device is checked for functional failures.

The failure is indicated by an out of range parameter: ADC error above a certain limit (higher than 5 LSB TUE), out of conventional limits of induced leakage current on adjacent pins (out of the  $-5\text{ }\mu\text{A}/+0\text{ }\mu\text{A}$  range) or other functional failure (for example reset occurrence or oscillator frequency deviation).

The characterization results are given in [Table 57](#).

Negative induced leakage current is caused by negative injection and positive induced leakage current is caused by positive injection.

**Table 57. I/O current injection susceptibility<sup>(1)</sup>**

Symbol	Description	Functional susceptibility		Unit
		Negative injection	Positive injection	
$I_{INJ}$	Injected current on all pins except PA4, PA5, PE8, PE9, PE10, PE11, PE12	-5	NA	mA
	Injected current on PE8, PE9, PE10, PE11, PE12	-0	NA	
	Injected current on PA4, PA5 pins	-5	0	

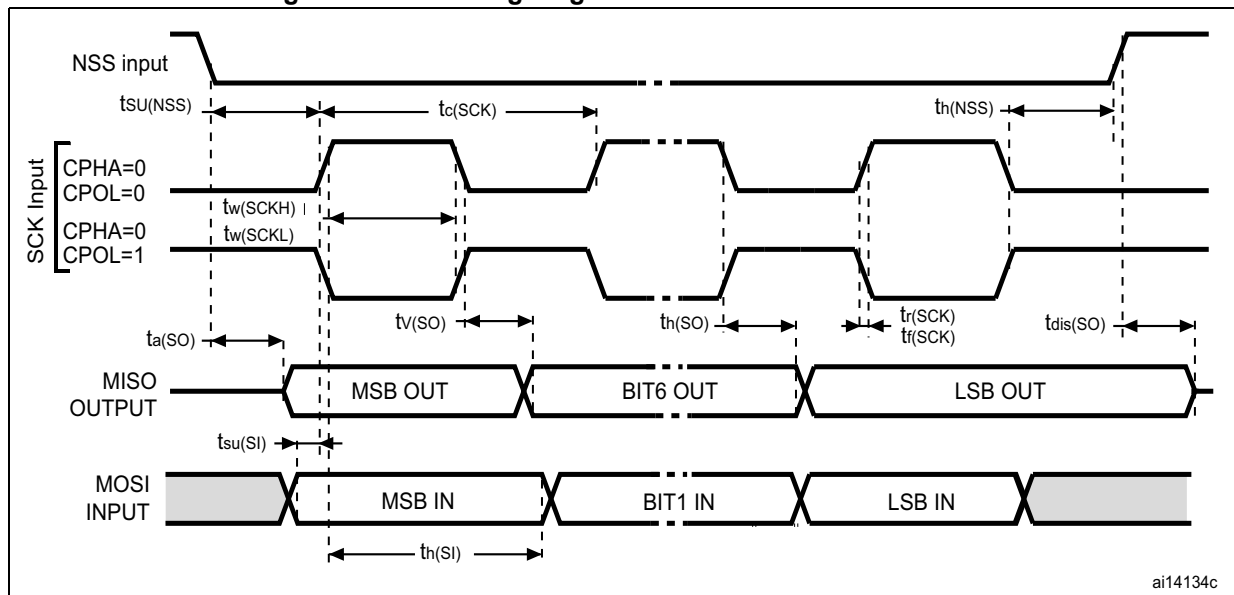
1. Guaranteed by characterization results.

Table 82. SPI characteristics<sup>(1)</sup> (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{v(SO)}$	Data output valid time	Slave mode $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	12.5	13.5	ns
		Slave mode $1.71 < V_{DD} < 3.6$ V Voltage Range 1	-	12.5	24	
		Slave mode $1.71 < V_{DD} < 3.6$ V Voltage Range 2	-	12.5	33	
$t_{v(MO)}$		Master mode	-	4.5	6	
$t_{h(SO)}$	Data output hold time	Slave mode	7	-	-	ns
$t_{h(MO)}$		Master mode	0	-	-	

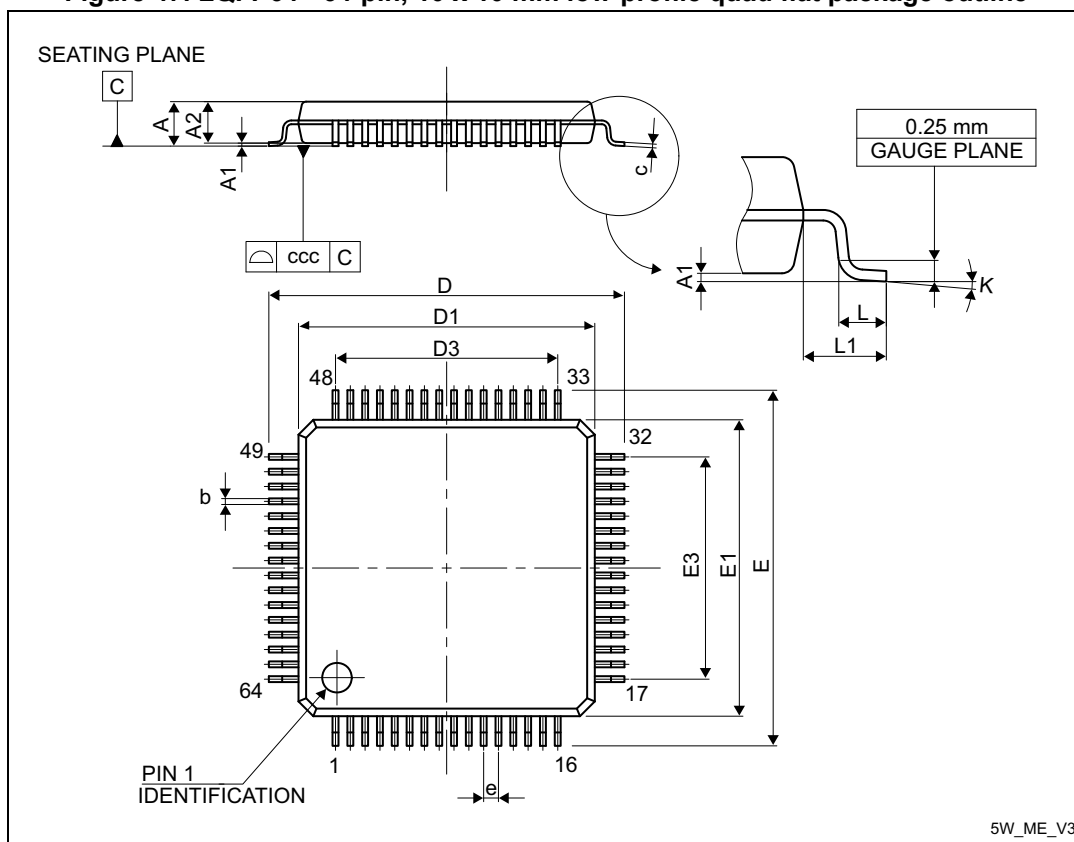
1. Guaranteed by characterization results.
2. Maximum frequency in Slave transmitter mode is determined by the sum of  $t_{v(SO)}$  and  $t_{su(MI)}$  which has to fit into SCK low or high phase preceding the SCK sampling edge. This value can be achieved when the SPI communicates with a master having  $t_{su(MI)} = 0$  while  $Duty(SCK) = 50\%$ .

Figure 32. SPI timing diagram - slave mode and CPHA = 0



## 7.3 LQFP64 package information

Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline

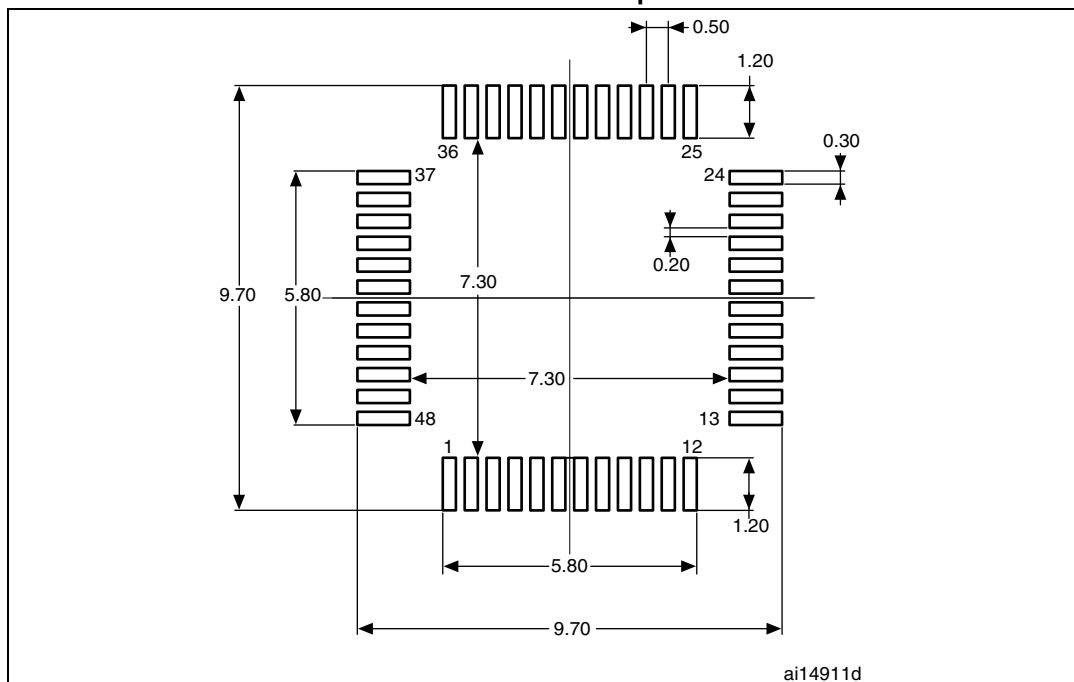


1. Drawing is not to scale.

Table 93. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data

Symbol	millimeters			inches <sup>(1)</sup>		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

**Figure 60. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package recommended footprint**

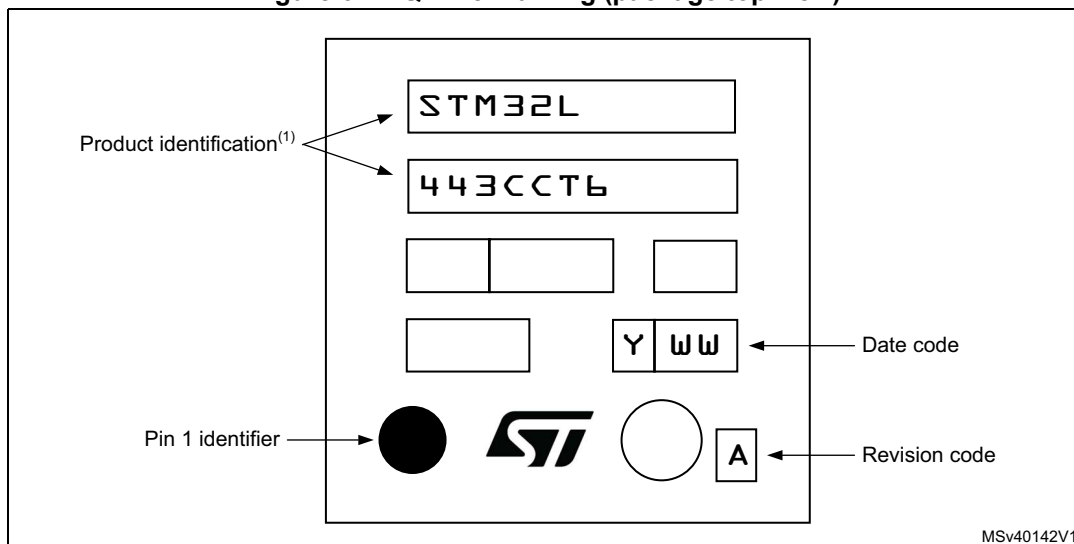


1. Dimensions are expressed in millimeters.

### Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

**Figure 61. LQFP48 marking (package top view)**



1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.