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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	38
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 10x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-UFQFN Exposed Pad
Supplier Device Package	48-UFQFPN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l443ccu6

3.15 Analog to digital converter (ADC)

The device embeds a successive approximation analog-to-digital converter with the following features:

- 12-bit native resolution, with built-in calibration
- 5.33 Msps maximum conversion rate with full resolution
  - Down to 18.75 ns sampling time
  - Increased conversion rate for lower resolution (up to 8.88 Msps for 6-bit resolution)
- Up to 16 external channels.
- 5 internal channels: internal reference voltage, temperature sensor, VBAT/3, DAC1 and DAC2 outputs.
- One external reference pin is available on some package, allowing the input voltage range to be independent from the power supply
- Single-ended and differential mode inputs
- Low-power design
  - Capable of low-current operation at low conversion rate (consumption decreases linearly with speed)
  - Dual clock domain architecture: ADC speed independent from CPU frequency
- Highly versatile digital interface
  - Single-shot or continuous/discontinuous sequencer-based scan mode: 2 groups of analog signals conversions can be programmed to differentiate background and high-priority real-time conversions
  - ADC supports multiple trigger inputs for synchronization with on-chip timers and external signals
  - Results stored into data register or in RAM with DMA controller support
  - Data pre-processing: left/right alignment and per channel offset compensation
  - Built-in oversampling unit for enhanced SNR
  - Channel-wise programmable sampling time
  - Three analog watchdog for automatic voltage monitoring, generating interrupts and trigger for selected timers
  - Hardware assistant to prepare the context of the injected channels to allow fast context switching

3.15.1 Temperature sensor

The temperature sensor (TS) generates a voltage V_{TS} that varies linearly with temperature.

The temperature sensor is internally connected to the ADC1_IN17 input channel which is used to convert the sensor output voltage into a digital value.

The sensor provides good linearity but it has to be calibrated to obtain good overall accuracy of the temperature measurement. As the offset of the temperature sensor varies from chip to chip due to process variation, the uncalibrated internal temperature sensor is suitable for applications that detect temperature changes only.

To improve the accuracy of the temperature sensor measurement, each device is individually factory-calibrated by ST. The temperature sensor factory calibration data are stored by ST in the system memory area, accessible in read-only mode.

Table 6. Temperature sensor calibration values

Calibration value name	Description	Memory address
TS_CAL1	TS ADC raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75A8 - 0x1FFF 75A9
TS_CAL2	TS ADC raw data acquired at a temperature of 130 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75CA - 0x1FFF 75CB

3.15.2 Internal voltage reference (V_{REFINT})

The internal voltage reference (VREFINT) provides a stable (bandgap) voltage output for the ADC and Comparators. VREFINT is internally connected to the ADC1_IN0 input channel. The precise voltage of VREFINT is individually measured for each part by ST during production test and stored in the system memory area. It is accessible in read-only mode.

Table 7. Internal voltage reference calibration values

Calibration value name	Description	Memory address
VREFINT	Raw data acquired at a temperature of 30 °C (± 5 °C), $V_{DDA} = V_{REF+}$ = 3.0 V (± 10 mV)	0x1FFF 75AA - 0x1FFF 75AB

3.15.3 V_{BAT} battery voltage monitoring

This embedded hardware feature allows the application to measure the V_{BAT} battery voltage using the internal ADC channel ADC1_IN18. As the V_{BAT} voltage may be higher than VDDA, and thus outside the ADC input range, the VBAT pin is internally connected to a bridge divider by 3. As a consequence, the converted digital value is one third the V_{BAT} voltage.

3.16 Digital to analog converter (DAC)

Two 12-bit buffered DAC channels can be used to convert digital signals into analog voltage signal outputs. The chosen design structure is composed of integrated resistor strings and an amplifier in inverting configuration.

This digital interface supports the following features:

- Up to two DAC output channels
- 8-bit or 12-bit output mode
- Buffer offset calibration (factory and user trimming)
- Left or right data alignment in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation

Table 15. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 14*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port D	PD0	-	CAN1_RX	-	-	-	-	-	EVENTOUT
	PD1	-	CAN1_TX	-	-	-	-	-	EVENTOUT
	PD2	-	TSC_SYNC	-	LCD_COM7/ LCD_SEG31/ LCD_SEG43	SDMMC1_ CMD	-	-	EVENTOUT
Port D	PD3	-	-	QUADSPI_BK2 _NCS	-	-	-	-	EVENTOUT
	PD4	-	-	QUADSPI_BK2 _IO0	-	-	-	-	EVENTOUT
	PD5	-	-	QUADSPI_BK2 _IO1	-	-	-	-	EVENTOUT
	PD6	-	-	QUADSPI_BK2 _IO2	-	-	SAI1_SD_A	-	EVENTOUT
	PD7	-	-	QUADSPI_BK2 _IO3	-	-	-	-	EVENTOUT
	PD8	-	-	-	LCD_SEG28	-	-	-	EVENTOUT
	PD9	-	-	-	LCD_SEG29	-	-	-	EVENTOUT
	PD10	-	TSC_G6_IO1	-	LCD_SEG30	-	-	-	EVENTOUT
	PD11	-	TSC_G6_IO2	-	LCD_SEG31	-	-	LPTIM2_ETR	EVENTOUT
	PD12	-	TSC_G6_IO3	-	LCD_SEG32	-	-	LPTIM2_IN1	EVENTOUT
	PD13	-	TSC_G6_IO4	-	LCD_SEG33	-	-	LPTIM2_OUT	EVENTOUT
	PD14	-	-	-	LCD_SEG34	-	-	-	EVENTOUT
	PD15	-	-	-	LCD_SEG35	-	-	-	EVENTOUT

Table 15. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 14*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT

Table 16. STM32L443xx memory map and peripheral register boundary addresses

Bus	Boundary address	Size(bytes)	Peripheral
APB2	0x4001 2800 - 0x4001 2BFF	1 KB	SDMMC1
	0x4001 2000 - 0x4001 27FF	2 KB	Reserved
	0x4001 1C00 - 0x4001 1FFF	1 KB	FIREWALL
	0x4001 0800- 0x4001 1BFF	5 KB	Reserved
	0x4001 0400 - 0x4001 07FF	1 KB	EXTI
	0x4001 0200 - 0x4001 03FF	1 KB	COMP
	0x4001 0030 - 0x4001 01FF		VREFBUF
	0x4001 0000 - 0x4001 002F		SYSCFG
APB1	0x4000 9800 - 0x4000 FFFF	26 KB	Reserved
	0x4000 9400 - 0x4000 97FF	1 KB	LPTIM2
	0x4000 8C00 - 0x4000 93FF	2 KB	Reserved
	0x4000 8800 - 0x4000 8BFF	1 KB	SWPMI1
	0x4000 8400 - 0x4000 87FF	1 KB	Reserved
	0x4000 8000 - 0x4000 83FF	1 KB	LPUART1
	0x4000 7C00 - 0x4000 7FFF	1 KB	LPTIM1
	0x4000 7800 - 0x4000 7BFF	1 KB	OPAMP
	0x4000 7400 - 0x4000 77FF	1 KB	DAC
	0x4000 7000 - 0x4000 73FF	1 KB	PWR
	0x4000 6C00 - 0x4000 6FFF	1 KB	USB SRAM
	0x4000 6800 - 0x4000 6BFF	1 KB	USB FS
	0x4000 6400 - 0x4000 67FF	1 KB	CAN1
	0x4000 6000 - 0x4000 63FF	1 KB	CRS
	0x4000 5C00- 0x4000 5FFF	1 KB	I2C3
	0x4000 5800 - 0x4000 5BFF	1 KB	I2C2
	0x4000 5400 - 0x4000 57FF	1 KB	I2C1
	0x4000 4C00 - 0x4000 53FF	2 KB	Reserved
	0x4000 4800 - 0x4000 4BFF	1 KB	USART3
	0x4000 4400 - 0x4000 47FF	1 KB	USART2
	0x4000 4000 - 0x4000 43FF	1 KB	Reserved
	0x4000 3C00 - 0x4000 3FFF	1 KB	SPI3
	0x4000 3800 - 0x4000 3BFF	1 KB	SPI2
	0x4000 3400 - 0x4000 37FF	1 KB	Reserved
	0x4000 3000 - 0x4000 33FF	1 KB	IWDG
	0x4000 2C00 - 0x4000 2FFF	1 KB	WWDG
	0x4000 2800 - 0x4000 2BFF	1 KB	RTC

Table 25. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.66	2.68	2.73	2.81	2.96	3.0	3.1	3.2	3.3	3.6	mA
				16 MHz	1.88	1.9	1.94	2.02	2.17	2.1	2.2	2.3	2.4	2.7	
				8 MHz	1.05	1.06	1.11	1.18	1.33	1.2	1.2	1.3	1.4	1.7	
				4 MHz	0.6	0.62	0.66	0.73	0.87	0.7	0.7	0.8	0.9	1.2	
				2 MHz	0.36	0.37	0.34	0.48	0.62	0.4	0.4	0.5	0.6	0.9	
				1 MHz	0.23	0.25	0.25	0.36	0.5	0.3	0.3	0.4	0.5	0.8	
				100 kHz	0.12	0.14	0.17	0.25	0.39	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.56	8.61	8.69	8.79	8.97	9.6	9.7	9.8	10.0	10.3	
				72 MHz	7.74	7.79	7.86	7.96	8.14	8.7	8.7	8.8	9.0	9.4	
				64 MHz	7.63	7.68	7.75	7.85	8.04	8.6	8.6	8.7	8.9	9.3	
				48 MHz	6.36	6.4	6.48	6.58	6.76	7.2	7.3	7.4	7.6	7.9	
				32 MHz	4.56	4.6	4.66	4.76	4.93	5.2	5.2	5.3	5.5	5.8	
				24 MHz	3.45	3.48	3.54	3.64	3.8	3.9	4.0	4.1	4.2	4.6	
				16 MHz	2.48	2.51	2.56	2.65	2.82	2.8	2.9	3.0	3.1	3.5	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	310	317	364	440	593	375.3	400.9	456.7	595.3	909.6	µA
				1 MHz	157	173	226	296	448	204.8	234.2	298.2	445.8	758.9	
				400 kHz	72.6	89	130	206	356	99.7	131.2	199.7	349.3	663.7	
				100 kHz	32.3	46	89.7	164	314	52.4	82.1	153.3	301.2	616.9	

1. Guaranteed by characterization results, unless otherwise specified.

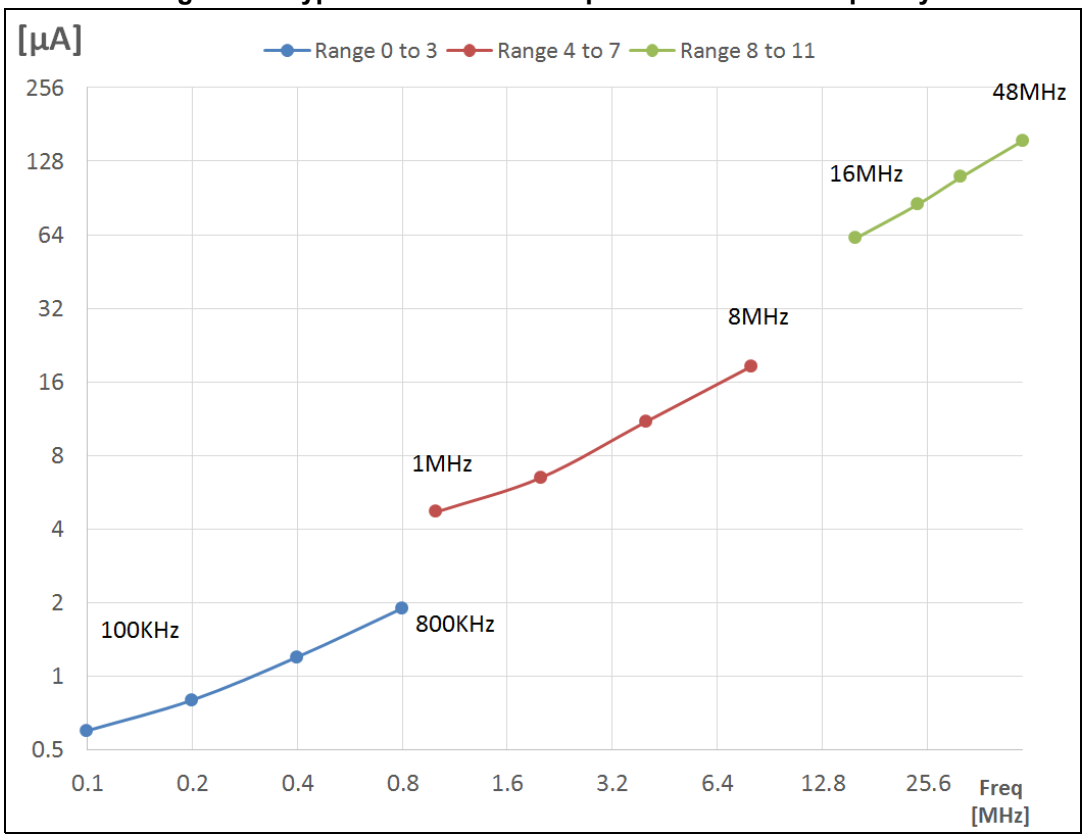
Table 35. Current consumption in Standby mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{DD}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Standby)	Supply current in Standby mode (backup registers retained), RTC disabled	no independent watchdog	1.8 V	27.7	144	758	2 072	5 425	119	425	2866	7524	20510	nA
			2.4 V	50.9	187	892	2 408	6 247	183	564	3383	8778	23768	
			3 V	90.2	253	1 090	2 884	7 409	225	681	3912	10071	26976	
			3.6 V	253	459	1 474	3 575	8 836	292	877	4638	11659	30758	
		with independent watchdog	1.8 V	216	-	-	-	-	-	-	-	-	-	
			2.4 V	342	-	-	-	-	-	-	-	-	-	
			3 V	416	-	-	-	-	-	-	-	-	-	
			3.6 V	551	-	-	-	-	-	-	-	-	-	
I_{DD}(Standby with RTC)	Supply current in Standby mode (backup registers retained), RTC enabled	RTC clocked by LSI, no independent watchdog	1.8 V	287	407	989	2 230	5 396	585	944	3344	7866	20504	nA
			2.4 V	386	526	1 201	2 638	6 274	811	1230	4007	9246	23824	
			3 V	513	679	1 478	3 167	7 414	1022	1521	4683	10671	27124	
			3.6 V	771	978	1 963	3 992	9 039	1284	1924	5577	12383	30954 (2)	
		RTC clocked by LSI, with independent watchdog	1.8 V	342	-	-	-	-	-	-	-	-	-	
			2.4 V	521	-	-	-	-	-	-	-	-	-	
			3 V	655	-	-	-	-	-	-	-	-	-	
			3.6 V	865	-	-	-	-	-	-	-	-	-	
		RTC clocked by LSE bypassed at 32768Hz	1.8 V	142	126	865	2 220	5 650	-	-	-	-	-	nA
			2.4 V	249	219	1 090	2 660	6 600	-	-	-	-	-	
			3 V	404	364	1 410	3 260	7 850	-	-	-	-	-	
			3.6 V	742	670	2 000	4 230	9 700	-	-	-	-	-	
		RTC clocked by LSE quartz (3) in low drive mode	1.8 V	281	423	1 046	2 410	5 700	-	-	-	-	-	
			2.4 V	388	548	1 268	2 847	6 564	-	-	-	-	-	
			3 V	535	715	1 565	3 420	7 694	-	-	-	-	-	
			3.6 V	836	1 048	2 081	4 311	9 338	-	-	-	-	-	

Table 47. MSI oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
$\Delta_{VDD}(MSI)^{(2)}$	MSI oscillator frequency drift over V_{DD} (reference is 3 V)	MSI mode	Range 0 to 3	V_{DD}=1.62 V to 3.6 V	-1.2	-	0.5	%
				V_{DD}=2.4 V to 3.6 V	-0.5	-		
			Range 4 to 7	V_{DD}=1.62 V to 3.6 V	-2.5	-	0.7	
				V_{DD}=2.4 V to 3.6 V	-0.8	-		
			Range 8 to 11	V_{DD}=1.62 V to 3.6 V	-5	-	1	
				V_{DD}=2.4 V to 3.6 V	-1.6	-		
$\Delta F_{SAMPLING}(MSI)^{(2)(6)}$	Frequency variation in sampling mode(3)	MSI mode	T_A= -40 to 85 °C		-	1	2	%
			T_A= -40 to 125 °C		-	2	4	
P_USB Jitter(MSI)(6)	Period jitter for USB clock(4)	PLL mode Range 11	for next transition	-	-	-	3.458	ns
			for paired transition	-	-	-	3.916	
MT_USB Jitter(MSI)(6)	Medium term jitter for USB clock(5)	PLL mode Range 11	for next transition	-	-	-	2	ns
			for paired transition	-	-	-	1	
CC jitter(MSI)(6)	RMS cycle-to-cycle jitter	PLL mode Range 11		-	-	60	-	ps
P jitter(MSI)(6)	RMS Period jitter	PLL mode Range 11		-	-	50	-	ps
$t_{SU}(MSI)^{(6)}$	MSI oscillator start-up time	Range 0		-	-	10	20	us
		Range 1		-	-	5	10	
		Range 2		-	-	4	8	
		Range 3		-	-	3	7	
		Range 4 to 7		-	-	3	6	
		Range 8 to 11		-	-	2.5	6	
$t_{STAB}(MSI)^{(6)}$	MSI oscillator stabilization time	PLL mode Range 11	10 % of final frequency	-	-	0.25	0.5	ms
			5 % of final frequency	-	-	0.5	1.25	
			1 % of final frequency	-	-	-	2.5	

Figure 24. Typical current consumption versus MSI frequency



High-speed internal 48 MHz (HSI48) RC oscillator

Table 48. HSI48 oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI48}	HSI48 Frequency	V_{DD}=3.0V, T_A=30°C	-	48	-	MHz
TRIM	HSI48 user trimming step	-	-	0.11(2)	0.18(2)	%
USER TRIM COVERAGE	HSI48 user trimming coverage	±32 steps	±3(3)	±3.5(3)	-	%
DuCy(HSI48)	Duty Cycle	-	45(2)	-	55(2)	%
ACC_{HSI48_REL}	Accuracy of the HSI48 oscillator over temperature (factory calibrated)	V_{DD} = 3.0 V to 3.6 V, T_A = –15 to 85 °C	-	-	±3(3)	%
		V_{DD} = 1.65 V to 3.6 V, T_A = –40 to 125 °C	-	-	±4.5(3)	
D_{VDD}(HSI48)	HSI48 oscillator frequency drift with V_{DD}	V_{DD} = 3 V to 3.6 V	-	0.025(3)	0.05(3)	%
		V_{DD} = 1.65 V to 3.6 V	-	0.05(3)	0.1(3)	
t_{su}(HSI48)	HSI48 oscillator start-up time	-	-	2.5(2)	6(2)	µs
I_{DD}(HSI48)	HSI48 oscillator power consumption	-	-	340(2)	380(2)	µA

6.3.14 I/O port characteristics

General input/output characteristics

Unless otherwise specified, the parameters given in *Table 58* are derived from tests performed under the conditions summarized in *Table 20: General operating conditions*. All I/Os are designed as CMOS- and TTL-compliant.

Table 58. I/O static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL} (1)	I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	0.3xV_{DDIOx} (2)	V
	I/O input low level voltage	1.62 V<V_{DDIOx}<3.6 V	-	-	0.39xV_{DDIOx}-0.06 (3)	
	I/O input low level voltage	1.08 V<V_{DDIOx}<1.62 V	-	-	0.43xV_{DDIOx}-0.1 (3)	
V_{IH} (1)	I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.7xV_{DDIOx} (2)	-	-	V
	I/O input high level voltage	1.62 V<V_{DDIOx}<3.6 V	0.49xV_{DDIOX}+0.26 (3)	-	-	
	I/O input high level voltage	1.08 V<V_{DDIOx}<1.62 V	0.61xV_{DDIOX}+0.05 (3)	-	-	
V_{hys} (3)	TT_xx, FT_xxx and NRST I/O input hysteresis	1.62 V<V_{DDIOx}<3.6 V	-	200	-	mV
	FT_sx	1.08 V<V_{DDIOx}<1.62 V	-	150	-	
I_{lkg}	FT_xx input leakage current(3)	V_{IN} ≤ Max(V_{DDXXX})(4)	-	-	±100	nA
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)(5)	-	-	650(3)(6)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(3)(5)	-	-	200(6)	
	FT_lu, FT_u and PC3 IO	V_{IN} ≤ Max(V_{DDXXX}) (4)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} ≤ Max(V_{DDXXX})+1 V(4)	-	-	2500(3)(7)	
		Max(V_{DDXXX})+1 V < VIN ≤ 5.5 V(4)(5)(7)	-	-	250(7)	
	TT_xx input leakage current	V_{IN} ≤ Max(V_{DDXXX})(6)	-	-	±150	
		Max(V_{DDXXX}) ≤ V_{IN} < 3.6 V(6)	-	-	2000(3)	
R_{PU}	Weak pull-up equivalent resistor (8)	V_{IN} = V_{SS}	25	40	55	kΩ
R_{PD}	Weak pull-down equivalent resistor(8)	V_{IN} = V_{DDIOx}	25	40	55	kΩ
C_{IO}	I/O pin capacitance	-	-	5	-	pF

1. Refer to *Figure 26: I/O input characteristics*.

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 59. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx} \geq$ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(3)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx} \geq$ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 27* and *Table 60*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

6.3.17 Analog-to-Digital converter characteristics

Unless otherwise specified, the parameters given in *Table 63* are preliminary values derived from tests performed under ambient temperature, f_{PCLK} frequency and V_{DDA} supply voltage conditions summarized in *Table 20: General operating conditions*.

Note: It is recommended to perform a calibration after each power-up.

Table 63. ADC characteristics(1) (2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	1.62	-	3.6	V
V_{REF+}	Positive reference voltage	$V_{DDA} \geq 2$ V	2	-	V_{DDA}	V
		$V_{DDA} < 2$ V	V_{DDA}			V
V_{REF-}	Negative reference voltage	-	V_{SSA}			V
f_{ADC}	ADC clock frequency	Range 1	-	-	80	MHz
		Range 2	-	-	26	
f_s	Sampling rate for FAST channels	Resolution = 12 bits	-	-	5.33	Msps
		Resolution = 10 bits	-	-	6.15	
		Resolution = 8 bits	-	-	7.27	
		Resolution = 6 bits	-	-	8.88	
	Sampling rate for SLOW channels	Resolution = 12 bits	-	-	4.21	
		Resolution = 10 bits	-	-	4.71	
		Resolution = 8 bits	-	-	5.33	
		Resolution = 6 bits	-	-	6.15	
f_{TRIG}	External trigger frequency	f_{ADC} = 80 MHz Resolution = 12 bits	-	-	5.33	MHz
		Resolution = 12 bits	-	-	15	$1/f_{ADC}$
V_{CMIN}	Input common mode	Differential mode	$(V_{REF+}+V_{REF-})/2 - 0.18$	$(V_{REF+}+V_{REF-})/2$	$(V_{REF+}+V_{REF-})/2 + 0.18$	V
V_{AIN} (3)	Conversion voltage range(2)	-	0	-	V_{REF+}	V
R_{AIN}	External input impedance	-	-	-	50	kΩ
C_{ADC}	Internal sample and hold capacitor	-	-	5	-	pF
t_{STAB}	Power-up time	-	1			conversion cycle
t_{CAL}	Calibration time	f_{ADC} = 80 MHz	1.45			µs
		-	116			$1/f_{ADC}$

Table 73. OPAMP characteristics(1) (continued)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
GBW	Gain Bandwidth Product	Normal mode	V_{DDA} ≥ 2.4 V (OPA_RANGE = 1)	550	1600	2200	kHz
		Low-power mode		100	420	600	
		Normal mode	V_{DDA} < 2.4 V (OPA_RANGE = 0)	250	700	950	
		Low-power mode		40	180	280	
SR(3)	Slew rate (from 10 and 90% of output voltage)	Normal mode	V_{DDA} ≥ 2.4 V	-	700	-	V/ms
		Low-power mode		-	180	-	
		Normal mode	V_{DDA} < 2.4 V	-	300	-	
		Low-power mode		-	80	-	
AO	Open loop gain	Normal mode		55	110	-	dB
		Low-power mode		45	110	-	
V_{OHSAT}(3)	High saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at V_{DDA}.	V_{DDA} - 100	-	-	mV
		Low-power mode		V_{DDA} - 50	-	-	
V_{OLSAT}(3)	Low saturation voltage	Normal mode	I_{load} = max or R_{load} = min Input at 0.	-	-	100	
		Low-power mode		-	-	50	
φ_m	Phase margin	Normal mode		-	74	-	°
		Low-power mode		-	66	-	
GM	Gain margin	Normal mode		-	13	-	dB
		Low-power mode		-	20	-	
t_{WAKEUP}	Wake up time from OFF state.	Normal mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 4 kΩ follower configuration	-	5	10	µs
		Low-power mode	C_{LOAD} ≤ 50 pf, R_{LOAD} ≥ 20 kΩ follower configuration	-	10	30	
I_{bias}	OPAMP input bias current	General purpose input		-	-	-(4)	nA
PGA gain(3)	Non inverting gain value	-		-	2	-	-
				-	4	-	
				-	8	-	
				-	16	-	

Quad SPI characteristics

Unless otherwise specified, the parameters given in *Table 83* and *Table 84* for Quad SPI are derived from tests performed under the ambient temperature, f_{AHB} frequency and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 15 or 20 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

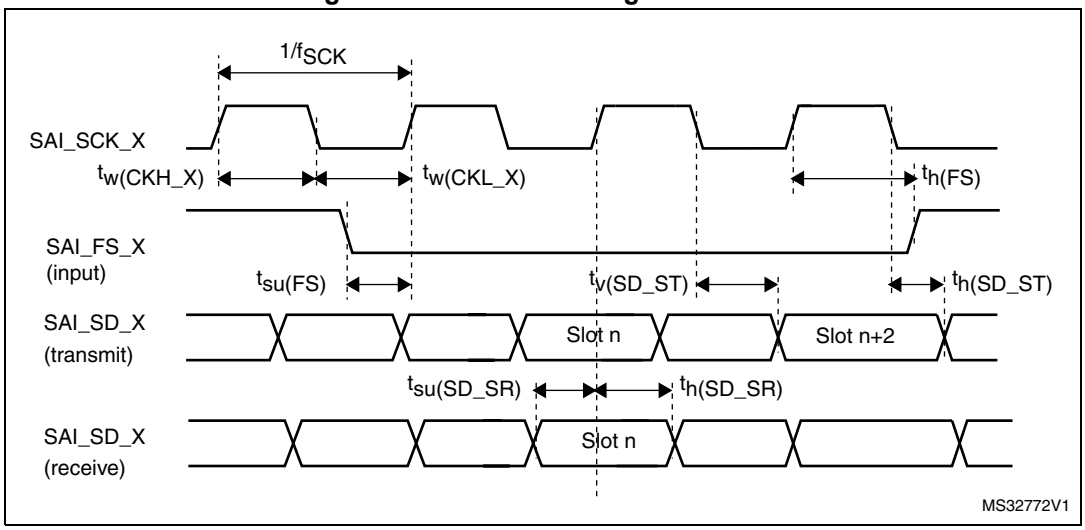
Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics.

Table 83. Quad SPI characteristics in SDR mode(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{CK} $1/t_{(CK)}$	Quad SPI clock frequency	1.71 < V_{DD}< 3.6 V, C_{LOAD} = 20 pF Voltage Range 1	-	-	40	MHz
		1.71 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	48	
		2.7 < V_{DD}< 3.6 V, C_{LOAD} = 15 pF Voltage Range 1	-	-	60	
		1.71 < V_{DD} < 3.6 V C_{LOAD} = 20 pF Voltage Range 2	-	-	26	
$t_{w(CKH)}$	Quad SPI clock high and low time	f_{AHBCLK}= 48 MHz, presc=0	$t_{(CK)}/2$-2	-	$t_{(CK)}/2$	ns
$t_{w(CKL)}$			$t_{(CK)}/2$	-	$t_{(CK)}/2$+2	
$t_{s(IN)}$	Data input setup time	Voltage Range 1	2	-	-	
		Voltage Range 2	3.5	-	-	
$t_{h(IN)}$	Data input hold time	Voltage Range 1	5	-	-	
		Voltage Range 2	6.5	-	-	
$t_{v(OUT)}$	Data output valid time	Voltage Range 1	-	1	5	
		Voltage Range 2	-	3	5	
$t_{h(OUT)}$	Data output hold time	Voltage Range 1	0	-	-	
		Voltage Range 2	0	-	-	

1. Guaranteed by characterization results.

Figure 38. SAI slave timing waveforms



SDMMC characteristics

Unless otherwise specified, the parameters given in *Table 86* for SDIO are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and V_{DD} supply voltage conditions summarized in *Table 20: General operating conditions*, with the following configuration:

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: 0.5 x V_{DD}

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output characteristics.

Table 86. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/fPCLK2 frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in MMC and SD HS mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	3.5	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	2.5	-	-	ns
CMD, D outputs (referenced to CK) in MMC and SD HS mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	12	13	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	10	-	-	ns
CMD, D inputs (referenced to CK) in SD default mode						
t_{ISUD}	Input setup time SD	f_{PP} = 50 MHz	3.5	-	-	ns
t_{IHD}	Input hold time SD	f_{PP} = 50 MHz	3	-	-	ns

Table 86. SD / MMC dynamic characteristics, V_{DD}=2.7 V to 3.6 V(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CMD, D outputs (referenced to CK) in SD default mode						
t_{OVD}	Output valid default time SD	f_{PP} = 50 MHz	-	2	3	ns
t_{OHD}	Output hold default time SD	f_{PP} = 50 MHz	0	-	-	ns

1. Guaranteed by characterization results.

Table 87. eMMC dynamic characteristics, V_{DD} = 1.71 V to 1.9 V(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	-	50	MHz
-	SDIO_CK/f_{PCLK2} frequency ratio	-	-	-	4/3	-
$t_{W(CKL)}$	Clock low time	f_{PP} = 50 MHz	8	10	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 50 MHz	8	10	-	ns
CMD, D inputs (referenced to CK) in eMMC mode						
t_{ISU}	Input setup time HS	f_{PP} = 50 MHz	0	-	-	ns
t_{IH}	Input hold time HS	f_{PP} = 50 MHz	1.5	-	-	ns
CMD, D outputs (referenced to CK) in eMMC mode						
t_{OV}	Output valid time HS	f_{PP} = 50 MHz	-	13.5	15	ns
t_{OH}	Output hold time HS	f_{PP} = 50 MHz	9	-	-	ns

1. Guaranteed by characterization results.
2. C_{LOAD} = 20pF.

Figure 39. SDIO high-speed mode

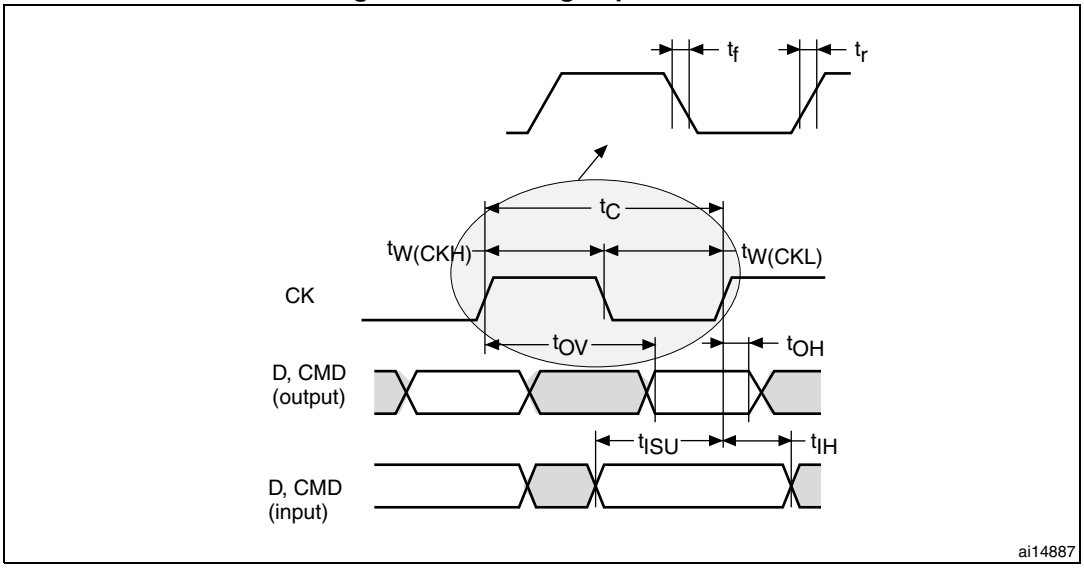


Table 91. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min.	Typ.	Max.	Min.	Typ.	Max.
e	-	0.500	-	-	0.0197	-
F	0.700	0.750	0.800	0.0276	0.0295	0.0315
ddd	-	-	0.100	-	-	0.0039
eee	-	-	0.150	-	-	0.0059
fff	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 45. UFBGA100 - 100-ball, 7 x 7 mm, 0.50 mm pitch, ultra fine pitch ball grid array package recommended footprint

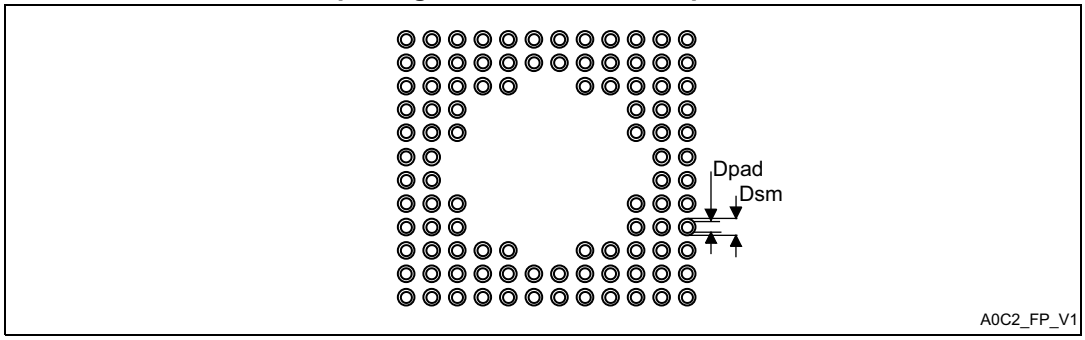


Table 92. UFBGA100 recommended PCB design rules (0.5 mm pitch BGA)

Dimension	Recommended values
Pitch	0.5
Dpad	0.280 mm
Dsm	0.370 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.280 mm
Stencil thickness	Between 0.100 mm and 0.125 mm

Device marking

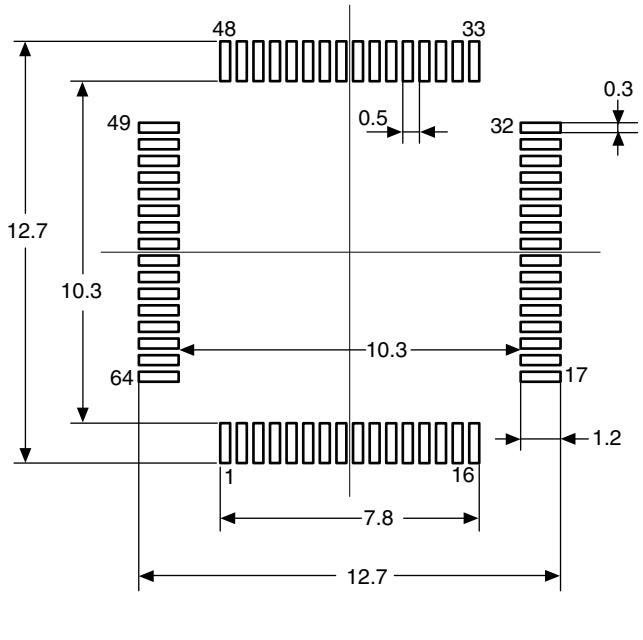
The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Table 93. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
E3	-	7.500	-	-	0.2953	-
e	-	0.500	-	-	0.0197	-
K	0°	3.5°	7°	0°	3.5°	7°
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 48. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package recommended footprint



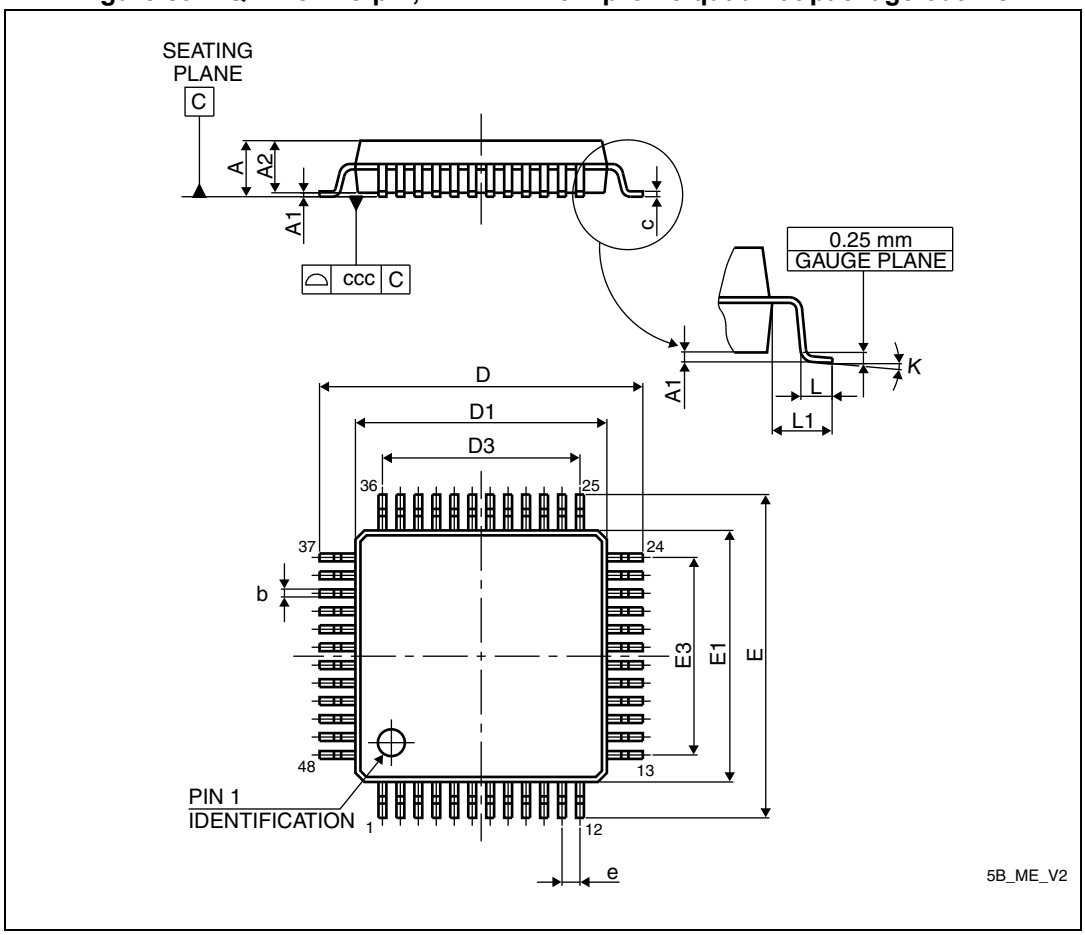
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

7.7 LQFP48 package information

Figure 59. LQFP48 - 48-pin, 7 x 7 mm low-profile quad flat package outline



1. Drawing is not to scale.

9 Revision history

Table 104. Document revision history

Date	Revision	Changes
08-Feb-2016	1	Initial release.
23-May-2016	2	Updated document title. Updated *Table 1: STM32L443xx family device features and peripheral counts*. Updated *Section 3.15.3: VBAT battery voltage monitoring*. Updated *Section 3.27: Universal synchronous/asynchronous receiver transmitter (USART)*. Updated *Table 13: STM32L443xx pin definitions*. Updated *Table 15: Alternate function AF8 to AF15 (for AF0 to AF7 see Table 14)*. Updated *Table 17: Voltage characteristics*. Updated *Table 20: General operating conditions*. Added *Figure 18: VREFINT versus temperature*. Updated *Table 22: Embedded reset and power control block characteristics*. Updated *Table 24* to *Table 26* and *Table 30* to *Table 39*. Updated *Table 39: Low-power mode wakeup timings*. Added *Table 41: Wakeup time using USART/LPUART*. Updated *Table 47: MSI oscillator characteristics*. Added *Table 48: HSI48 oscillator characteristics*. Added *Figure 25: HSI48 frequency versus temperature*. Updated *Table 50: PLL, PLLSAI1 characteristics*. Updated introduction of *Section 6.3.14: I/O port characteristics*. Added note to *Figure 28: Recommended NRST pin protection*. Updated *Table 62: Analog switches booster characteristics*. Updated *Table 63: ADC characteristics*. Updated *Table 71: VREFBUF characteristics*. Updated *Table 72: COMP characteristics*. Updated *Table 88: USB electrical characteristics*. Added *Section : SWPMI characteristics*. Updated *Table 102: Package thermal characteristics*.