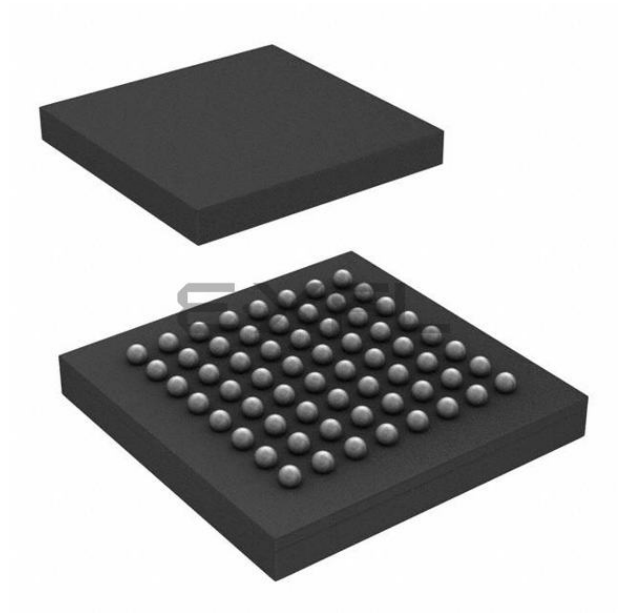

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

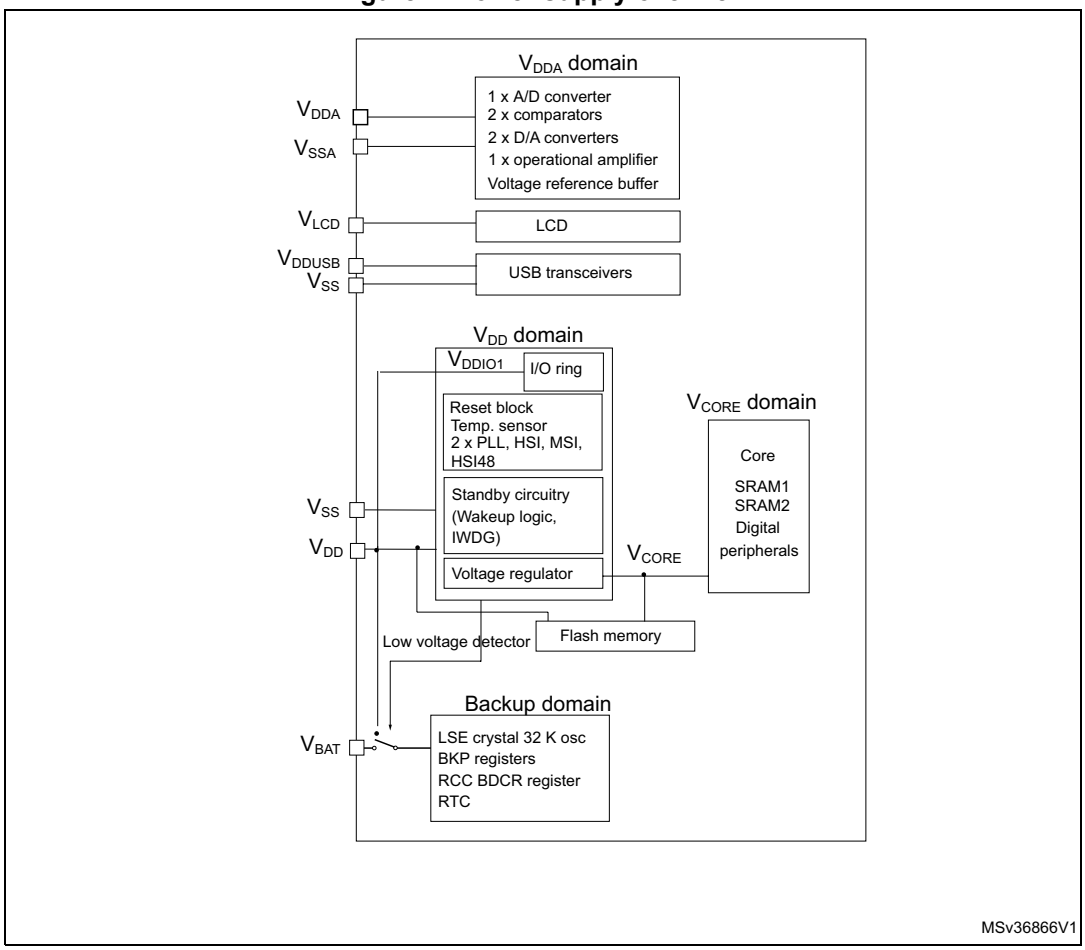
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.14x3.13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l443rci3

Note: If these supplies are tied to ground, the I/Os supplied by these power supplies are not 5 V tolerant (refer to Table 17: Voltage characteristics).

Note: V_{DDIOx} is the I/Os general purpose digital functions supply. V_{DDIOx} represents V_{DDIO1}, with $V_{DDIO1} = V_{DD}$.

Figure 2. Power supply overview



3.9.2 Power supply supervisor

The device has an integrated ultra-low-power brown-out reset (BOR) active in all modes except Shutdown and ensuring proper operation after power-on and during power down. The device remains in reset mode when the monitored supply voltage V_{DD} is below a specified threshold, without the need for an external reset circuit.

The lowest BOR level is 1.71V at power on, and other higher thresholds can be selected through option bytes.The device features an embedded programmable voltage detector (PVD) that monitors the V_{DD} power supply and compares it to the VPVD threshold. An interrupt can be generated when V_{DD} drops below the VPVD threshold and/or when V_{DD} is higher than the VPVD threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

In addition, the devices embed a Peripheral Voltage Monitor which compares the independent supply voltages V_{DDA}, V_{DDUSB} with a fixed threshold in order to ensure that the peripheral is in its functional supply range.

Table 3. Functionalities depending on the working mode(1) (continued)

Peripheral	Run	Sleep	Low-power run	Low-power sleep	Stop 0/1		Stop 2		Standby		Shutdown		VBAT
					-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	-	Wakeup capability	
CRC calculation unit	O	O	O	O	-	-	-	-	-	-	-	-	-
GPIOs	O	O	O	O	O	O	O	O	(9)	5 pins (10)	(11)	5 pins (10)	-

1. Legend: Y = Yes (Enable). O = Optional (Disable by default. Can be enabled by software). - = Not available.
2. The Flash can be configured in power-down mode. By default, it is not in power-down mode.
3. The SRAM clock can be gated on or off.
4. SRAM2 content is preserved when the bit RRS is set in PWR_CR3 register.
5. Some peripherals with wakeup from Stop capability can request HSI16 to be enabled. In this case, HSI16 is woken up by the peripheral, and only feeds the peripheral which requested it. HSI16 is automatically put off when the peripheral does not need it anymore.
6. UART and LPUART reception is functional in Stop mode, and generates a wakeup interrupt on Start, address match or received frame event.
7. I2C address detection is functional in Stop mode, and generates a wakeup interrupt in case of address match.
8. Voltage scaling Range 1 only.
9. I/Os can be configured with internal pull-up, pull-down or floating in Standby mode.
10. The I/Os with wakeup from Standby/Shutdown capability are: PA0, PC13, PE6, PA2, PC5.
11. I/Os can be configured with internal pull-up, pull-down or floating in Shutdown mode but the configuration is lost when exiting the Shutdown mode.

3.9.5 Reset mode

In order to improve the consumption under reset, the I/Os state under and after reset is “analog state” (the I/O schmitt trigger is disable). In addition, the internal reset pull-up is deactivated when the reset source is internal.

3.9.6 VBAT operation

The VBAT pin allows to power the device VBAT domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present. The VBAT pin supplies the RTC with LSE and the backup registers. Three anti-tamper detection pins are available in VBAT mode.

VBAT operation is automatically activated when V_{DD} is not present.

An internal VBAT battery charging circuit is embedded and can be activated when V_{DD} is present.

Note: When the microcontroller is supplied from VBAT, external interrupts and RTC alarm/events do not exit it from VBAT operation.

3.12 General-purpose inputs/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain), as input (with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. Fast I/O toggling can be achieved thanks to their mapping on the AHB2 bus.

The I/Os alternate function configuration can be locked if needed following a specific sequence in order to avoid spurious writing to the I/Os registers.

3.13 Direct memory access controller (DMA)

The device embeds 2 DMAs. Refer to *Table 5: DMA implementation* for the features implementation.

Direct memory access (DMA) is used in order to provide high-speed data transfer between peripherals and memory as well as memory to memory. Data can be quickly moved by DMA without any CPU actions. This keeps CPU resources free for other operations.

The two DMA controllers have 14 channels in total, each dedicated to managing memory access requests from one or more peripherals. Each has an arbiter for handling the priority between DMA requests.

The DMA supports:

- 14 independently configurable channels (requests)
- Each channel is connected to dedicated hardware DMA requests, software trigger is also supported on each channel. This configuration is done by software.
- Priorities between requests from channels of one DMA are software programmable (4 levels consisting of very high, high, medium, low) or hardware in case of equality (request 1 has priority over request 2, etc.)
- Independent source and destination transfer size (byte, half word, word), emulating packing and unpacking. Source/destination addresses must be aligned on the data size.
- Support for circular buffer management
- 3 event flags (DMA Half Transfer, DMA Transfer complete and DMA Transfer Error) logically ORed together in a single interrupt request for each channel
- Memory-to-memory transfer
- Peripheral-to-memory and memory-to-peripheral, and peripheral-to-peripheral transfers
- Access to Flash, SRAM, APB and AHB peripherals as source and destination
- Programmable number of data to be transferred: up to 65536.

Table 5. DMA implementation

DMA features	DMA1	DMA2
Number of regular channels	7	7

- Dual DAC channel independent or simultaneous conversions
- DMA capability for each channel
- External triggers for conversion
- Sample and hold low-power mode, with internal or external capacitor

The DAC channels are triggered through the timer update outputs that are also connected to different DMA channels.

3.17 Voltage reference buffer (VREFBUF)

The STM32L443xx devices embed an voltage reference buffer which can be used as voltage reference for ADCs, DACs and also as voltage reference for external components through the VREF+ pin.

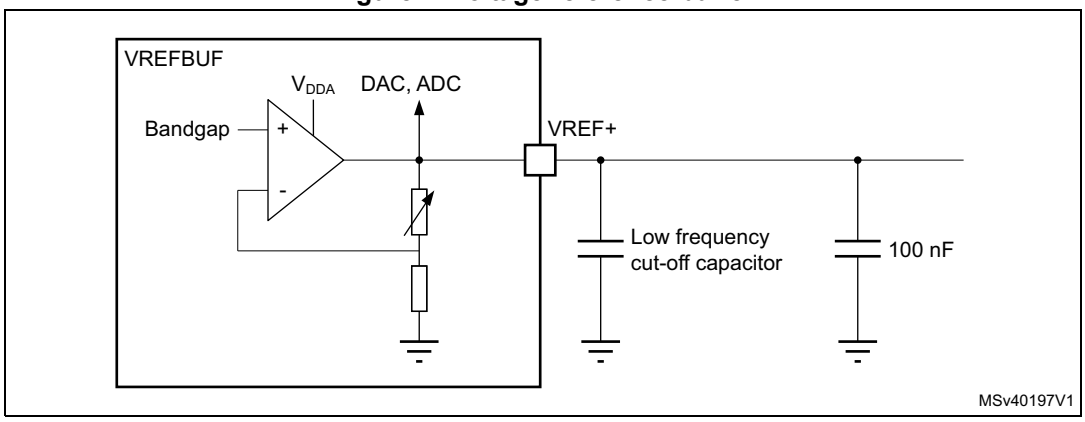
The internal voltage reference buffer supports two voltages:

- 2.048 V
- 2.5 V

An external voltage reference can be provided through the VREF+ pin when the internal voltage reference buffer is off.

The VREF+ pin is double-bonded with VDDA on some packages. In these packages the internal voltage reference buffer is not available.

Figure 4. Voltage reference buffer



3.18 Comparators (COMP)

The STM32L443xx devices embed two rail-to-rail comparators with programmable reference voltage (internal or external), hysteresis and speed (low speed for low-power) and with selectable output polarity.

The reference voltage can be one of the following:

- External I/O
- DAC output channels
- Internal reference voltage or submultiple (1/4, 1/2, 3/4).

All comparators can wake up from Stop mode, generate interrupts and breaks for the timers and can be also combined into a window comparator.

Table 11. SAI implementation

SAI features	Support[1]
I2S, LSB or MSB-justified, PCM/DSP, TDM, AC'97	X
Mute mode	X
Stereo/Mono audio frame capability.	X
16 slots	X
Data size configurable: 8-, 10-, 16-, 20-, 24-, 32-bit	X
FIFO Size	X (8 Word)
SPDIF	X

1. X: supported

3.31 Single wire protocol master interface (SWPMI)

The Single wire protocol master interface (SWPMI) is the master interface corresponding to the Contactless Frontend (CLF) defined in the ETSI TS 102 613 technical specification. The main features are:

- full-duplex communication mode
- automatic SWP bus state management (active, suspend, resume)
- configurable bitrate up to 2 Mbit/s
- automatic SOF, EOF and CRC handling

SWPMI can be served by the DMA controller.

3.32 Controller area network (CAN)

The CAN is compliant with specifications 2.0A and B (active) with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. It has three transmit mailboxes, two receive FIFOs with 3 stages and 14 scalable filter banks.

The CAN peripheral supports:

- Supports CAN protocol version 2.0 A, B Active
- Bit rates up to 1 Mbit/s

6.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, I/O pin loading, device software configuration, operating frequencies, I/O pin switching rate, program location in memory and executed binary code.

The current consumption is measured as described in *Figure 17: Current consumption measurement scheme*.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All I/O pins are in analog input mode
- All peripherals are disabled except when explicitly mentioned
- The Flash memory access time is adjusted with the minimum wait states number, depending on the f_{HCLK} frequency (refer to the table “Number of wait states according to CPU clock (HCLK) frequency” available in the RM0394 reference manual).
- When the peripherals are enabled $f_{PCLK} = f_{HCLK}$

The parameters given in *Table 24* to *Table 37* are derived from tests performed under ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 25. Current consumption in Run and Low-power run modes, code with data processing running from Flash, ART disable

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.66	2.68	2.73	2.81	2.96	3.0	3.1	3.2	3.3	3.6	mA
				16 MHz	1.88	1.9	1.94	2.02	2.17	2.1	2.2	2.3	2.4	2.7	
				8 MHz	1.05	1.06	1.11	1.18	1.33	1.2	1.2	1.3	1.4	1.7	
				4 MHz	0.6	0.62	0.66	0.73	0.87	0.7	0.7	0.8	0.9	1.2	
				2 MHz	0.36	0.37	0.34	0.48	0.62	0.4	0.4	0.5	0.6	0.9	
				1 MHz	0.23	0.25	0.25	0.36	0.5	0.3	0.3	0.4	0.5	0.8	
				100 kHz	0.12	0.14	0.17	0.25	0.39	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.56	8.61	8.69	8.79	8.97	9.6	9.7	9.8	10.0	10.3	
				72 MHz	7.74	7.79	7.86	7.96	8.14	8.7	8.7	8.8	9.0	9.4	
				64 MHz	7.63	7.68	7.75	7.85	8.04	8.6	8.6	8.7	8.9	9.3	
				48 MHz	6.36	6.4	6.48	6.58	6.76	7.2	7.3	7.4	7.6	7.9	
				32 MHz	4.56	4.6	4.66	4.76	4.93	5.2	5.2	5.3	5.5	5.8	
				24 MHz	3.45	3.48	3.54	3.64	3.8	3.9	4.0	4.1	4.2	4.6	
				16 MHz	2.48	2.51	2.56	2.65	2.82	2.8	2.9	3.0	3.1	3.5	
I_{DD}(LPRun)	Supply current in Low-power run	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	310	317	364	440	593	375.3	400.9	456.7	595.3	909.6	µA
				1 MHz	157	173	226	296	448	204.8	234.2	298.2	445.8	758.9	
				400 kHz	72.6	89	130	206	356	99.7	131.2	199.7	349.3	663.7	
				100 kHz	32.3	46	89.7	164	314	52.4	82.1	153.3	301.2	616.9	

1. Guaranteed by characterization results, unless otherwise specified.

Table 26. Current consumption in Run and Low-power run modes, code with data processing running from SRAM1

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Run)	Supply current in Run mode	$f_{HCLK} = f_{HSE}$ up to 48MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2	26 MHz	2.42	2.43	2.49	2.56	2.71	2.7	2.7	2.8	3.0	3.3	mA
				16 MHz	1.54	1.55	1.6	1.67	1.82	1.7	1.7	1.8	2.0	2.3	
				8 MHz	0.82	0.84	0.88	0.95	1.1	0.9	1.0	1.0	1.2	1.5	
				4 MHz	0.47	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				2 MHz	0.29	0.3	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				1 MHz	0.2	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				100 kHz	0.12	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	8.63	8.68	8.74	8.84	9.01	9.5	9.6	9.7	9.9	10.2	
				72 MHz	7.79	7.83	7.9	7.99	8.17	8.6	8.6	8.8	8.9	9.3	
				64 MHz	6.95	6.99	7.05	7.15	7.32	7.7	7.7	7.9	8.0	8.4	
				48 MHz	5.19	5.22	5.29	5.38	5.55	5.8	5.8	5.9	6.1	6.5	
				32 MHz	3.51	3.53	3.6	3.68	3.85	3.9	4.0	4.1	4.2	4.6	
				24 MHz	2.66	2.68	2.74	2.83	2.99	3.0	3.0	3.1	3.3	3.6	
				16 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.2	2.3	2.7	
I_{DD}(LPRun)	Supply current in low-power run mode	$f_{HCLK} = f_{MSI}$ all peripherals disable FLASH in power-down		2 MHz	205	228	275	352	501	276.5	302.3	358.4	502.5	816.4	µA
				1 MHz	111	126	175	248	397	151.3	180.9	245.3	390.7	703.4	
				400 kHz	49.2	62.7	108	181	330	73.3	104.0	170.8	321.0	632.4	
				100 kHz	21.5	33.3	76.6	151	299	36.4	67.7	137.2	287.8	600.8	

1. Guaranteed by characterization results, unless otherwise specified.

Table 37. Current consumption in VBAT mode

Symbol	Parameter	Conditions		TYP					MAX(1)					Unit
		-	V_{BAT}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(VBAT)	Backup domain supply current	RTC disabled	1.8 V	2	12	66	193	540	5	30	165	482	1350	nA
			2.4 V	1	12	73	217	600	6	30	182	542	1500	
			3 V	5	16	92	266	731	12.5	40	230	665	1928	
			3.6 V	6	30	161	459	1 269	15	75	402	1147	3173	
		RTC enabled and clocked by LSE bypassed at 32768 Hz	1.8 V	154	175	247	430	-	-	-	-	-	-	
			2.4 V	228	246	335	542	-	-	-	-	-	-	
			3 V	316	340	459	714	-	-	-	-	-	-	
			3.6 V	419	462	684	1 140	-	-	-	-	-	-	
		RTC enabled and clocked by LSE quartz(2)	1.8 V	256	297	385	558	823	-	-	-	-	-	
			2.4 V	345	381	477	673	906	-	-	-	-	-	
			3 V	455	495	603	836	1 085	-	-	-	-	-	
			3.6 V	591	642	824	1 207	1 733	-	-	-	-	-	

1. Guaranteed by characterization results, unless otherwise specified.
2. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 38*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 17: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 38*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 38. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	3.2	2.9	3.1	µA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	AES	1.7	1.5	1.6	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA(2)	1.7	1.4	1.6	
	GPIOB(2))	1.6	1.3	1.6	
	GPIOC(2)	1.7	1.5	1.6	
	GPIOD(2)	1.8	1.6	1.7	
	GPIOE(2)	1.7	1.6	1.6	
	GPIOH(2)	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	NA	NA	
	RNG clock domain	0.5	NA	NA	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge(3)	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. HSE oscillator characteristics(1)

Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup(3)	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$(4)	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.
2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.
3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time
4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Output voltage levels

Unless otherwise specified, the parameters given in the table below are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*. All I/Os are CMOS- and TTL-compliant (FT OR TT unless otherwise specified).

Table 59. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		V_{DDIOx}-0.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	TTL port(2) $\|I_{IO}\|$ = 8 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
V_{OH}(3)	Output high level voltage for an I/O pin		2.4	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	1.3	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-1.3	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 4 mA $V_{DDIOx} \geq 1.62$ V	-	0.45	
V_{OH}(3)	Output high level voltage for an I/O pin		V_{DDIOx}-0.45	-	
V_{OL}(3)	Output low level voltage for an I/O pin	$\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx} \geq$ 1.08 V	-	$0.35_x V_{DDIOx}$	
V_{OH}(3)	Output high level voltage for an I/O pin		$0.65_x V_{DDIOx}$	-	
V_{OLFM+}(3)	Output low level voltage for an FT I/O pin in FM+ mode (FT I/O with "f" option)	$\|I_{IO}\|$ = 20 mA $V_{DDIOx} \geq 2.7$ V	-	0.4	
		$\|I_{IO}\|$ = 10 mA $V_{DDIOx} \geq 1.62$ V	-	0.4	
		$\|I_{IO}\|$ = 2 mA 1.62 V ≥ $V_{DDIOx} \geq$ 1.08 V	-	0.4	

1. The I_{IO} current sourced or sunk by the device must always respect the absolute maximum rating specified in *Table 17: Voltage characteristics*, and the sum of the currents sourced or sunk by all the I/Os (I/O ports and control pins) must always respect the absolute maximum ratings ΣI_{IO}.
2. TTL and CMOS outputs are compatible with JEDEC standards JESD36 and JESD52.
3. Guaranteed by design.

Input/output AC characteristics

The definition and values of input/output AC characteristics are given in *Figure 27* and *Table 60*, respectively.

Unless otherwise specified, the parameters given are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 60. I/O AC characteristics(1)(2)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
00	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	10	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	1.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	0.1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	52	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	140	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	17	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	110	
01	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	25	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	10	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	15	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	1	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	9	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	16	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	40	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	4.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	9	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	21	

Table 65. ADC accuracy - limited test conditions 1(1)(2)(3) (continued)

Symbol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, $V_{DDA} = V_{REF+} = 3$ V, TA = 25 °C	Single ended	Fast channel (max speed)	-	-74	-73	dB
				Slow channel (max speed)	-	-74	-73	
			Differential	Fast channel (max speed)	-	-79	-76	
				Slow channel (max speed)	-	-79	-76	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when $V_{DDA} < 2.4$ V (BOOSTEN = 1 in the SYSCFG_CFGR1 when $V_{DDA} < 2.4$ V). It is disable when $V_{DDA} \geq 2.4$ V. No oversampling.

Table 67. ADC accuracy - limited test conditions 3(1)(2)(3)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	5.5	7.5	LSB
				Slow channel (max speed)	-	4.5	6.5	
			Differential	Fast channel (max speed)	-	4.5	7.5	
				Slow channel (max speed)	-	4.5	5.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	2	5	
				Slow channel (max speed)	-	2.5	5	
			Differential	Fast channel (max speed)	-	2	3.5	
				Slow channel (max speed)	-	2.5	3	
EG	Gain error		Single ended	Fast channel (max speed)	-	4.5	7	
				Slow channel (max speed)	-	3.5	6	
			Differential	Fast channel (max speed)	-	3.5	4	
				Slow channel (max speed)	-	3.5	5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1.2	1.5	
				Slow channel (max speed)	-	1.2	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	3	3.5	
				Slow channel (max speed)	-	2.5	3.5	
			Differential	Fast channel (max speed)	-	2	2.5	
				Slow channel (max speed)	-	2	2.5	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10	10.4	-	bits
				Slow channel (max speed)	10	10.4	-	
			Differential	Fast channel (max speed)	10.6	10.7	-	
				Slow channel (max speed)	10.6	10.7	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	62	64	-	dB
				Slow channel (max speed)	62	64	-	
			Differential	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	63	65	-	
				Slow channel (max speed)	63	65	-	
			Differential	Fast channel (max speed)	66	67	-	
				Slow channel (max speed)	66	67	-	

Table 67. ADC accuracy - limited test conditions 3(1)(2)(3) (continued)

Sym-bol	Parameter	Conditions(4)			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.
2. ADC DC accuracy values are measured after internal calibration.
3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.
4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

6.3.19 Voltage reference buffer characteristics

Table 71. VREFBUF characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	Normal mode	V_{RS} = 0	2.4	-	3.6	V
			V_{RS} = 1	2.8	-	3.6	
		Degraded mode(2)	V_{RS} = 0	1.65	-	2.4	
			V_{RS} = 1	1.65	-	2.8	
V_{REFBUF_OUT}	Voltage reference output	Normal mode	V_{RS} = 0	2.046(3)	2.048	2.049(3)	
			V_{RS} = 1	2.498(3)	2.5	2.502(3)	
		Degraded mode(2)	V_{RS} = 0	V_{DDA}-150 mV	-	V_{DDA}	
			V_{RS} = 1	V_{DDA}-150 mV	-	V_{DDA}	
TRIM	Trim step resolution	-	-	-	±0.05	±0.1	%
CL	Load capacitor	-	-	0.5	1	1.5	µF
esr	Equivalent Serial Resistor of Cload	-	-	-	-	2	Ω
I_{load}	Static load current	-	-	-	-	4	mA
I_{line_reg}	Line regulation	2.8 V ≤ V_{DDA} ≤ 3.6 V	I_{load} = 500 µA	-	200	1000	ppm/V
			I_{load} = 4 mA	-	100	500	
I_{load_reg}	Load regulation	500 µA ≤ I_{load} ≤4 mA	Normal mode	-	50	500	ppm/mA
T_{Coeff}	Temperature coefficient	-40 °C < T_J < +125 °C		-	-	$T_{coeff\_vrefint}$ + 50	ppm/ °C
		0 °C < T_J < +50 °C		-	-	$T_{coeff\_vrefint}$ + 50	
PSRR	Power supply rejection	DC		40	60	-	dB
		100 kHz		25	40	-	
t_{START}	Start-up time	CL = 0.5 µF(4)		-	300	350	µs
		CL = 1.1 µF(4)		-	500	650	
		CL = 1.5 µF(4)		-	650	800	
I_{INRUSH}	Control of maximum DC current drive on VREFBUF_OUT during start-up phase (5)	-	-	-	8	-	mA

Table 71. VREFBUF characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.
2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).
3. Guaranteed by test in production.
4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.
5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.20 Comparator characteristics

Table 72. COMP characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range	-		0	-	V_{DDA}	V
V_{BG}(2)	Scaler input voltage	-		V_{REFINT}			V
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D(3)	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.

Table 90. LQPF100 - 100-pin, 14 x 14 mm low-profile quad flat package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	15.800	16.000	16.200	0.6220	0.6299	0.6378
D1	13.800	14.000	14.200	0.5433	0.5512	0.5591
D3	-	12.000	-	-	0.4724	-
E	15.800	16.000	16.200	0.6220	0.6299	0.6378
E1	13.800	14.000	14.200	0.5433	0.5512	0.5591
E3	-	12.000	-	-	0.4724	-
e	-	0.500	-	-	0.0197	-
L	0.450	0.600	0.750	0.0177	0.0236	0.0295
L1	-	1.000	-	-	0.0394	-
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.