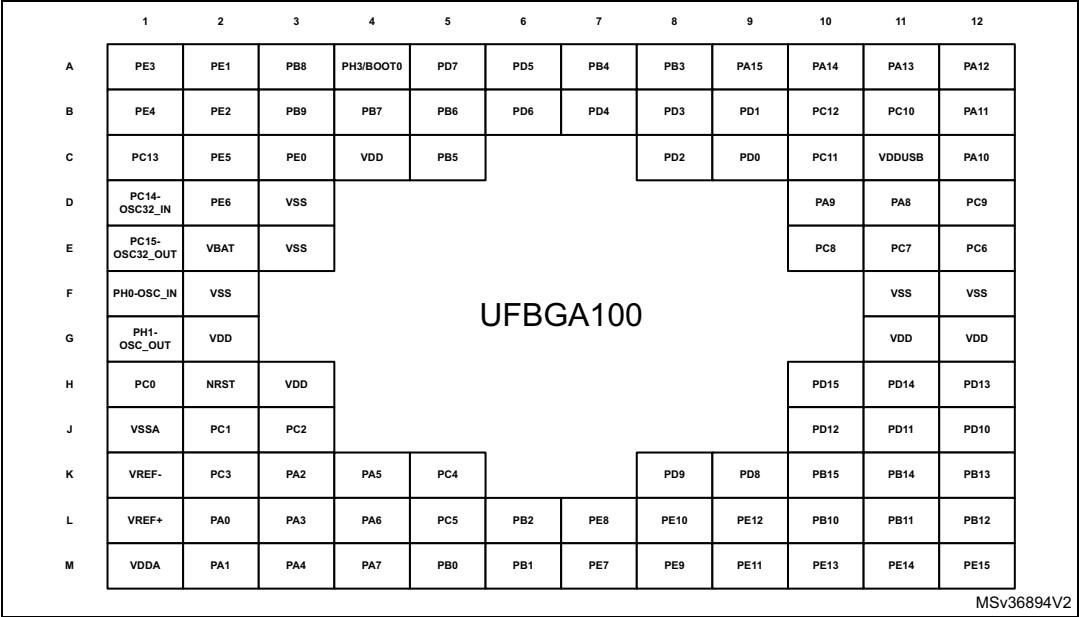**What is "Embedded - Microcontrollers"?**

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

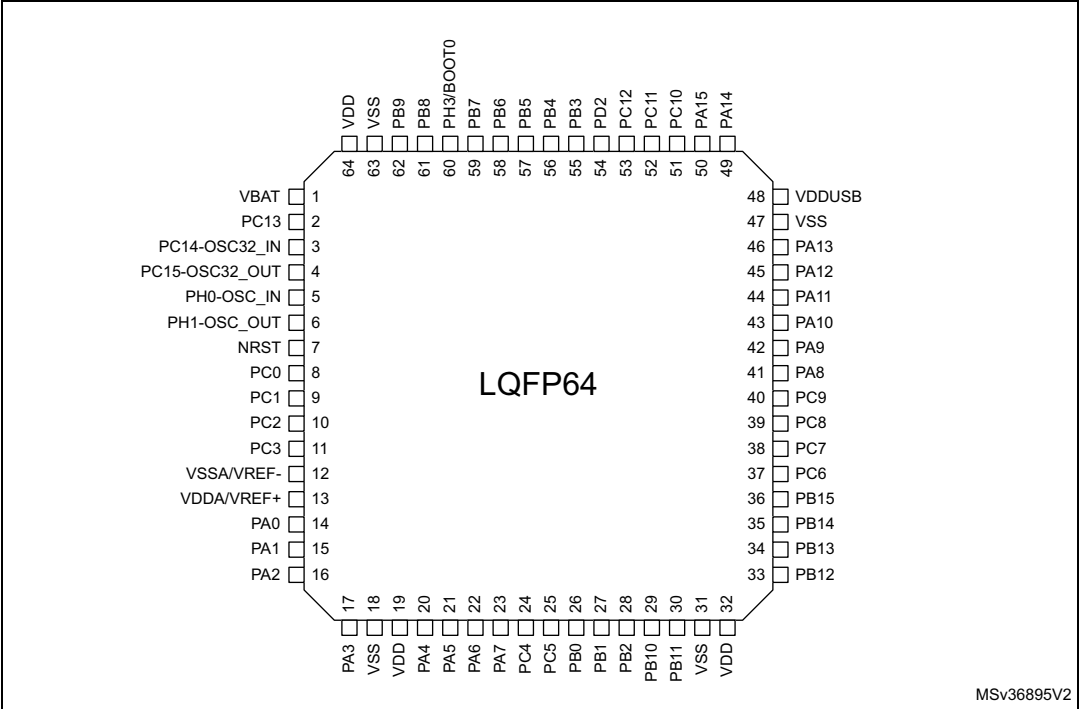**Applications of "Embedded - Microcontrollers"**

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l443rct6

Figure 6. STM32L443Vx UFBGA100 ballout[1]

	1	2	3	4	5	6	7	8	9	10	11	12
A	PE3	PE1	PB8	PH3/BOOT0	PD7	PD5	PB4	PB3	PA15	PA14	PA13	PA12
B	PE4	PE2	PB9	PB7	PB6	PD6	PD4	PD3	PD1	PC12	PC10	PA11
C	PC13	PE5	PE0	VDD	PB5			PD2	PD0	PC11	VDDUSB	PA10
D	PC14-OSC32_IN	PE6	VSS							PA9	PA8	PC9
E	PC15-OSC32_OUT	VBAT	VSS							PC8	PC7	PC6
F	PH0-OSC_IN	VSS									VSS	VSS
G	PH1-OSC_OUT	VDD									VDD	VDD
H	PC0	NRST	VDD							PD15	PD14	PD13
J	VSSA	PC1	PC2							PD12	PD11	PD10
K	VREF-	PC3	PA2	PA5	PC4			PD9	PD8	PB15	PB14	PB13
L	VREF+	PA0	PA3	PA6	PC5	PB2	PE8	PE10	PE12	PB10	PB11	PB12
M	VDDA	PA1	PA4	PA7	PB0	PB1	PE7	PE9	PE11	PE13	PE14	PE15

MSv36894V2

1. The above figure shows the package top view.

Figure 7. STM32L443Rx LQFP64 pinout[1]

1. The above figure shows the package top view.

Table 13. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					**Alternate functions**	**Additional functions**
25	25	F1	G3	33	H8	51	L12	PB12	I/O	FT_I	-	TIM1_BKIN, TIM1_BKIN_COMP2, I2C2_SMBA, SPI2_NSS, USART3_CK, LPUART1_RTS_DE, TSC_G1_IO1, LCD_SEG12, SWPMI1_IO, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-
26	26	E2	G2	34	G8	52	K12	PB13	I/O	FT_fl	-	TIM1_CH1N, I2C2_SCL, SPI2_SCK, USART3_CTS, LPUART1_CTS, TSC_G1_IO2, LCD_SEG13, SWPMI1_TX, SAI1_SCK_A, TIM15_CH1N, EVENTOUT	-
27	27	E1	G1	35	F8	53	K11	PB14	I/O	FT_fl	-	TIM1_CH2N, I2C2_SDA, SPI2_MISO, USART3_RTS_DE, TSC_G1_IO3, LCD_SEG14, SWPMI1_RX, SAI1_MCLK_A, TIM15_CH1, EVENTOUT	-
28	28	D3	F2	36	F7	54	K10	PB15	I/O	FT_I	-	RTC_REFIN, TIM1_CH3N, SPI2_MOSI, TSC_G1_IO4, LCD_SEG15, SWPMI1_SUSPEND, SAI1_SD_A, TIM15_CH2, EVENTOUT	-
-	-	-	-	-	-	55	K9	PD8	I/O	FT_I	-	USART3_TX, LCD_SEG28, EVENTOUT	-
-	-	-	-	-	-	56	K8	PD9	I/O	FT_I	-	USART3_RX, LCD_SEG29, EVENTOUT	-
-	-	-	-	-	-	57	J12	PD10	I/O	FT_I	-	USART3_CK, TSC_G6_IO1, LCD_SEG30, EVENTOUT	-

Table 14. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 15*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port D	PD0	-	-	-	-	-	SPI2_NSS	-	-
	PD1	-	-	-	-	-	SPI2_SCK	-	-
	PD2	-	-	-	-	-	-	-	USART3_RTS_DE
	PD3	-	-	-	-	-	SPI2_MISO	-	USART2_CTS
	PD4	-	-	-	-	-	SPI2_MOSI	-	USART2_RTS_DE
	PD5	-	-	-	-	-	-	-	USART2_TX
	PD6	-	-	-	-	-	-	-	USART2_RX
	PD7	-	-	-	-	-	-	-	USART2_CK
	PD8	-	-	-	-	-	-	-	USART3_TX
	PD9	-	-	-	-	-	-	-	USART3_RX
	PD10	-	-	-	-	-	-	-	USART3_CK
	PD11	-	-	-	-	-	-	-	USART3_CTS
	PD12	-	-	-	-	-	-	-	USART3_RTS_DE
	PD13	-	-	-	-	-	-	-	-
	PD14	-	-	-	-	-	-	-	-
	PD15	-	-	-	-	-	-	-	-
Port E	PE0	-	-	-	-	-	-	-	-

Table 14. Alternate function AF0 to AF7 (for AF8 to AF15 see *Table 15*) (continued)

Port		AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
		SYS_AF	TIM1/TIM2/ LPTIM1	TIM1/TIM2	USART2	I2C1/I2C2/I2C3	SPI1/SPI2	SPI3	USART1/ USART2/ USART3
Port E	PE1	-	-	-	-	-	-	-	-
	PE2	TRACECK	-	-	-	-	-	-	-
	PE3	TRACED0	-	-	-	-	-	-	-
	PE4	TRACED1	-	-	-	-	-	-	-
	PE5	TRACED2	-	-	-	-	-	-	-
	PE6	TRACED3	-	-	-	-	-	-	-
	PE7	-	TIM1_ETR	-	-	-	-	-	-
	PE8	-	TIM1_CH1N	-	-	-	-	-	-
	PE9	-	TIM1_CH1	-	-	-	-	-	-
	PE10	-	TIM1_CH2N	-	-	-	-	-	-
	PE11	-	TIM1_CH2	-	-	-	-	-	-
	PE12	-	TIM1_CH3N	-	-	-	SPI1_NSS	-	-
	PE13	-	TIM1_CH3	-	-	-	SPI1_SCK	-	-
	PE14	-	TIM1_CH4	TIM1_BKIN2	TIM1_BKIN2_ COMP2	-	SPI1_MISO	-	-
	PE15	-	TIM1_BKIN	-	TIM1_BKIN_ COMP1	-	SPI1_MOSI	-	-
Port H	PH0	-	-	-	-	-	-	-	-
	PH1	-	-	-	-	-	-	-	-
	PH3	-	-	-	-	-	-	-	-

Table 20. General operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
T_A	Ambient temperature for the suffix 6 version	Maximum power dissipation	–40	85	°C
		Low-power dissipation[5]	–40	105	
	Ambient temperature for the suffix 7 version	Maximum power dissipation	–40	105	
		Low-power dissipation[5]	–40	125	
	Ambient temperature for the suffix 3 version	Maximum power dissipation	–40	125	
		Low-power dissipation[5]	–40	130	
T_J	Junction temperature range	Suffix 6 version	–40	105	°C
		Suffix 7 version	–40	125	
		Suffix 3 version	–40	130	

1. When RESET is released functionality is guaranteed down to V_{BOR0} Min.

2. This formula has to be applied only on the power supplies related to the IO structure described by the pin definition table. Maximum I/O input voltage is the smallest value between MIN(V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD})+3.6 V and 5.5V.

3. For operation with voltage higher than Min (V_{DD}, V_{DDA}, V_{DDUSB}, V_{LCD}) +0.3 V, the internal Pull-up and Pull-Down resistors must be disabled.

4. If T_A is lower, higher P_D values are allowed as long as T_J does not exceed T_{Jmax} (see *Section 7.9: Thermal characteristics*).

5. In low-power dissipation state, T_A can be extended to this range as long as T_J does not exceed T_{Jmax} (see *Section 7.9: Thermal characteristics*).

6.3.2 Operating conditions at power-up / power-down

The parameters given in *Table 21* are derived from tests performed under the ambient temperature condition summarized in *Table 20*.

Table 21. Operating conditions at power-up / power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞	µs/V
	V_{DD} fall time rate		10	∞	
t_{VDDA}	V_{DDA} rise time rate	-	0	∞	
	V_{DDA} fall time rate		10	∞	
t_{VDDUSB}	V_{DDUSB} rise time rate	-	0	∞	
	V_{DDUSB} fall time rate		10	∞	

6.3.3 Embedded reset and power control block characteristics

The parameters given in *Table 22* are derived from tests performed under the ambient temperature conditions summarized in *Table 20: General operating conditions*.

Table 22. Embedded reset and power control block characteristics (continued)

Symbol	Parameter	Conditions[1]	Min	Typ	Max	Unit
V_{PVM3}	V_{DDA} peripheral voltage monitoring	Rising edge	1.61	1.65	1.69	V
		Falling edge	1.6	1.64	1.68	
V_{PVM4}	V_{DDA} peripheral voltage monitoring	Rising edge	1.78	1.82	1.86	V
		Falling edge	1.77	1.81	1.85	
V_{hyst_PVM3}	PVM3 hysteresis	-	-	10	-	mV
V_{hyst_PVM4}	PVM4 hysteresis	-	-	10	-	mV
I_{DD} (PVM1) [2]	PVM1 consumption from V_{DD}	-	-	0.2	-	µA
I_{DD} (PVM3/PVM4) [2]	PVM3 and PVM4 consumption from V_{DD}	-	-	2	-	µA

1. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

2. Guaranteed by design.

3. BOR0 is enabled in all modes (except shutdown) and its consumption is therefore included in the supply current characteristics tables.

Table 28. Typical current consumption in Run and Low-power run modes, with different codes running from Flash, ART disable

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code[1]	2.66	mA	102	µA/MHz
				Coremark	2.44		94	
				Dhrystone 2.1	2.46		95	
				Fibonacci	2.27		87	
				While(1)	2.20		84.6	
			Range 1 f_{HCLK} = 80 MHz	Reduced code[1]	8.56	mA	107	µA/MHz
				Coremark	8.00		100	
				Dhrystone 2.1	7.98		100	
				Fibonacci	7.41		93	
				While(1)	7.83		98	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code[1]	310	µA	155	µA/MHz
				Coremark	342		171	
				Dhrystone 2.1	324		162	
				Fibonacci	324		162	
				While(1)	384		192	

1. Reduced code used for characterization results provided in *Table 24*, *Table 25*, *Table 26*.

Table 29. Typical current consumption in Run and Low-power run modes, with different codes running from SRAM1

Symbol	Parameter	Conditions			TYP	Unit	TYP	Unit
		-	Voltage scaling	Code	25 °C		25 °C	
I_{DD}(Run)	Supply current in Run mode	f_{HCLK} = f_{HSE} up to 48 MHz included, bypass mode PLL ON above 48 MHz all peripherals disable	Range 2 f_{HCLK} = 26 MHz	Reduced code[1]	2.42	mA	93	µA/MHz
				Coremark	2.18		84	
				Dhrystone 2.1	2.40		92	
				Fibonacci	2.40		92	
				While(1)	2.29		88	
			Range 1 f_{HCLK} = 80 MHz	Reduced code[1]	8.63	mA	108	µA/MHz
				Coremark	7.76		97	
				Dhrystone 2.1	8.55		107	
				Fibonacci	8.56		107	
				While(1)	8.12		102	
I_{DD}(LPRun)	Supply current in Low-power run	f_{HCLK} = f_{MSI} = 2 MHz all peripherals disable		Reduced code[1]	205	µA	103	µA/MHz
				Coremark	188		94	
				Dhrystone 2.1	222		111	
				Fibonacci	204		102	
				While(1)	211		106	

1. Reduced code used for characterization results provided in *Table 24*, *Table 25*, *Table 26*.

High-speed external clock generated from a crystal/ceramic resonator

The high-speed external (HSE) clock can be supplied with a 4 to 48 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 44*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 44. HSE oscillator characteristics[1]

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
f_{OSC_IN}	Oscillator frequency	-	4	8	48	MHz
R_F	Feedback resistor	-	-	200	-	kΩ
$I_{DD(HSE)}$	HSE current consumption	During startup[3]	-	-	5.5	mA
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@8 MHz	-	0.44	-	
		V_{DD} = 3 V, Rm = 45 Ω, CL = 10 pF@8 MHz	-	0.45	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 5 pF@48 MHz	-	0.68	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 10 pF@48 MHz	-	0.94	-	
		V_{DD} = 3 V, Rm = 30 Ω, CL = 20 pF@48 MHz	-	1.77	-	
G_m	Maximum critical crystal transconductance	Startup	-	-	1.5	mA/V
$t_{SU(HSE)}$[4]	Startup time	V_{DD} is stabilized	-	2	-	ms

1. Guaranteed by design.

2. Resonator characteristics given by the crystal/ceramic resonator manufacturer.

3. This consumption level occurs during the first 2/3 of the $t_{SU(HSE)}$ startup time

4. $t_{SU(HSE)}$ is the startup time measured from the moment it is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 20 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator (see *Figure 21*). C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Note: *For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.*

Figure 21. Typical application with an 8 MHz crystal

MS19876V1
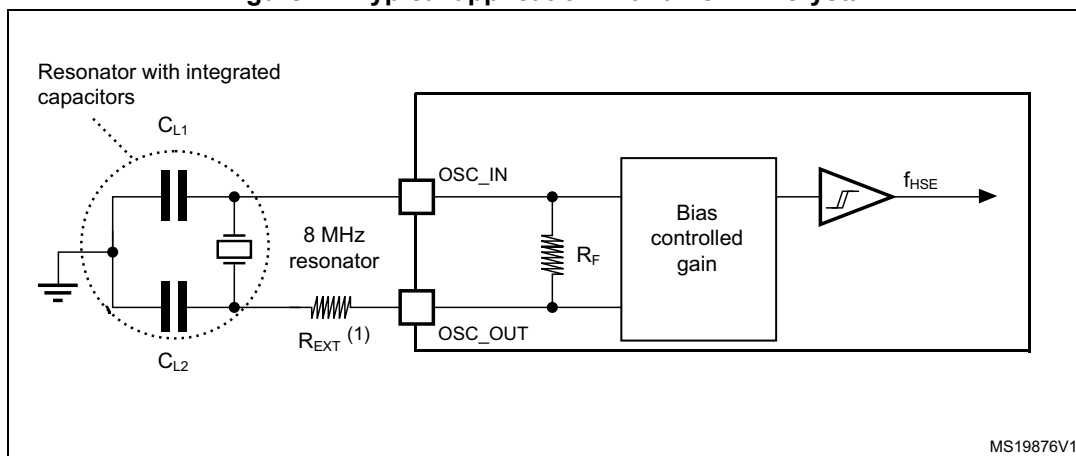
1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 45. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)[1]

Symbol	Parameter	Conditions[2]	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$[3]	Startup time	V_{DD} is stabilized	-	2	-	s

6.3.10　Flash memory characteristics

Table 51. Flash memory characteristics[1]

Symbol	Parameter	Conditions	Typ	Max	Unit
t_{prog}	64-bit programming time	-	81.69	90.76	μs
t_{prog_row}	one row (32 double word) programming time	normal programming	2.61	2.90	ms
		fast programming	1.91	2.12	
t_{prog_page}	one page (2 Kbyte) programming time	normal programming	20.91	23.24	ms
		fast programming	15.29	16.98	
t_{ERASE}	Page (2 KB) erase time	-	22.02	24.47	
t_{prog_bank}	one bank (512 Kbyte) programming time	normal programming	5.35	5.95	s
		fast programming	3.91	4.35	
t_{ME}	Mass erase time (one or two banks)	-	22.13	24.59	ms
I_{DD}	Average consumption from V_{DD}	Write mode	3.4	-	mA
		Erase mode	3.4	-	
	Maximum current (peak)	Write mode	7 (for 2 μs)	-	
		Erase mode	7 (for 41 μs)	-	

1. Guaranteed by design.

Table 52. Flash memory endurance and data retention

Symbol	Parameter	Conditions	Min[1]	Unit
N_{END}	Endurance	T_A = –40 to +105 °C	10	kcycles
t_{RET}	Data retention	1 kcycle[2] at T_A = 85 °C	30	Years
		1 kcycle[2] at T_A = 105 °C	15	
		1 kcycle[2] at T_A = 125 °C	7	
		10 kcycles[2] at T_A = 55 °C	30	
		10 kcycles[2] at T_A = 85 °C	15	
		10 kcycles[2] at T_A = 105 °C	10	

1. Guaranteed by characterization results.

2. Cycling performed over the whole temperature range.

Prequalification trials

Most of the common failures (unexpected reset and program counter corruption) can be reproduced by manually forcing a low state on the NRST pin or the Oscillator pins for 1 second.

To complete these trials, ESD stress can be applied directly on the device, over the range of specification values. When unexpected behavior is detected, the software can be hardened to prevent unrecoverable errors occurring (see application note AN1015).

Electromagnetic Interference (EMI)

The electromagnetic field emitted by the device are monitored while a simple application is executed (toggling 2 LEDs through the I/O ports). This emission test is compliant with IEC 61967-2 standard which specifies the test board and the pin loading.

Table 54. EMI characteristics

Symbol	Parameter	Conditions	Monitored frequency band	Max vs. [f_{HSE}/f_{HCLK}] 8 MHz/ 80 MHz	Unit
S_{EMI}	Peak level	V_{DD} = 3.6 V, T_A = 25 °C, LQFP100 package compliant with IEC 61967-2	0.1 MHz to 30 MHz	-8	dBµV
			30 MHz to 130 MHz	2	
			130 MHz to 1 GHz	5	
			1 GHz to 2 GHz	8	
			EMI Level	2.5	-

6.3.12 Electrical sensitivity characteristics

Based on three different tests (ESD, LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × (n+1) supply pins). This test conforms to the ANSI/JEDEC standard.

Table 55. ESD absolute maximum ratings

Symbol	Ratings	Conditions	Class	Maximum value[1]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforming to ANSI/ESDA/JEDEC JS-001	2	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforming to ANSI/ESD STM5.3.1	C3	250	

1. Guaranteed by characterization results.

Table 65. ADC accuracy - limited test conditions 1[(1)(2)(3)]

Sym-bol	Parameter	Conditions[(4)]			Min	Typ	Max	Unit
ET	Total unadjusted error	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, V_{DDA} = VREF+ = 3 V, TA = 25 °C	Single ended	Fast channel (max speed)	-	4	5	LSB
				Slow channel (max speed)	-	4	5	
			Differential	Fast channel (max speed)	-	3.5	4.5	
				Slow channel (max speed)	-	3.5	4.5	
EO	Offset error		Single ended	Fast channel (max speed)	-	1	2.5	
				Slow channel (max speed)	-	1	2.5	
			Differential	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
EG	Gain error		Single ended	Fast channel (max speed)	-	2.5	4.5	
				Slow channel (max speed)	-	2.5	4.5	
			Differential	Fast channel (max speed)	-	2.5	3.5	
				Slow channel (max speed)	-	2.5	3.5	
ED	Differential linearity error		Single ended	Fast channel (max speed)	-	1	1.5	
				Slow channel (max speed)	-	1	1.5	
			Differential	Fast channel (max speed)	-	1	1.2	
				Slow channel (max speed)	-	1	1.2	
EL	Integral linearity error		Single ended	Fast channel (max speed)	-	1.5	2.5	
				Slow channel (max speed)	-	1.5	2.5	
			Differential	Fast channel (max speed)	-	1	2	
				Slow channel (max speed)	-	1	2	
ENOB	Effective number of bits		Single ended	Fast channel (max speed)	10.4	10.5	-	bits
				Slow channel (max speed)	10.4	10.5	-	
			Differential	Fast channel (max speed)	10.8	10.9	-	
				Slow channel (max speed)	10.8	10.9	-	
SINAD	Signal-to-noise and distortion ratio		Single ended	Fast channel (max speed)	64.4	65	-	dB
				Slow channel (max speed)	64.4	65	-	
			Differential	Fast channel (max speed)	66.8	67.4	-	
				Slow channel (max speed)	66.8	67.4	-	
SNR	Signal-to-noise ratio		Single ended	Fast channel (max speed)	65	66	-	
				Slow channel (max speed)	65	66	-	
			Differential	Fast channel (max speed)	67	68	-	
				Slow channel (max speed)	67	68	-	

Table 67. ADC accuracy - limited test conditions 3[1][2][3] (continued)

Sym-bol	Parameter	Conditions[4]			Min	Typ	Max	Unit
THD	Total harmonic distortion	ADC clock frequency ≤ 80 MHz, Sampling rate ≤ 5.33 Msps, 1.65 V ≤ V_{DDA} = V_{REF+} ≤ 3.6 V, Voltage scaling Range 1	Single ended	Fast channel (max speed)	-	-69	-67	dB
				Slow channel (max speed)	-	-71	-67	
			Differential	Fast channel (max speed)	-	-72	-71	
				Slow channel (max speed)	-	-72	-71	

1. Guaranteed by design.

2. ADC DC accuracy values are measured after internal calibration.

3. ADC accuracy vs. negative Injection Current: Injecting negative current on any analog input pins should be avoided as this significantly reduces the accuracy of the conversion being performed on another analog input. It is recommended to add a Schottky diode (pin to ground) to analog pins which may potentially inject negative current.

4. The I/O analog switch voltage booster is enable when V_{DDA} < 2.4 V (BOOSTEN = 1 in the SYSCFG_CFGR1 when V_{DDA} < 2.4 V). It is disable when V_{DDA} ≥ 2.4 V. No oversampling.

Table 71. VREFBUF characteristics[1] (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DDA}(VREFBUF)	VREFBUF consumption from V_{DDA}	I_{load} = 0 µA	-	16	25	µA
		I_{load} = 500 µA	-	18	30	
		I_{load} = 4 mA	-	35	50	

1. Guaranteed by design, unless otherwise specified.

2. In degraded mode, the voltage reference buffer can not maintain accurately the output voltage which will follow (V_{DDA} - drop voltage).

3. Guaranteed by test in production.

4. The capacitive load must include a 100 nF capacitor in order to cut-off the high frequency noise.

5. To correctly control the VREFBUF inrush current during start-up phase and scaling change, the V_{DDA} voltage should be in the range [2.4 V to 3.6 V] and [2.8 V to 3.6 V] respectively for V_{RS} = 0 and V_{RS} = 1.

6.3.20 Comparator characteristics

Table 72. COMP characteristics[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-		1.62	-	3.6	V
V_{IN}	Comparator input voltage range			0	-	V_{DDA}	
V_{BG}[2]	Scaler input voltage	-			V_{REFINT}		
V_{SC}	Scaler offset voltage	-		-	±5	±10	mV
I_{DDA}(SCALER)	Scaler static consumption from V_{DDA}	BRG_EN=0 (bridge disable)		-	200	300	nA
		BRG_EN=1 (bridge enable)		-	0.8	1	µA
t_{START_SCALER}	Scaler startup time	-		-	100	200	µs
t_{START}	Comparator startup time to reach propagation delay specification	High-speed mode	$V_{DDA} \geq 2.7$ V	-	-	5	µs
			$V_{DDA} < 2.7$ V	-	-	7	
		Medium mode	$V_{DDA} \geq 2.7$ V	-	-	15	
			$V_{DDA} < 2.7$ V	-	-	25	
		Ultra-low-power mode		-	-	40	
t_D[3]	Propagation delay with 100 mV overdrive	High-speed mode	$V_{DDA} \geq 2.7$ V	-	55	80	ns
			$V_{DDA} < 2.7$ V	-	65	100	
		Medium mode		-	0.55	0.9	µs
		Ultra-low-power mode		-	4	7	
V_{offset}	Comparator offset error	Full common mode range	-	-	±5	±20	mV
V_{hys}	Comparator hysteresis	No hysteresis		-	0	-	mV
		Low hysteresis		-	8	-	
		Medium hysteresis		-	15	-	
		High hysteresis		-	27	-	
I_{DDA}(COMP)	Comparator consumption from V_{DDA}	Ultra-low-power mode	Static	-	400	600	nA
			With 50 kHz ±100 mV overdrive square signal	-	1200	-	
		Medium mode	Static	-	5	7	µA
			With 50 kHz ±100 mV overdrive square signal	-	6	-	
		High-speed mode	Static	-	70	100	µA
			With 50 kHz ±100 mV overdrive square signal	-	75	-	

1. Guaranteed by design, unless otherwise specified.

6.3.22 Temperature sensor characteristics

Table 74. TS characteristics

Symbol	Parameter	Min	Typ	Max	Unit
T_L[1]	V_{TS} linearity with temperature	-	±1	±2	°C
Avg_Slope[2]	Average slope	2.3	2.5	2.7	mV/°C
V_{30}	Voltage at 30°C (±5 °C)[3]	0.742	0.76	0.785	V
t_{START} (TS_BUF)[1]	Sensor Buffer Start-up time in continuous mode[4]	-	8	15	µs
t_{START}[1]	Start-up time when entering in continuous mode[4]	-	70	120	µs
t_{S_temp}[1]	ADC sampling time when reading the temperature	5	-	-	µs
$I_{DD}(TS)$[1]	Temperature sensor consumption from V_{DD}, when selected by ADC	-	4.7	7	µA

1. Guaranteed by design.

2. Guaranteed by characterization results.

3. Measured at V_{DDA} = 3.0 V ±10 mV. The V_{30} ADC conversion result is stored in the TS_CAL1 byte. Refer to *Table 6: Temperature sensor calibration values*.

4. Continuous mode means Run/Sleep modes, or temperature sensor enable in Low-power run/Low-power sleep modes.

6.3.23 V_{BAT} monitoring characteristics

Table 75. V_{BAT} monitoring characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R	Resistor bridge for V_{BAT}	-	39	-	kΩ
Q	Ratio on V_{BAT} measurement	-	3	-	-
Er[1]	Error on Q	-10	-	10	%
t_{S_vbat}[1]	ADC sampling time when reading the VBAT	12	-	-	µs

1. Guaranteed by design.

Table 76. V_{BAT} charging characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{BC}	Battery charging resistor	VBRS = 0	-	5	-	kΩ
		VBRS = 1	-	1.5	-	

SPI characteristics

Unless otherwise specified, the parameters given in *Table 82* for SPI are derived from tests performed under the ambient temperature, f_{PCLKx} frequency and supply voltage conditions summarized in *Table 20: General operating conditions*.

- Output speed is set to OSPEEDRy[1:0] = 11
- Capacitive load C = 30 pF
- Measurement points are done at CMOS levels: $0.5 \times V_{DD}$

Refer to *Section 6.3.14: I/O port characteristics* for more details on the input/output alternate function characteristics (NSS, SCK, MOSI, MISO for SPI).

Table 82. SPI characteristics[1]

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{SCK} $1/t_{c(SCK)}$	SPI clock frequency	Master mode receiver/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1	-	-	40	MHz
		Master mode receiver/full duplex $1.71 < V_{DD} < 3.6$ V Voltage Range 1			16	
		Master mode transmitter $1.71 < V_{DD} < 3.6$ V Voltage Range 1			40	
		Slave mode receiver $1.71 < V_{DD} < 3.6$ V Voltage Range 1			40	
		Slave mode transmitter/full duplex $2.7 < V_{DD} < 3.6$ V Voltage Range 1			37[2]	
		Slave mode transmitter/full duplex $1.71 < V_{DD} < 3.6$ V Voltage Range 1			20[2]	
		Voltage Range 2			13	
$t_{su(NSS)}$	NSS setup time	Slave mode, SPI prescaler = 2	$4_x T_{PCLK}$	-	-	ns
$t_{h(NSS)}$	NSS hold time	Slave mode, SPI prescaler = 2	$2_x T_{PCLK}$	-	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode	T_{PCLK}-2	T_{PCLK}	T_{PCLK}+2	ns
$t_{su(MI)}$	Data input setup time	Master mode	4	-	-	ns
$t_{su(SI)}$		Slave mode	1.5	-	-	
$t_{h(MI)}$	Data input hold time	Master mode	6.5	-	-	ns
$t_{h(SI)}$		Slave mode	1.5	-	-	
$t_{a(SO)}$	Data output access time	Slave mode	9	-	36	ns
$t_{dis(SO)}$	Data output disable time	Slave mode	9	-	16	ns

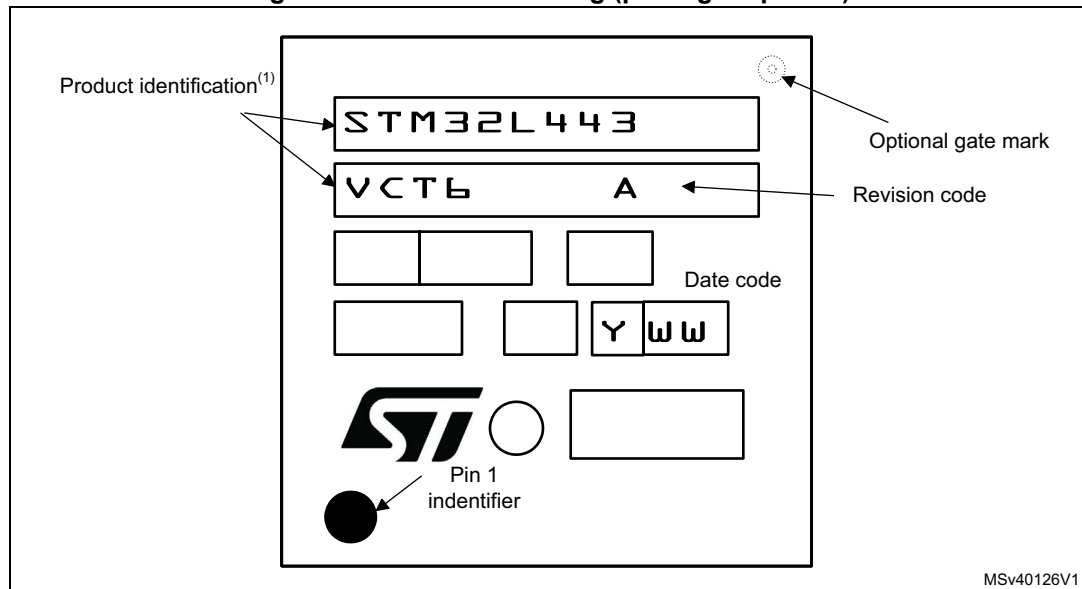**Figure 42. LQFP100 - 100-pin, 14 x 14 mm low-profile quad flat recommended footprint**
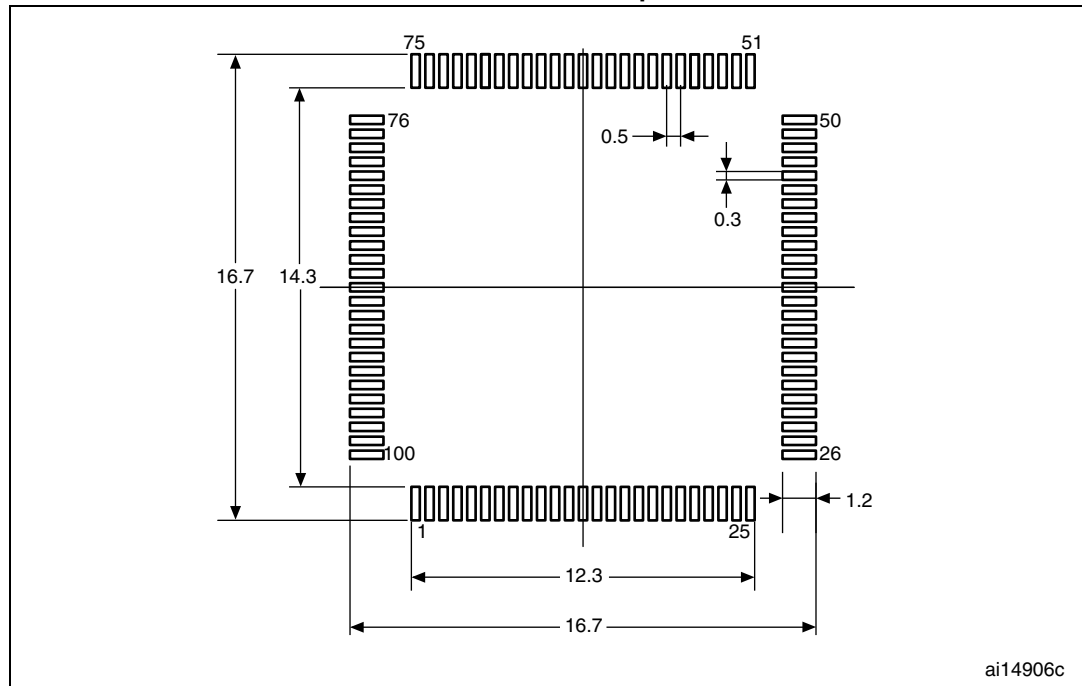
1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Figure 43. LQFP100 marking (package top view)

1. Parts marked as "ES", "E" or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering

7.3   LQFP64 package information

Figure 47. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat package outline

5W_ME_V3
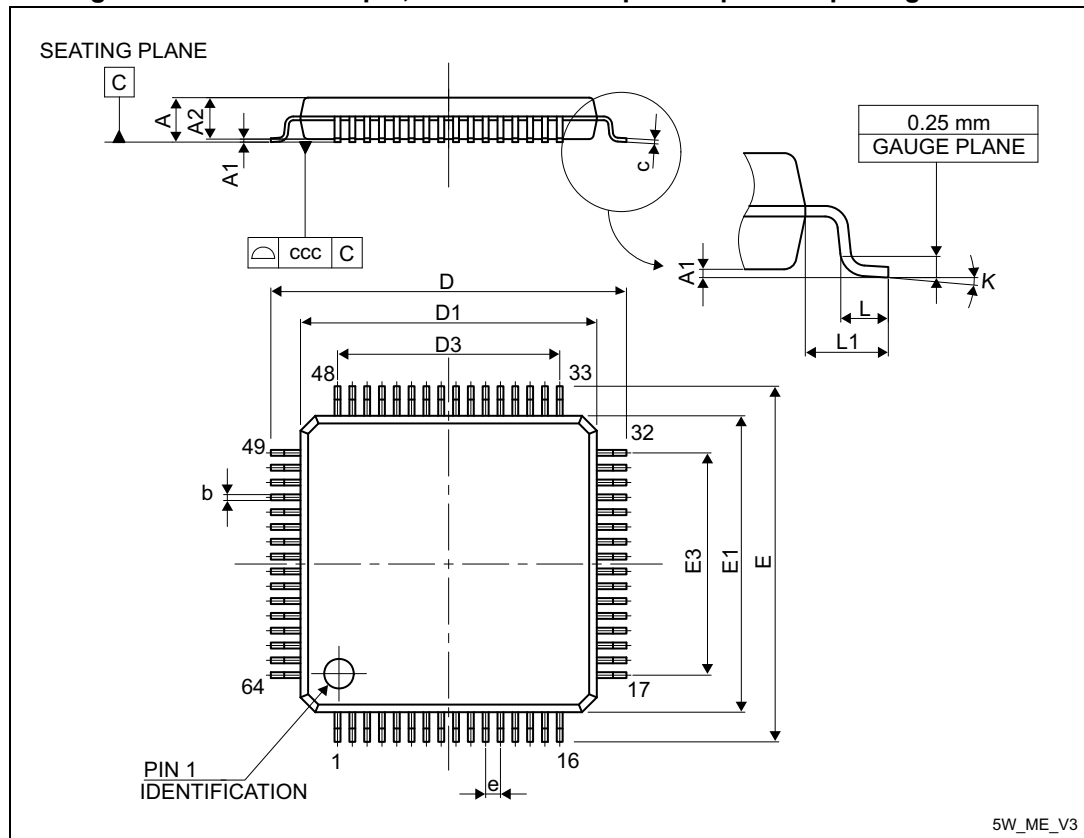
1.   Drawing is not to scale.

**Table 93. LQFP64 - 64-pin, 10 x 10 mm low-profile quad flat
package mechanical data**

| Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.600	-	-	0.0630
A1	0.050	-	0.150	0.0020	-	0.0059
A2	1.350	1.400	1.450	0.0531	0.0551	0.0571
b	0.170	0.220	0.270	0.0067	0.0087	0.0106
c	0.090	-	0.200	0.0035	-	0.0079
D	-	12.000	-	-	0.4724	-
D1	-	10.000	-	-	0.3937	-
D3	-	7.500	-	-	0.2953	-
E	-	12.000	-	-	0.4724	-
E1	-	10.000	-	-	0.3937	-

Table 96. WLCSP64 - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package mechanical data (continued)

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
b[3]	0.190	0.220	0.250	0.0075	0.0087	0.0098
D	3.106	3.141	3.176	0.1223	0.1237	0.1250
E	3.092	3.127	3.162	0.1217	0.1231	0.1245
e	-	0.350	-	-	0.0138	-
e1	-	2.450	-	-	0.0965	-
e2	-	2.450	-	-	0.0965	-
F	-	0.3455	-	-	0.0136	-
G	-	0.3385	-	-	0.0133	-
aaa	-	-	0.100	-	-	0.0039
bbb	-	-	0.100	-	-	0.0039
ccc	-	-	0.100	-	-	0.0039
ddd	-	-	0.050	-	-	0.0020
eee	-	-	0.050	-	-	0.0020

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating.

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Figure 54. WLCSP64 - 64-ball, 3.141 x 3.127 mm, 0.35 mm pitch wafer level chip scale package recommended footprint

WLCSP49_A04Z_FP_V1
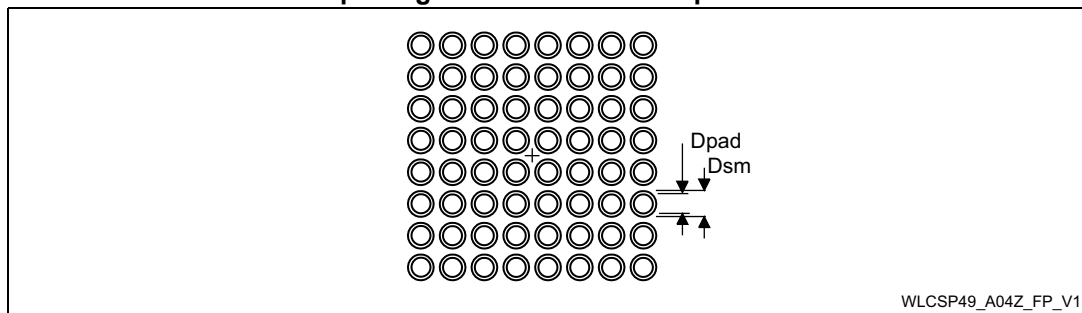
Table 97. WLCSP64 recommended PCB design rules (0.35 mm pitch)

Dimension	Recommended values
Pitch	0.35 mm
Dpad	0.210 mm
Dsm	0.275 mm typ. (depends on the soldermask registration tolerance)
Stencil opening	0.235 mm
Stencil thickness	0.100 mm