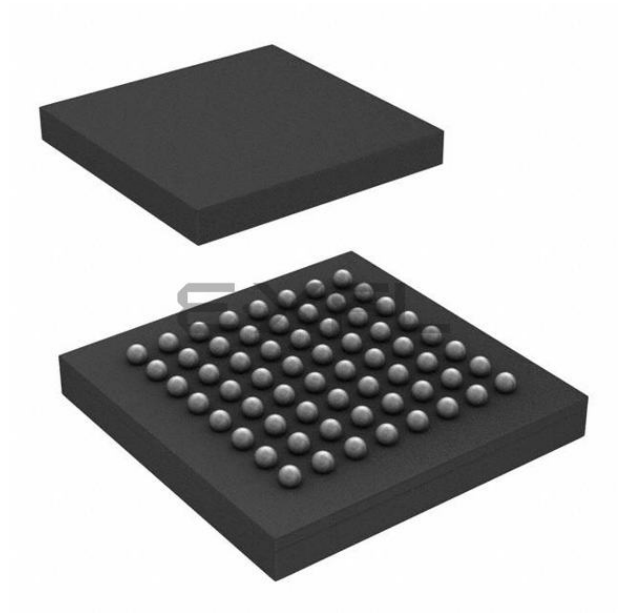

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	80MHz
Connectivity	CANbus, I²C, IrDA, LINbus, MMC/SD, QSPI, SAI, SPI, SWPMI, UART/USART, USB
Peripherals	Brown-out Detect/Reset, DMA, LCD, PWM, WDT
Number of I/O	52
Program Memory Size	256KB (256K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	64K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 16x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-UFBGA, WLCSP
Supplier Device Package	64-WLCSP (3.14x3.13)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/stm32l443rcy6tr

3.27 Universal synchronous/asynchronous receiver transmitter (USART)

The STM32L443xx devices have three embedded universal synchronous receiver transmitters (USART1, USART2 and USART3).

These interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. They provide hardware management of the CTS and RTS signals, and RS485 Driver Enable. They are able to communicate at speeds of up to 10Mbit/s.

USART1, USART2 and USART3 also provide Smart Card mode (ISO 7816 compliant) and SPI-like communication capability.

All USART have a clock domain independent from the CPU clock, allowing the USARTx (x=1,2,3) to wake up the MCU from Stop mode using baudrates up to 200 Kbaud. The wake up events from Stop mode are programmable and can be:

- Start bit detection
- Any received data frame
- A specific programmed data frame

All USART interfaces can be served by the DMA controller.

Table 10. STM32L443xx USART/LPUART features

USART modes/features(1)	USART1	USART2	USART3	LPUART1
Hardware flow control for modem	X	X	X	X
Continuous communication using DMA	X	X	X	X
Multiprocessor communication	X	X	X	X
Synchronous mode	X	X	X	-
Smartcard mode	X	X	X	-
Single-wire half-duplex communication	X	X	X	X
IrDA SIR ENDEC block	X	X	X	-
LIN mode	X	X	X	-
Dual clock domain	X	X	X	X
Wakeup from Stop 0 / Stop 1 modes	X	X	X	X
Wakeup from Stop 2 mode	-	-	-	X
Receiver timeout interrupt	X	X	X	-
Modbus communication	X	X	X	-
Auto baud rate detection	X (4 modes)			-
Driver Enable	X	X	X	X
LPUART/USART data length	7, 8 and 9 bits			

1. X = supported.

- Transmission
  - Three transmit mailboxes
  - Configurable transmit priority
- Reception
  - Two receive FIFOs with three stages
  - 14 Scalable filter banks
  - Identifier list feature
  - Configurable FIFO overrun
- Time-triggered communication option
  - Disable automatic retransmission mode
  - 16-bit free running timer
  - Time Stamp sent in last two data bytes
- Management
  - Maskable interrupts
  - Software-efficient mailbox mapping at a unique address space

3.33 Secure digital input/output and MultiMediaCards Interface (SDMMC)

The card host interface (SDMMC) provides an interface between the APB peripheral bus and MultiMediaCards (MMCs), SD memory cards and SDIO cards.

The SDMMC features include the following:

- Full compliance with MultiMediaCard System Specification Version 4.2. Card support for three different databus modes: 1-bit (default), 4-bit and 8-bit
- Full compatibility with previous versions of MultiMediaCards (forward compatibility)
- Full compliance with SD Memory Card Specifications Version 2.0
- Full compliance with SD I/O Card Specification Version 2.0: card support for two different databus modes: 1-bit (default) and 4-bit
- Data transfer up to 48 MHz for the 8 bit mode
- Data write and read with DMA capability

3.34 Universal serial bus (USB)

The STM32L443xx devices embed a full-speed USB device peripheral compliant with the USB specification version 2.0. The internal USB PHY supports USB FS signaling, embedded DP pull-up and also battery charging detection according to Battery Charging Specification Revision 1.2. The USB interface implements a full-speed (12 Mbit/s) function interface with added support for USB 2.0 Link Power Management. It has software-configurable endpoint setting with packet memory up-to 1 KB and suspend/resume support. It requires a precise 48 MHz clock which can be generated from the internal main PLL (the clock source must use a HSE crystal oscillator) or by the internal 48 MHz oscillator in automatic trimming mode. The synchronization for this oscillator can be taken from the USB data stream itself (SOF signalization) which allows crystal less operation.

Table 13. STM32L443xx pin definitions (continued)

Pin Number								Pin name (function after reset)	Pin type	I/O structure	Notes	Pin functions	
LQFP48	UFQFPN48	WLCSP49	WLCSP64	LQFP64	UFBGA64	LQFP100	UFBGA100					Alternate functions	Additional functions
-	-	-	-	-	-	58	J11	PD11	I/O	FT_l	-	USART3_CTS, TSC_G6_IO2, LCD_SEG31, LPTIM2_ETR, EVENTOUT	-
-	-	-	-	-	-	59	J10	PD12	I/O	FT_l	-	USART3_RTS_DE, TSC_G6_IO3, LCD_SEG32, LPTIM2_IN1, EVENTOUT	-
-	-	-	-	-	-	60	H12	PD13	I/O	FT_l	-	TSC_G6_IO4, LCD_SEG33, LPTIM2_OUT, EVENTOUT	-
-	-	-	-	-	-	61	H11	PD14	I/O	FT_l	-	LCD_SEG34, EVENTOUT	-
-	-	-	-	-	-	62	H10	PD15	I/O	FT_l	-	LCD_SEG35, EVENTOUT	-
-	-	-	F1	37	F6	63	E12	PC6	I/O	FT_l	-	TSC_G4_IO1, LCD_SEG24, SDMMC1_D6, EVENTOUT	-
-	-	-	E1	38	E7	64	E11	PC7	I/O	FT_l	-	TSC_G4_IO2, LCD_SEG25, SDMMC1_D7, EVENTOUT	-
-	-	-	F3	39	E8	65	E10	PC8	I/O	FT_l	-	TSC_G4_IO3, LCD_SEG26, SDMMC1_D0, EVENTOUT	-
-	-	-	E2	40	D8	66	D12	PC9	I/O	FT_l	-	TSC_G4_IO4, USB_NOE, LCD_SEG27, SDMMC1_D1, EVENTOUT	-
29	29	D1	E3	41	D7	67	D11	PA8	I/O	FT_l	-	MCO, TIM1_CH1, USART1_CK, LCD_COM0, SWPMI1_IO, SAI1_SCK_A, LPTIM2_OUT, EVENTOUT	-
30	30	D2	D1	42	C7	68	D10	PA9	I/O	FT_fl	-	TIM1_CH2, I2C1_SCL, USART1_TX, LCD_COM1, SAI1_FS_A, TIM15_BKIN, EVENTOUT	-

Table 15. Alternate function AF8 to AF15 (for AF0 to AF7 see *Table 14*) (continued)

Port		AF8	AF9	AF10	AF11	AF12	AF13	AF14	AF15
		LPUART1	CAN1/TSC	USB/QUADSPI	LCD	SDMMC1/ COMP1/ COMP2/ SWPMI1	SAI1	TIM2/TIM15/ TIM16/LPTIM2	EVENTOUT
Port H	PH0	-	-	-	-	-	-	-	EVENTOUT
	PH1	-	-	-	-	-	-	-	EVENTOUT
	PH3	-	-	-	-	-	-	-	EVENTOUT

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified, the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = $T_A$max (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean ±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = V_{DDA} = 3 V. They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean ±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in *Figure 14*.

6.1.5 Pin input voltage

The input voltage measurement on a pin of the device is described in *Figure 15*.

Figure 14. Pin loading conditions

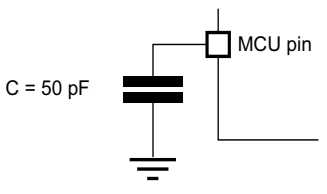
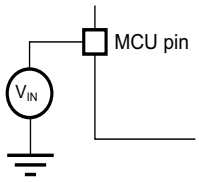


Figure 15. Pin input voltage



6.3.4 Embedded voltage reference

The parameters given in *Table 23* are derived from tests performed under the ambient temperature and supply voltage conditions summarized in *Table 20: General operating conditions*.

Table 23. Embedded internal voltage reference

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{REFINT}	Internal reference voltage	–40 °C < T_A < +130 °C	1.182	1.212	1.232	V
$t_{S\_vrefint}$ (1)	ADC sampling time when reading the internal reference voltage	-	4(2)	-	-	µs
$t_{start\_vrefint}$	Start time of reference voltage buffer when ADC is enable	-	-	8	12(2)	µs
$I_{DD}(V_{REFINTBUF})$	V_{REFINT} buffer consumption from V_{DD} when converted by ADC	-	-	12.5	20(2)	µA
ΔV_{REFINT}	Internal reference voltage spread over the temperature range	V_{DD} = 3 V	-	5	7.5(2)	mV
T_{Coeff}	Temperature coefficient	–40°C < T_A < +130°C	-	30	50(2)	ppm/°C
A_{Coeff}	Long term stability	1000 hours, T = 25°C	-	-	TBD(2)	ppm
$V_{DDCoeff}$	Voltage coefficient	3.0 V < V_{DD} < 3.6 V	-	250	1200(2)	ppm/V
V_{REFINT_DIV1}	1/4 reference voltage	-	24	25	26	% V_{REFINT}
V_{REFINT_DIV2}	1/2 reference voltage		49	50	51	
V_{REFINT_DIV3}	3/4 reference voltage		74	75	76	

1. The shortest sampling time can be determined in the application by multiple iterations.
2. Guaranteed by design.

Table 30. Current consumption in Sleep and Low-power sleep modes, Flash ON

Symbol	Parameter	Conditions			TYP					MAX(1)					Unit
		-	Voltage scaling	f_{HCLK}	25 °C	55 °C	85 °C	105 °C	125 °C	25 °C	55 °C	85 °C	105 °C	125 °C	
I_{DD}(Sleep)	Supply current in sleep mode,	$f_{HCLK} = f_{HSE}$ up to 48 MHz included, bypass mode pll ON above 48 MHz all peripherals disable	Range 2	26 MHz	0.68	0.69	0.74	0.81	0.95	0.8	0.8	0.9	1.0	1.3	mA
				16 MHz	0.46	0.48	0.52	0.59	0.73	0.5	0.6	0.6	0.8	1.1	
				8 MHz	0.29	0.30	0.34	0.41	0.55	0.3	0.4	0.4	0.6	0.9	
				4 MHz	0.20	0.21	0.25	0.32	0.46	0.2	0.3	0.3	0.5	0.8	
				2 MHz	0.16	0.17	0.21	0.28	0.42	0.2	0.2	0.3	0.4	0.7	
				1 MHz	0.13	0.15	0.19	0.26	0.40	0.1	0.2	0.3	0.4	0.7	
				100 kHz	0.11	0.13	0.17	0.24	0.38	0.1	0.2	0.2	0.4	0.7	
			Range 1	80 MHz	2.23	2.25	2.30	2.38	2.54	2.5	2.5	2.6	2.8	3.1	
				72 MHz	2.02	2.04	2.10	2.18	2.34	2.2	2.3	2.4	2.5	2.9	
				64 MHz	1.82	1.84	1.89	1.98	2.14	2.0	2.1	2.1	2.3	2.6	
				48 MHz	1.34	1.36	1.42	1.50	1.66	1.5	1.6	1.7	1.8	2.2	
				32 MHz	0.93	0.95	1.01	1.09	1.25	1.1	1.1	1.2	1.4	1.7	
				24 MHz	0.73	0.75	0.80	0.88	1.04	0.8	0.9	1.0	1.1	1.4	
				16 MHz	0.53	0.55	0.60	0.68	0.84	0.6	0.6	0.7	0.9	1.2	
I_{DD}(LPSleep)	Supply current in low-power sleep mode	$f_{HCLK} = f_{MSI}$ all peripherals disable		2 MHz	71.8	80.7	125	200	350	91.1	122.7	191.3	341.5	653.5	µA
				1 MHz	45.0	57.3	101	176	325	63.2	95.4	165.4	316.5	628.7	
				400 kHz	27.0	40.7	84.6	158	308	43.9	75.8	147.2	297.6	609.2	
				100 kHz	22.8	30.9	63.3	113.2	207.7	35.2	67.9	140.9	290.8	602.4	

1. Guaranteed by characterization results, unless otherwise specified.

1. Guaranteed by characterization results, unless otherwise specified.
2. LCD enabled with external voltage source. Consumption from VLCD excluded. Refer to LCD controller characteristics for I_{VLCD}.
3. Guaranteed by test in production.
4. Based on characterization done with a 32.768 kHz crystal (MC306-G-06Q-32.768, manufacturer JFVNY) with two 6.8 pF loading capacitors.
5. Wakeup with code execution from Flash. Average value given for a typical wakeup time as specified in *Table 39: Low-power mode wakeup timings*.

On-chip peripheral current consumption

The current consumption of the on-chip peripherals is given in *Table 38*. The MCU is placed under the following conditions:

- All I/O pins are in Analog mode
- The given value is calculated by measuring the difference of the current consumptions:
  - when the peripheral is clocked on
  - when the peripheral is clocked off
- Ambient operating temperature and supply voltage conditions summarized in *Table 17: Voltage characteristics*
- The power consumption of the digital part of the on-chip peripherals is given in *Table 38*. The power consumption of the analog part of the peripherals (where applicable) is indicated in each related section of the datasheet.

Table 38. Peripheral current consumption

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
AHB	Bus Matrix(1)	3.2	2.9	3.1	µA/MHz
	ADC independent clock domain	0.4	0.1	0.2	
	ADC clock domain	2.1	1.9	1.9	
	AES	1.7	1.5	1.6	
	CRC	0.4	0.2	0.3	
	DMA1	1.4	1.3	1.4	
	DMA2	1.5	1.3	1.4	
	FLASH	6.2	5.2	5.8	
	GPIOA(2)	1.7	1.4	1.6	
	GPIOB(2))	1.6	1.3	1.6	
	GPIOC(2)	1.7	1.5	1.6	
	GPIOD(2)	1.8	1.6	1.7	
	GPIOE(2)	1.7	1.6	1.6	
	GPIOH(2)	0.6	0.6	0.5	
	QSPI	7.0	5.8	7.3	
	RNG independent clock domain	2.2	NA	NA	
	RNG clock domain	0.5	NA	NA	
	SRAM1	0.8	0.9	0.7	
	SRAM2	1.0	0.8	0.8	
	TSC	1.6	1.3	1.3	
	All AHB Peripherals	25.2	21.7	23.6	
APB1	AHB to APB1 bridge(3)	0.9	0.7	0.9	
	CAN1	4.1	3.2	3.9	

Table 38. Peripheral current consumption (continued)

Peripheral		Range 1	Range 2	Low-power run and sleep	Unit
APB1	USART3 independent clock domain	4.3	3.5	4.2	µA/MHz
	USART3 clock domain	1.5	1.1	1.3	
	WWDG	0.5	0.5	0.5	
	All APB1 on	51.5	35.5	48.6	
APB2	AHB to APB2(4)	1.0	0.9	0.9	
	FW	0.2	0.2	0.2	
	SAI1 independent clock domain	2.3	1.8	1.9	
	SAI1 clock domain	2.1	1.8	2.0	
	SDMMC1 independent clock domain	4.7	3.9	3.9	
	SDMMC1 clock domain	2.5	1.9	1.9	
	SPI1	1.8	1.6	1.7	
	SYSCFG/VREFBUF/COMP	0.6	0.5	0.6	
	TIM1	8.1	6.5	7.6	
	TIM15	3.7	3.0	3.4	
	TIM16	2.7	2.1	2.6	
	USART1 independent clock domain	4.8	4.2	4.6	
	USART1 clock domain	1.5	1.3	1.7	
	All APB2 on	24.2	19.9	22.6	
ALL		100.9	77.1	94.8	

1. The BusMatrix is automatically active when at least one master is ON (CPU, DMA).
2. The GPIOx (x= A…H) dynamic current consumption is approximately divided by a factor two versus this table values when the GPIO port is locked thanks to LCKK and LCKy bits in the GPIOx_LCKR register. In order to save the full GPIOx current consumption, the GPIOx clock should be disabled in the RCC when all port I/Os are used in alternate function or analog mode (clock is only required to read or write into GPIO registers, and is not used in AF or analog modes).
3. The AHB to APB1 Bridge is automatically active when at least one peripheral is ON on the APB1.
4. The AHB to APB2 Bridge is automatically active when at least one peripheral is ON on the APB2.

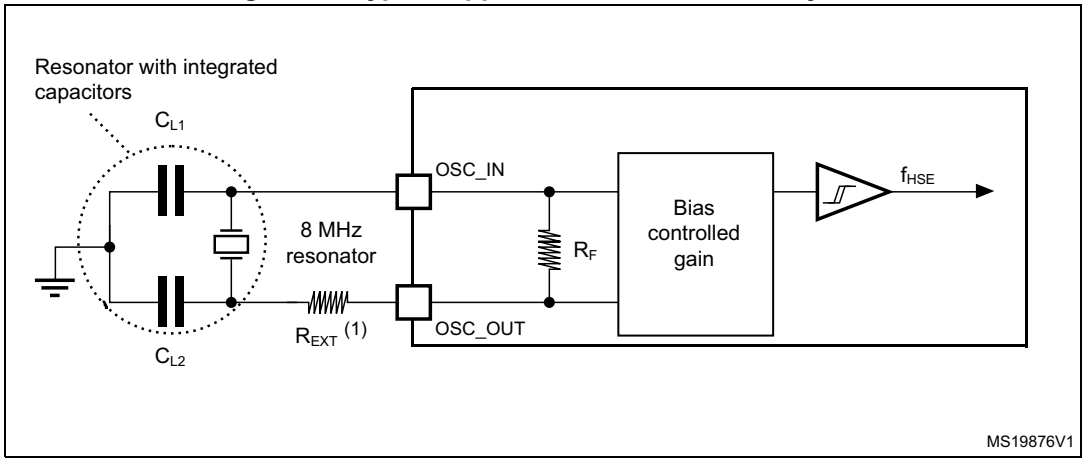
6.3.6 Wakeup time from low-power modes and voltage scaling transition times

The wakeup times given in *Table 39* are the latency between the event and the execution of the first user instruction.

The device goes in low-power mode after the WFE (Wait For Event) instruction.

Note: For information on selecting the crystal, refer to the application note AN2867 "Oscillator design guide for ST microcontrollers" available from the ST website www.st.com.

Figure 21. Typical application with an 8 MHz crystal



1. R_{EXT} value depends on the crystal characteristics.

Low-speed external clock generated from a crystal resonator

The low-speed external (LSE) clock can be supplied with a 32.768 kHz crystal resonator oscillator. All the information given in this paragraph are based on design simulation results obtained with typical external components specified in *Table 45*. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 45. LSE oscillator characteristics (f_{LSE} = 32.768 kHz)(1)

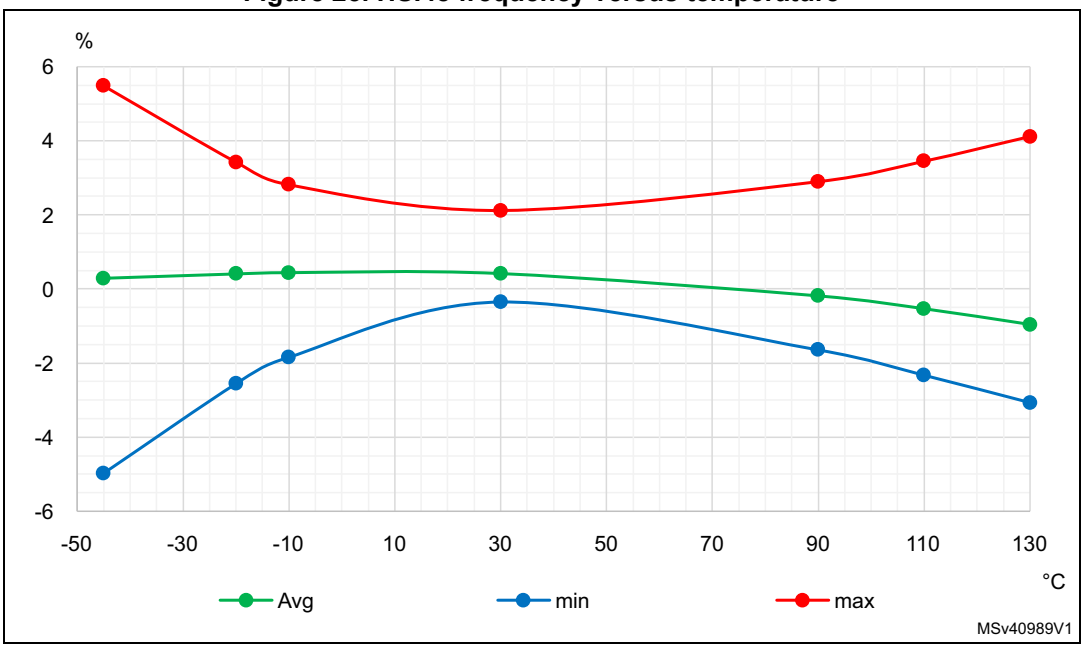
Symbol	Parameter	Conditions(2)	Min	Typ	Max	Unit
$I_{DD(LSE)}$	LSE current consumption	LSEDRV[1:0] = 00 Low drive capability	-	250	-	nA
		LSEDRV[1:0] = 01 Medium low drive capability	-	315	-	
		LSEDRV[1:0] = 10 Medium high drive capability	-	500	-	
		LSEDRV[1:0] = 11 High drive capability	-	630	-	
$Gm_{critmax}$	Maximum critical crystal gm	LSEDRV[1:0] = 00 Low drive capability	-	-	0.5	µA/V
		LSEDRV[1:0] = 01 Medium low drive capability	-	-	0.75	
		LSEDRV[1:0] = 10 Medium high drive capability	-	-	1.7	
		LSEDRV[1:0] = 11 High drive capability	-	-	2.7	
$t_{SU(LSE)}$(3)	Startup time	V_{DD} is stabilized	-	2	-	s

Table 48. HSI48 oscillator characteristics(1) (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
N_T jitter	Next transition jitter Accumulated jitter on 28 cycles(4)	-	-	+/-0.15(2)	-	ns
P_T jitter	Paired transition jitter Accumulated jitter on 56 cycles(4)	-	-	+/-0.25(2)	-	ns

1. V_{DD} = 3 V, T_A = –40 to 125°C unless otherwise specified.
2. Guaranteed by design.
3. Guaranteed by characterization results.
4. Jitter measurement are performed without clock source activated in parallel.

Figure 25. HSI48 frequency versus temperature



Low-speed internal (LSI) RC oscillator

Table 49. LSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LSI}	LSI Frequency	V_{DD} = 3.0 V, T_A = 30 °C	31.04	-	32.96	kHz
		V_{DD} = 1.62 to 3.6 V, TA = -40 to 125 °C	29.5	-	34	
$t_{SU}(LSI)$(2)	LSI oscillator start-up time	-	-	80	130	µs
$t_{STAB}(LSI)$(2)	LSI oscillator stabilization time	5% of final frequency	-	125	180	µs
$I_{DD}(LSI)$(2)	LSI oscillator power consumption	-	-	110	180	nA

1. Guaranteed by characterization results.
2. Guaranteed by design.

Table 60. I/O AC characteristics(1)(2) (continued)

Speed	Symbol	Parameter	Conditions	Min	Max	Unit
10	Fmax	Maximum frequency	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	50	MHz
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	25	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	100(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	37.5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	5	
	Tr/Tf	Output rise and fall time	C=50 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	5.8	ns
			C=50 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	11	
			C=50 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	28	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	2.5	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	5	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	12	
11	Fmax	Maximum frequency	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	120(3)	MHz
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	50	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
			C=10 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	180(3)	
			C=10 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	75	
			C=10 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	10	
	Tr/Tf	Output rise and fall time	C=30 pF, 2.7 V≤V_{DDIOx}≤3.6 V	-	3.3	ns
			C=30 pF, 1.62 V≤V_{DDIOx}≤2.7 V	-	6	
			C=30 pF, 1.08 V≤V_{DDIOx}≤1.62 V	-	16	
Fm+	Fmax	Maximum frequency	C=50 pF, 1.6 V≤V_{DDIOx}≤3.6 V	-	1	MHz
	Tf	Output fall time(4)		-	5	ns

1. The I/O speed is configured using the OSPEEDRy[1:0] bits. The Fm+ mode is configured in the SYSCFG_CFGR1 register. Refer to the RM0394 reference manual for a description of GPIO Port configuration register.
2. Guaranteed by design.
3. This value represents the I/O capability but the maximum system frequency is limited to 80 MHz.
4. The fall time is defined between 70% and 30% of the output waveform accordingly to I^2C specification.

6.3.18 Digital-to-Analog converter characteristics

Table 69. DAC characteristics(1)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage for DAC ON	-		1.8	-	3.6	V
V_{REF+}	Positive reference voltage	-		1.8	-	V_{DDA}	
V_{REF-}	Negative reference voltage	-		V_{SSA}			
R_L	Resistive load	DAC output buffer ON	connected to V_{SSA}	5	-	-	kΩ
			connected to V_{DDA}	25	-	-	
R_O	Output Impedance	DAC output buffer OFF		9.6	11.7	13.8	kΩ
R_{BON}	Output impedance sample and hold mode, output buffer ON	V_{DD} = 2.7 V		-	-	2	kΩ
		V_{DD} = 2.0 V		-	-	3.5	
R_{BOFF}	Output impedance sample and hold mode, output buffer OFF	V_{DD} = 2.7 V		-	-	16.5	kΩ
		V_{DD} = 2.0 V		-	-	18.0	
C_L	Capacitive load	DAC output buffer ON		-	-	50	pF
C_{SH}		Sample and hold mode		-	0.1	1	µF
V_{DAC_OUT}	Voltage on DAC_OUT output	DAC output buffer ON		0.2	-	V_{REF+} – 0.2	V
		DAC output buffer OFF		0	-	V_{REF+}	
$t_{SETTLING}$	Settling time (full scale: for a 12-bit code transition between the lowest and the highest input codes when DAC_OUT reaches final value ±0.5LSB, ±1 LSB, ±2 LSB, ±4 LSB, ±8 LSB)	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ	±0.5 LSB	-	1.7	3	µs
			±1 LSB	-	1.6	2.9	
			±2 LSB	-	1.55	2.85	
			±4 LSB	-	1.48	2.8	
			±8 LSB	-	1.4	2.75	
		Normal mode DAC output buffer OFF, ±1LSB, CL = 10 pF		-	2	2.5	
t_{WAKEUP}(2)	Wakeup time from off state (setting the ENx bit in the DAC Control register) until final value ±1 LSB	Normal mode DAC output buffer ON CL ≤ 50 pF, RL ≥ 5 kΩ		-	4.2	7.5	µs
		Normal mode DAC output buffer OFF, CL ≤ 10 pF		-	2	5	
PSRR	V_{DDA} supply rejection ratio	Normal mode DAC output buffer ON CL ≤ 50 pF, RL = 5 kΩ, DC		-	-80	-28	dB

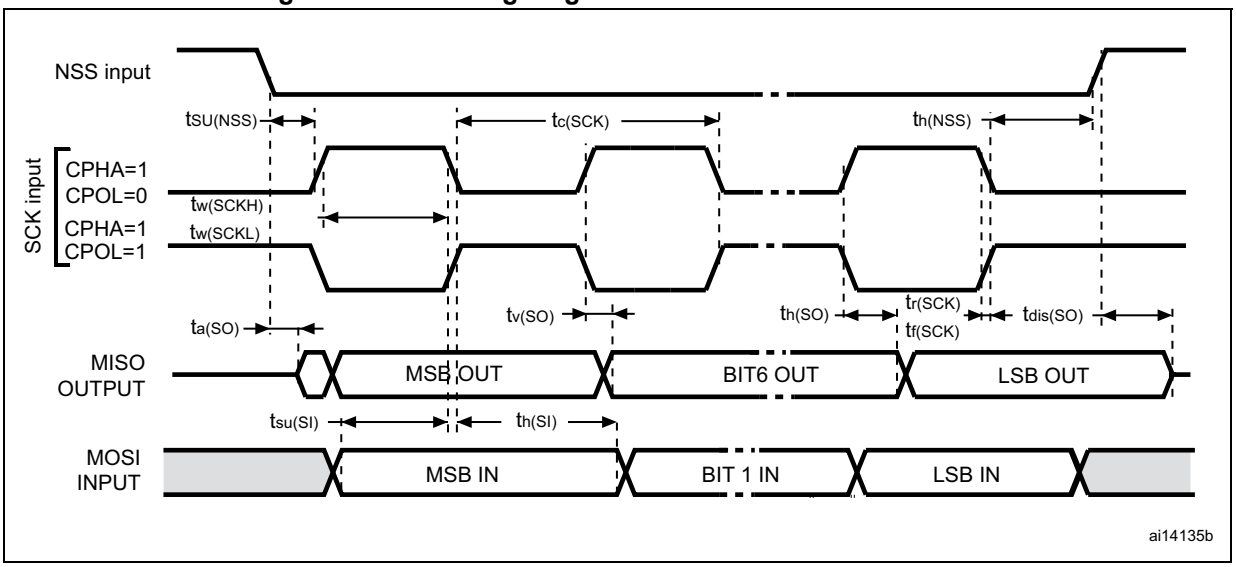
6.3.24 LCD controller characteristics

The devices embed a built-in step-up converter to provide a constant LCD reference voltage independently from the V_{DD} voltage. An external capacitor C_{ext} must be connected to the VLCD pin to decouple this converter.

Table 77. LCD controller characteristics(1)

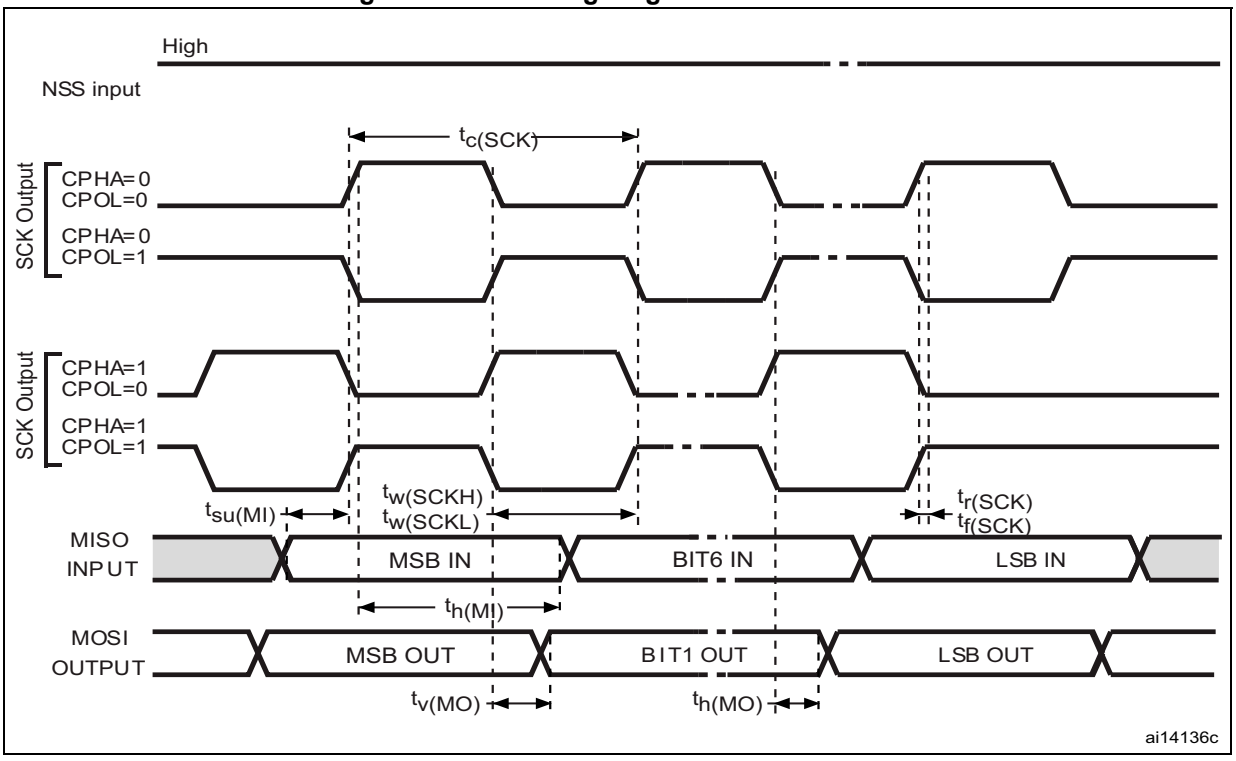
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{LCD}	LCD external voltage		-	-	3.6	V
V_{LCD0}	LCD internal reference voltage 0		-	2.62	-	
V_{LCD1}	LCD internal reference voltage 1		-	2.76	-	
V_{LCD2}	LCD internal reference voltage 2		-	2.89	-	
V_{LCD3}	LCD internal reference voltage 3		-	3.04	-	
V_{LCD4}	LCD internal reference voltage 4		-	3.19	-	
V_{LCD5}	LCD internal reference voltage 5		-	3.32	-	
V_{LCD6}	LCD internal reference voltage 6		-	3.46	-	
V_{LCD7}	LCD internal reference voltage 7		-	3.62	-	
C_{ext}	V_{LCD} external capacitance	Buffer OFF (BUFEN=0 is LCD_CR register)	0.2	-	2	µF
		Buffer ON (BUFEN=1 is LCD_CR register)	1	-	2	
I_{LCD}(2)	Supply current from V_{DD} at V_{DD} = 2.2 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	3	-	µA
	Supply current from V_{DD} at V_{DD} = 3.0 V	Buffer OFF (BUFEN=0 is LCD_CR register)	-	1.5	-	
I_{VLCD}	Supply current from V_{LCD} (V_{LCD} = 3 V)	Buffer OFF (BUFFEN = 0, PON = 0)	-	0.5	-	µA
		Buffer ON (BUFFEN = 1, 1/2 Bias)	-	0.6	-	
		Buffer ON (BUFFEN = 1, 1/3 Bias)	-	0.8	-	
		Buffer ON (BUFFEN = 1, 1/4 Bias)	-	1	-	
R_{HN}	Total High Resistor value for Low drive resistive network		-	5.5	-	MΩ
R_{LN}	Total Low Resistor value for High drive resistive network		-	240	-	kΩ
V_{44}	Segment/Common highest level voltage		-	V_{LCD}	-	V
V_{34}	Segment/Common 3/4 level voltage		-	3/4 V_{LCD}	-	
V_{23}	Segment/Common 2/3 level voltage		-	2/3 V_{LCD}	-	
V_{12}	Segment/Common 1/2 level voltage		-	1/2 V_{LCD}	-	
V_{13}	Segment/Common 1/3 level voltage		-	1/3 V_{LCD}	-	
V_{14}	Segment/Common 1/4 level voltage		-	1/4 V_{LCD}	-	
V_0	Segment/Common lowest level voltage		-	0	-	

Figure 33. SPI timing diagram - slave mode and CPHA = 1



1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Figure 34. SPI timing diagram - master mode

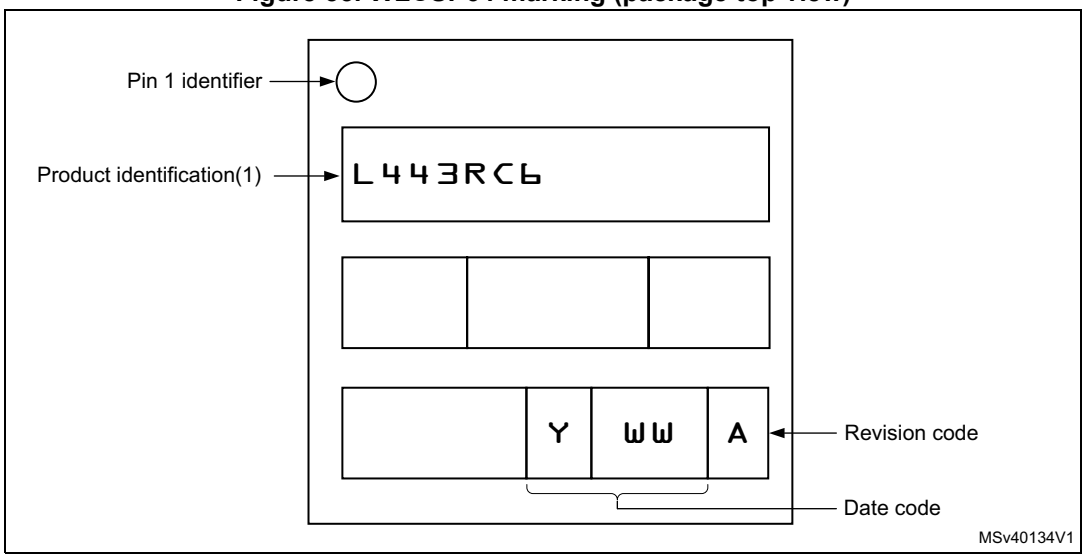


1. Measurement points are done at CMOS levels: 0.3 V_{DD} and 0.7 V_{DD}.

Device marking

The following figure gives an example of topside marking orientation versus ball A1 identifier location.

Figure 55. WLCSP64 marking (package top view)



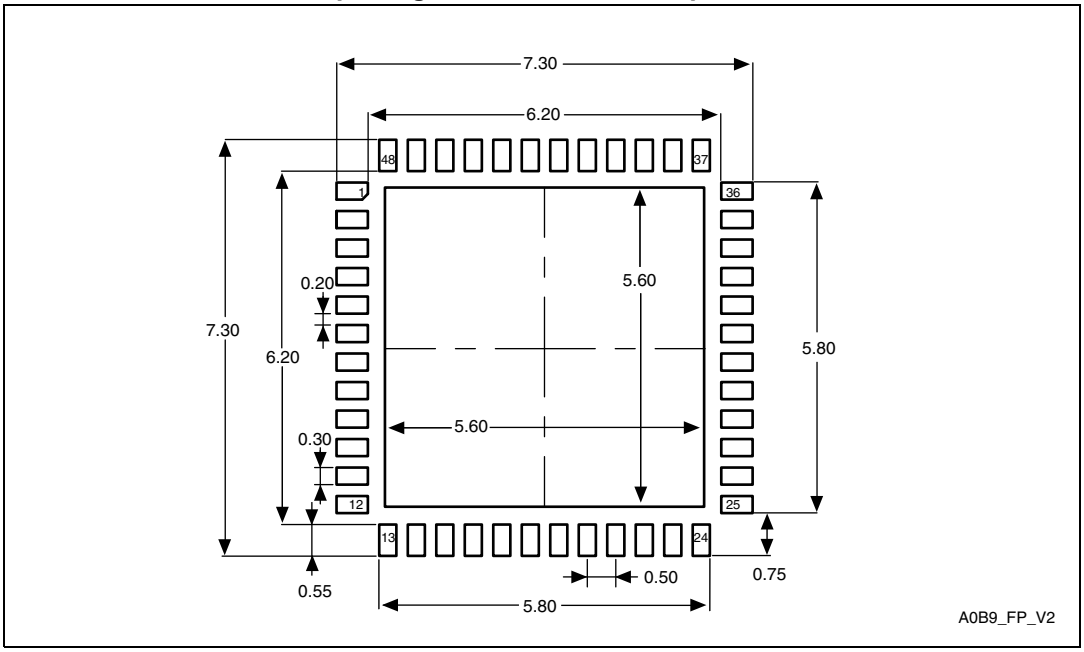
1. Parts marked as “ES”, “E” or accompanied by an Engineering Sample notification letter, are not yet qualified and therefore not yet ready to be used in production and any consequences deriving from such usage will not be at ST charge. In no event, ST will be liable for any customer usage of these engineering samples in production. ST Quality has to be contacted prior to any decision to use these Engineering samples to run qualification activity.

Table 101. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
D2	5.500	5.600	5.700	0.2165	0.2205	0.2244
E2	5.500	5.600	5.700	0.2165	0.2205	0.2244
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T	-	0.152	-	-	0.0060	-
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e	-	0.500	-	-	0.0197	-
ddd	-	-	0.080	-	-	0.0031

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 63. UFQFPN48 - 48-lead, 7x7 mm, 0.5 mm pitch, ultra thin fine pitch quad flat package recommended footprint



1. Dimensions are expressed in millimeters.

Device marking

The following figure gives an example of topside marking orientation versus pin 1 identifier location.

Assuming the following application conditions:

Maximum ambient temperature T_{Amax} = 100 °C (measured according to JESD51-2), I_{DDmax} = 20 mA, V_{DD} = 3.5 V, maximum 20 I/Os used at the same time in output at low level with I_{OL} = 8 mA, V_{OL}= 0.4 V

P_{INTmax} = 20 mA × 3.5 V= 70 mW

P_{IOmax} = 20 × 8 mA × 0.4 V = 64 mW

This gives: P_{INTmax} = 70 mW and P_{IOmax} = 64 mW:

P_{Dmax} = 70 + 64 = 134 mW

Thus: P_{Dmax} = 134 mW

Using the values obtained in *Table 102* T_{Jmax} is calculated as follows:

– For LQFP64, 46 °C/W

T_{Jmax} = 100 °C + (46 °C/W × 134 mW) = 100 °C + 6.164 °C = 106.164 °C

This is above the range of the suffix 6 version parts (–40 < T_J < 105 °C).

In this case, parts must be ordered at least with the temperature range suffix 7 (see *Section 8: Part numbering*) unless we reduce the power dissipation in order to be able to use suffix 6 parts.

Refer to *Figure 65* to select the required temperature range (suffix 6 or 7) according to your ambient temperature or power requirements.

Figure 65. LQFP64 P_D max vs. T_A