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Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I ² C), SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	40
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f501-imr

C8051F50x/F51x

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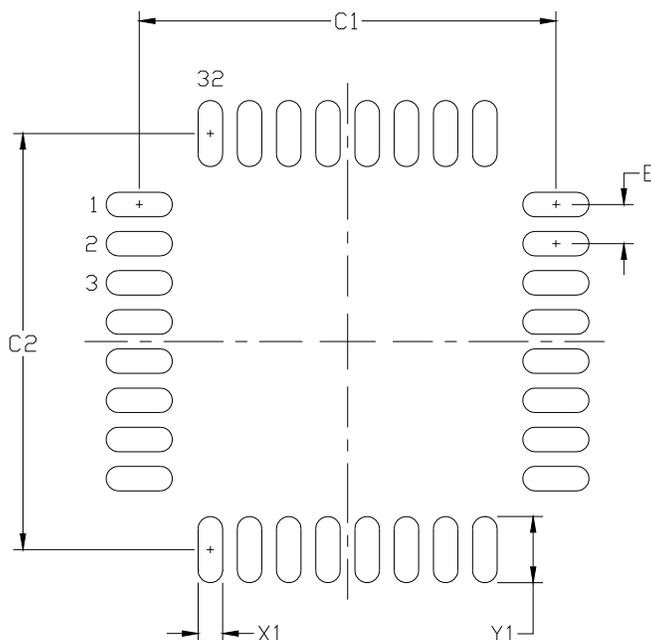


Figure 4.8. QFP-32 Package Drawing

Table 4.8. QFP-32 Landing Diagram Dimensions

Dimension	Min	Max	Dimension	Min	Max
C1	8.40	8.50	X1	0.40	0.50
C2	8.40	8.50	Y1	1.25	1.35
E	0.80 BSC				

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125 mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

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5.2. Electrical Characteristics

Table 5.2. Global Electrical Characteristics

–40 to +125 °C, 24 MHz system clock unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
Supply Input Voltage (V_{REGIN})		1.8	—	5.25	V
Digital Supply Voltage (V_{DD})	System Clock \leq 25 MHz	V_{RST}^1	—	2.75	V
	System Clock $>$ 25 MHz	2		2.75	
Analog Supply Voltage (V_{DDA}) (Must be connected to V_{DD})	System Clock \leq 25 MHz	V_{RST}^1	—	2.75	V
	System Clock $>$ 25 MHz	2		2.75	
Digital Supply RAM Data Retention Voltage			1.5		
Port I/O Supply Voltage (V_{IO})	Normal Operation	1.8 ²	—	5.25	V
SYSClk (System Clock) ³		0	—	50	MHz
T_{SYSH} (SYSClk High Time)		9	—	—	ns
T_{SYSL} (SYSClk Low Time)		9	—	—	ns
Specified Operating Temperature Range		–40	—	+125	°C
Digital Supply Current—CPU Active (Normal Mode, fetching instructions from Flash)					
I_{DD}^4	$V_{DD} = 2.1$ V, $F = 200$ kHz	—	95	—	μ A
	$V_{DD} = 2.1$ V, $F = 1.5$ MHz	—	700	—	μ A
	$V_{DD} = 2.1$ V, $F = 25$ MHz	—	10	11	mA
	$V_{DD} = 2.1$ V, $F = 50$ MHz	—	19	21	mA
Notes:					
<ol style="list-style-type: none"> Given in Table 5.4 on page 46. V_{IO} should not be lower than the V_{DD} voltage. SYSClk must be at least 32 kHz to enable debugging. Based on device characterization data; Not production tested. Does not include oscillator supply current. I_{DD} can be estimated for frequencies \leq 12.5 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate I_{DD} for $>$12.5 MHz, the estimate should be the current at 50 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD} = 2.6$ V; $F = 20$ MHz, $I_{DD} = 26$ mA - (50 MHz - 20 MHz) * 0.48 mA/MHz = 11.6 mA. Idle I_{DD} can be estimated for frequencies \leq 1 MHz by simply multiplying the frequency of interest by the frequency sensitivity number for that range. When using these numbers to estimate Idle I_{DD} for $>$1 MHz, the estimate should be the current at 50 MHz minus the difference in current indicated by the frequency sensitivity number. For example: $V_{DD} = 2.6$ V; $F = 5$ MHz, Idle $I_{DD} = 21$ mA - (50 MHz - 5 MHz) x 0.41 mA/MHz = 2.6 mA. 					

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Table 5.9. ADC0 Electrical Characteristics

VDDA = 1.8 to 2.75 V, -40 to +125 °C, VREF = 1.5 V (REFSL=0) unless otherwise specified.

Parameter	Conditions	Min	Typ	Max	Units
DC Accuracy					
Resolution			12		bits
Integral Nonlinearity		—	±0.5	±3	LSB
Differential Nonlinearity	Guaranteed Monotonic	—	±0.5	±1	LSB
Offset Error ¹		-10	-1.8	10	LSB
Full Scale Error		-20	1.7	20	LSB
Offset Temperature Coefficient		—	-2	—	ppm/°C
Dynamic performance (10 kHz sine-wave single-ended input, 1 dB below Full Scale, 200 ksps)					
Signal-to-Noise Plus Distortion		63	66	—	dB
Total Harmonic Distortion	Up to the 5th harmonic	—	82	—	dB
Spurious-Free Dynamic Range		—	-84	—	dB
Conversion Rate					
SAR Conversion Clock		—	—	3.6	MHz
Conversion Time in SAR Clocks ²		13	—	—	clocks
Track/Hold Acquisition Time ³	VDDA ≥ 2.0 V VDDA < 2.0 V	1.5 3.5	—	—	µs
Throughput Rate ⁴	VDDA ≥ 2.0 V	—	—	200	ksps
Analog Inputs					
ADC Input Voltage Range ⁵	gain = 1.0 (default) gain = n	0 0	—	VREF VREF/n	V
Absolute Pin Voltage with Respect to GND		0	—	V _{IO}	V
Sampling Capacitance		—	32	—	pF
Input Multiplexer Impedance		—	3	—	kΩ
Power Specifications					
Power Supply Current (VDDA supplied to ADC0)	Operating Mode, 200 ksps	—	1100	1500	µA
Burst Mode (Idle)		—	1100	1500	µA
Power-On Time		5	—	—	µs
Power Supply Rejection Ratio		—	-60	—	dB
Notes:					
<ol style="list-style-type: none"> 1. Represents one standard deviation from the mean. Offset and full-scale error can be removed through calibration. 2. An additional 2 FCLK cycles are required to start and complete a conversion 3. Additional tracking time may be required depending on the output impedance connected to the ADC input. See Section “6.2.1. Settling Time Requirements” on page 57. 4. An increase in tracking time will decrease the ADC throughput. 5. See Section “6.3. Selectable Gain” on page 58 for more information about the setting the gain. 					

Note that false rising edges and falling edges can be detected when the comparator is first powered on or if changes are made to the hysteresis or response time control bits. Therefore, it is recommended that the rising-edge and falling-edge flags be explicitly cleared to logic 0 a short time after the comparator is enabled or its mode bits have been changed.

SFR Definition 9.1. CPT0CN: Comparator0 Control

Bit	7	6	5	4	3	2	1	0
Name	CP0EN	CP0OUT	CP0RIF	CP0FIF	CP0HYP[1:0]		CP0HYN[1:0]	
Type	R/W	R	R/W	R/W	R/W		R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x9A; SFR Page = 0x00

Bit	Name	Function
7	CP0EN	Comparator0 Enable Bit. 0: Comparator0 Disabled. 1: Comparator0 Enabled.
6	CP0OUT	Comparator0 Output State Flag. 0: Voltage on CP0+ < CP0-. 1: Voltage on CP0+ > CP0-.
5	CP0RIF	Comparator0 Rising-Edge Flag. Must be cleared by software. 0: No Comparator0 Rising Edge has occurred since this flag was last cleared. 1: Comparator0 Rising Edge has occurred.
4	CP0FIF	Comparator0 Falling-Edge Flag. Must be cleared by software. 0: No Comparator0 Falling-Edge has occurred since this flag was last cleared. 1: Comparator0 Falling-Edge has occurred.
3:2	CP0HYP[1:0]	Comparator0 Positive Hysteresis Control Bits. 00: Positive Hysteresis Disabled. 01: Positive Hysteresis = 5 mV. 10: Positive Hysteresis = 10 mV. 11: Positive Hysteresis = 20 mV.
1:0	CP0HYN[1:0]	Comparator0 Negative Hysteresis Control Bits. 00: Negative Hysteresis Disabled. 01: Negative Hysteresis = 5 mV. 10: Negative Hysteresis = 10 mV. 11: Negative Hysteresis = 20 mV.

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SFR Definition 9.2. CPT0MD: Comparator0 Mode Selection

Bit	7	6	5	4	3	2	1	0
Name			CP0RIE	CP0FIE			CP0MD[1:0]	
Type	R	R	R/W	R/W	R	R	R/W	
Reset	0	0	0	0	0	0	1	0

SFR Address = 0x9B; SFR Page = 0x00

Bit	Name	Function
7:6	Unused	Read = 00b, Write = Don't Care.
5	CP0RIE	Comparator0 Rising-Edge Interrupt Enable. 0: Comparator0 Rising-edge interrupt disabled. 1: Comparator0 Rising-edge interrupt enabled.
4	CP0FIE	Comparator0 Falling-Edge Interrupt Enable. 0: Comparator0 Falling-edge interrupt disabled. 1: Comparator0 Falling-edge interrupt enabled.
3:2	Unused	Read = 00b, Write = don't care.
1:0	CP0MD[1:0]	Comparator0 Mode Select. These bits affect the response time and power consumption for Comparator0. 00: Mode 0 (Fastest Response Time, Highest Power Consumption) 01: Mode 1 10: Mode 2 11: Mode 3 (Slowest Response Time, Lowest Power Consumption)

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15.1.3. Flash Write Procedure

Flash bytes are programmed by software with the following sequence:

1. Disable interrupts (recommended).
2. Erase the 512-byte Flash page containing the target location, as described in Section 15.1.2.
3. Set the PSWE bit (register PSCTL).
4. Clear the PSEE bit (register PSCTL).
5. Write the first key code to FLKEY: 0xA5.
6. Write the second key code to FLKEY: 0xF1.
7. Using the MOVX instruction, write a single data byte to the desired location within the 512-byte sector.
8. Clear the PSWE bit.

Steps 5–7 must be repeated for each byte to be written. After Flash writes are complete, PSWE should be cleared so that MOVX instructions do not target program memory.

15.1.4. Flash Write Optimization

The Flash write procedure includes a block write option to optimize the time to perform consecutive byte writes. When block write is enabled by setting the CHBLKW bit (CCH0CN.0), writes to two consecutive bytes in Flash require the same amount of time as a single byte write. This is performed by caching the first byte that is written to Flash and then committing both bytes to Flash when the second byte is written. When block writes are enabled, if the second write does not occur, the first data byte written is not actually written to Flash. Flash bytes with block write enabled are programmed by software with the following sequence:

1. Disable interrupts (recommended).
2. Erase the 512-byte Flash page containing the target location, as described in Section 15.1.2.
3. Set the CHBLKW bit (register CCH0CN).
4. Set the PSWE bit (register PSCTL).
5. Clear the PSEE bit (register PSCTL).
6. Write the first key code to FLKEY: 0xA5.
7. Write the second key code to FLKEY: 0xF1.
8. Using the MOVX instruction, write the first data byte to the desired location within the 512-byte sector.
9. Write the first key code to FLKEY: 0xA5.
10. Write the second key code to FLKEY: 0xF1.
11. Using the MOVX instruction, write the second data byte to the desired location within the 512-byte sector. The location of the second byte must be the next higher address from the first data byte.
12. Clear the PSWE bit.
13. Clear the CHBLKW bit.

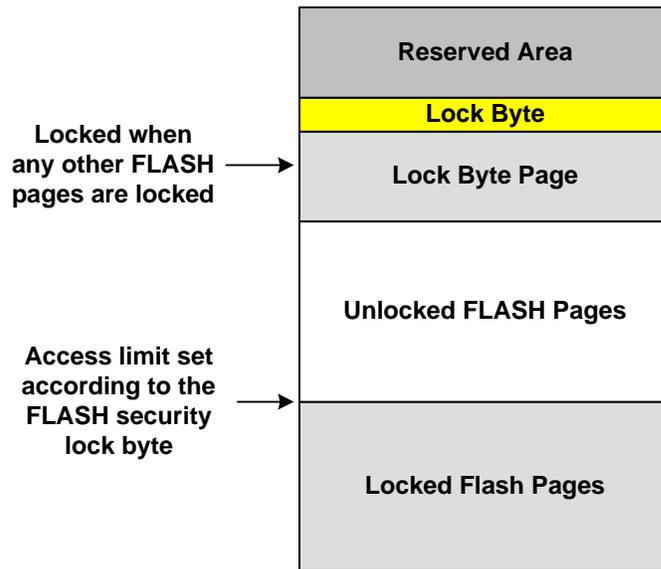
15.2. Non-volatile Data Storage

The Flash memory can be used for non-volatile data storage as well as program code. This allows data such as calibration coefficients to be calculated and stored at run time. Data is written using the MOVX write instruction and read using the MOVC instruction. Note: MOVX read instructions always target XRAM.

15.3. Security Options

The CIP-51 provides security options to protect the Flash memory from inadvertent modification by software as well as to prevent the viewing of proprietary program code and constants. The Program Store Write Enable (bit PSWE in register PSCTL) and the Program Store Erase Enable (bit PSEE in register PSCTL) bits protect the Flash memory from accidental modification by software. PSWE must be explicitly set to 1 before software can modify the Flash memory; both PSWE and PSEE must be set to 1 before software can erase Flash memory. Additional security features prevent proprietary program code and data constants from being read or altered across the C2 interface.

A Security Lock Byte located at the last byte of Flash user space offers protection of the Flash program memory from access (reads, writes, or erases) by unprotected code or the C2 interface. The Flash security mechanism allows the user to lock n 512-byte Flash pages, starting at page 0 (addresses 0x0000 to 0x01FF), where n is the ones complement number represented by the Security Lock Byte. **Note that the page containing the Flash Security Lock Byte is unlocked when no other Flash pages are locked (all bits of the Lock Byte are 1) and locked when any other Flash pages are locked (any bit of the Lock Byte is 0).** See example in Figure 15.1.



Security Lock Byte:	11111101b
1s Complement:	00000010b
Flash pages locked:	3 (First two Flash pages + Lock Byte Page)

Figure 15.1. Flash Program Memory Map

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SFR Definition 17.1. VDM0CN: V_{DD} Monitor Control

Bit	7	6	5	4	3	2	1	0
Name	VDMEN	VDDSTAT	VDMLVL					
Type	R/W	R	R/W	R	R	R	R	R
Reset	Varies	Varies	0	0	0	0	0	0

SFR Address = 0xFF; SFR Page = 0x00

Bit	Name	Function
7	VDMEN	V_{DD} Monitor Enable. This bit turns the V _{DD} monitor circuit on/off. The V _{DD} Monitor cannot generate system resets until it is also selected as a reset source in register RSTSRC (SFR Definition 17.2). Selecting the V _{DD} monitor as a reset source before it has stabilized may generate a system reset. In systems where this reset would be undesirable, a delay should be introduced between enabling the V _{DD} Monitor and selecting it as a reset source. See Table 5.4 for the minimum V _{DD} Monitor turn-on time. 0: V _{DD} Monitor Disabled. 1: V _{DD} Monitor Enabled.
6	VDDSTAT	V_{DD} Status. This bit indicates the current power supply status (V _{DD} Monitor output). 0: V _{DD} is at or below the V _{DD} monitor threshold. 1: V _{DD} is above the V _{DD} monitor threshold.
5	VDMLVL	V_{DD} Monitor Level Select. 0: V _{DD} Monitor Threshold is set to VRST-LOW 1: V _{DD} Monitor Threshold is set to VRST-HIGH. This setting is required for any system includes code that writes to and/or erases Flash.
4:0	Unused	Read = 00000b; Write = Don't care.

17.3. External Reset

The external \overline{RST} pin provides a means for external circuitry to force the device into a reset state. Asserting an active-low signal on the \overline{RST} pin generates a reset; an external pullup and/or decoupling of the \overline{RST} pin may be necessary to avoid erroneous noise-induced resets. See Table 5.4 for complete \overline{RST} pin specifications. The PINRSF flag (RSTSRC.0) is set on exit from an external reset.

17.4. Missing Clock Detector Reset

The Missing Clock Detector (MCD) is a one-shot circuit that is triggered by the system clock. If the system clock remains high or low for more than the value specified in Table 5.4, "Reset Electrical Characteristics," on page 46, the one-shot will time out and generate a reset. After a MCD reset, the MCDRSF flag (RSTSRC.2) will read 1, signifying the MCD as the reset source; otherwise, this bit reads 0. Writing a 1 to the MCDRSF bit enables the Missing Clock Detector; writing a 0 disables it. The state of the \overline{RST} pin is unaffected by this reset.

18.6.2.3. 8-bit MOVX with Bank Select: EMI0CF[4:2] = 010

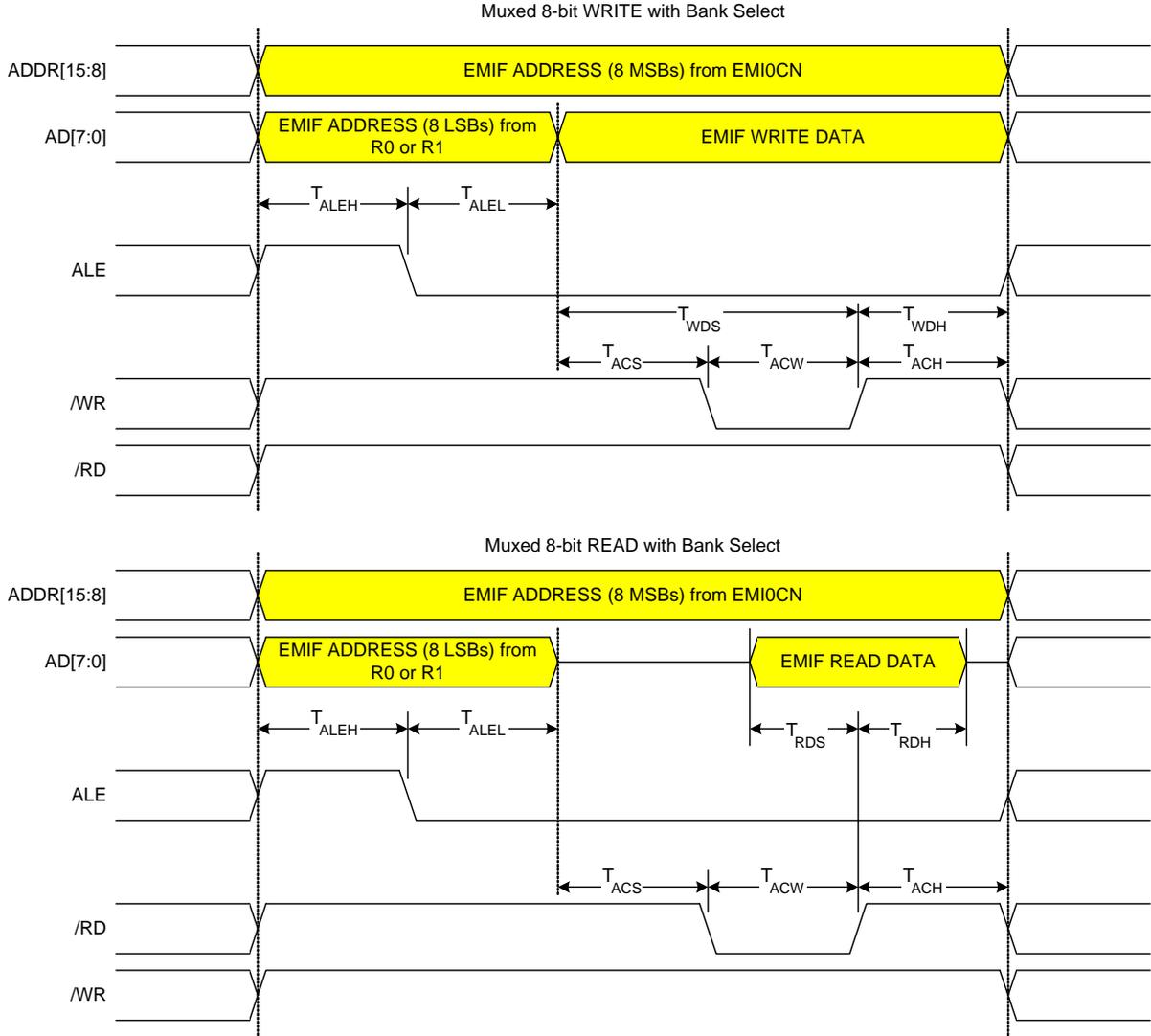


Figure 18.9. Multiplexed 8-bit MOVX with Bank Select Timing

Table 21.3. Autobaud Parameters Examples

System Clock (MHz)	Prescaler	Divider
25	1	312
24.5	1	306
24	1	300
22.1184	1	276
16	1	200
12.25	0	306
12	0	300
11.0592	0	276
8	0	200

21.3. LIN Master Mode Operation

The master node is responsible for the scheduling of messages and sends the header of each frame containing the SYNCH BREAK FIELD, SYNCH FIELD, and IDENTIFIER FIELD. The steps to schedule a message transmission or reception are listed below.

1. Load the 6-bit Identifier into the LIN0ID register.
2. Load the data length into the LIN0SIZE register. Set the value to the number of data bytes or "1111b" if the data length should be decoded from the identifier. Also, set the checksum type, classic or enhanced, in the same LIN0SIZE register.
3. Set the data direction by setting the TXRX bit (LIN0CTRL.5). Set the bit to 1 to perform a master transmit operation, or set the bit to 0 to perform a master receive operation.
4. If performing a master transmit operation, load the data bytes to transmit into the data buffer (LIN0DT1 to LIN0DT8).
5. Set the STREQ bit (LIN0CTRL.0) to start the message transfer. The LIN controller will schedule the message frame and request an interrupt if the message transfer is successfully completed or if an error has occurred.

This code segment shows the procedure to schedule a message in a transmission operation:

```

LIN0ADR = 0x08;           // Point to LIN0CTRL
LIN0DAT |= 0x20;         // Select to transmit data
LIN0ADR = 0x0E;         // Point to LIN0ID
LIN0DAT = 0x11;         // Load the ID, in this example 0x11
LIN0ADR = 0x0B;         // Point to LIN0SIZE
LIN0DAT = ( LIN0DAT & 0xF0 ) | 0x08; // Load the size with 8

LIN0ADR = 0x00;         // Point to Data buffer first byte
for (i=0; i<8; i++)
{
    LIN0DAT = i + 0x41; // Load the buffer with 'A', 'B', ...
    LIN0ADR++;         // Increment the address to the next buffer
}
LIN0ADR = 0x08;         // Point to LIN0CTRL
LIN0DAT = 0x01;         // Start Request
    
```

The application should perform the following steps when an interrupt is requested.

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LIN Register Definition 21.7. LIN0ERR: LIN0 Error Register

Bit	7	6	5	4	3	2	1	0
Name				SYNCH	PRTY	TOUT	CHK	BITERR
Type	R	R	R	R	R	R	R	R
Reset	0	0	0	0	0	0	0	0

Indirect Address = 0x0A

Bit	Name	Function
7:5	Unused	Read = 000b; Write = Don't Care
4	SYNCH	Synchronization Error Bit (slave mode only). 0: No error with the SYNCH FIELD has been detected. 1: Edges of the SYNCH FIELD are outside of the maximum tolerance.
3	PRTY	Parity Error Bit (slave mode only). 0: No parity error has been detected. 1: A parity error has been detected.
2	TOUT	Timeout Error Bit. 0: A timeout error has not been detected. 1: A timeout error has been detected. This error is detected whenever one of the following conditions is met: <ul style="list-style-type: none"> The master is expecting data from a slave and the slave does not respond. The slave is expecting data but no data is transmitted on the bus. A frame is not finished within the maximum frame length. The application does not set the DTACK bit (LIN0CTRL.4) or STOP bit (LIN0CTRL.7) until the end of the reception of the first byte after the identifier.
1	CHK	Checksum Error Bit. 0: Checksum error has not been detected. 1: Checksum error has been detected.
0	BITERR	Bit Transmission Error Bit. 0: No error in transmission has been detected. 1: The bit value monitored during transmission is different than the bit value sent.

23. SMBus

The SMBus I/O interface is a two-wire, bi-directional serial bus. The SMBus is compliant with the System Management Bus Specification, version 1.1, and compatible with the I2C serial bus. Reads and writes to the interface by the system controller are byte oriented with the SMBus interface autonomously controlling the serial transfer of the data. Data can be transferred at up to 1/20th of the system clock as a master or slave (this can be faster than allowed by the SMBus specification, depending on the system clock used). A method of extending the clock-low duration is available to accommodate devices with different speed capabilities on the same bus.

The SMBus interface may operate as a master and/or slave, and may function on a bus with multiple masters. The SMBus provides control of SDA (serial data), SCL (serial clock) generation and synchronization, arbitration logic, and START/STOP control and generation. A block diagram of the SMBus peripheral and the associated SFRs is shown in Figure 23.1.

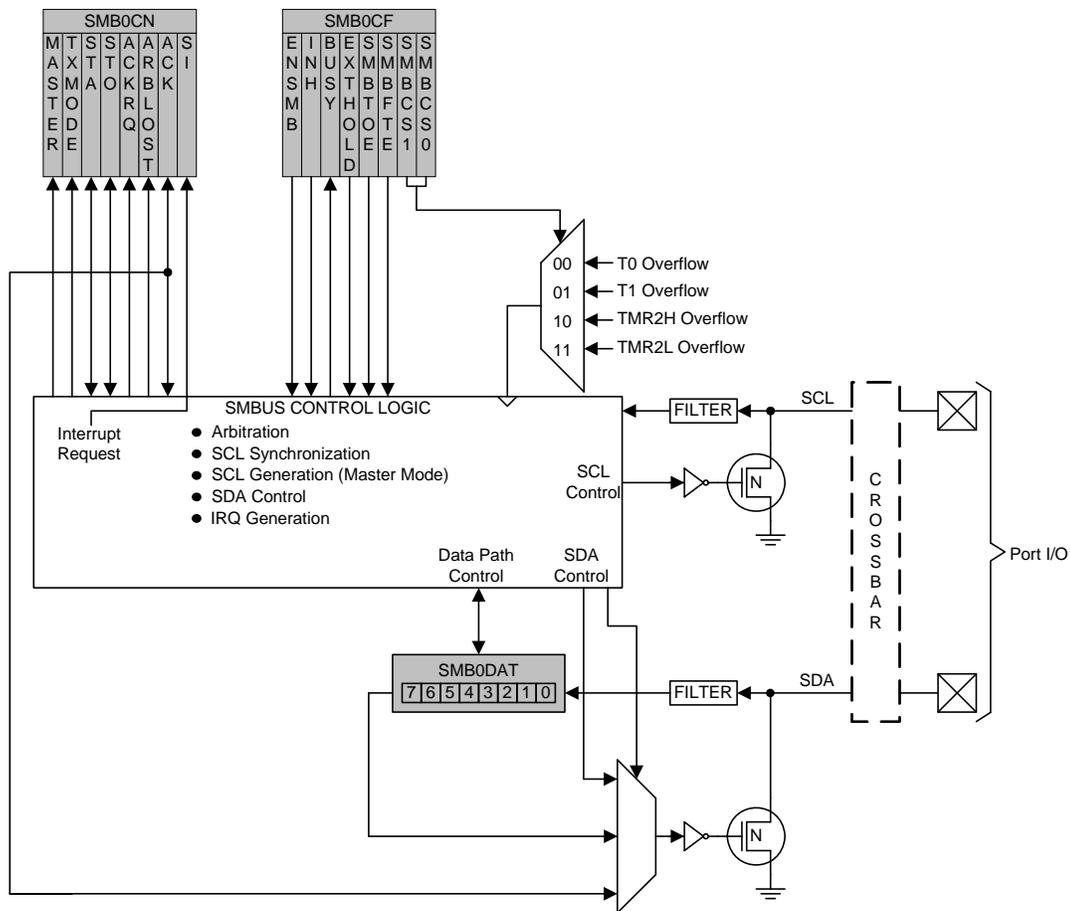


Figure 23.1. SMBus Block Diagram

24. UART0

UART0 is an asynchronous, full duplex serial port offering a variety of data formatting options. A dedicated baud rate generator with a 16-bit timer and selectable prescaler is included, which can generate a wide range of baud rates (details in Section “24.1. Baud Rate Generator” on page 243). A received data FIFO allows UART0 to receive up to three data bytes before data is lost and an overflow occurs.

UART0 has six associated SFRs. Three are used for the Baud Rate Generator (SBCON0, SBRLH0, and SBRL0), two are used for data formatting, control, and status functions (SCON0, SMOD0), and one is used to send and receive data (SBUF0). The single SBUF0 location provides access to both transmit and receive registers. **Writes to SBUF0 always access the Transmit register. Reads of SBUF0 always access the buffered Receive register; it is not possible to read data from the Transmit register.**

With UART0 interrupts enabled, an interrupt is generated each time a transmit is completed (TI0 is set in SCON0), or a data byte has been received (RI0 is set in SCON0). The UART0 interrupt flags are not cleared by hardware when the CPU vectors to the interrupt service routine. They must be cleared manually by software, allowing software to determine the cause of the UART0 interrupt (transmit complete or receive complete). If additional bytes are available in the Receive FIFO, the RI0 bit cannot be cleared by software.

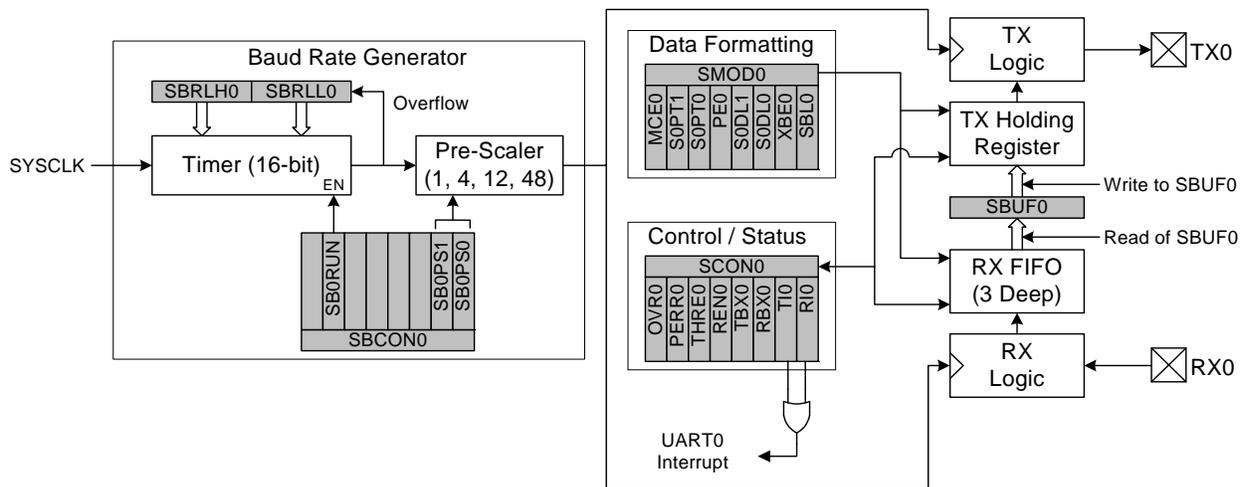


Figure 24.1. UART0 Block Diagram

24.1. Baud Rate Generator

The UART0 baud rate is generated by a dedicated 16-bit timer which runs from the controller’s core clock (SYSCLK) and has prescaler options of 1, 4, 12, or 48. The timer and prescaler options combined allow for a wide selection of baud rates over many clock frequencies.

The baud rate generator is configured using three registers: SBCON0, SBRLH0, and SBRL0. The UART0 Baud Rate Generator Control Register (SBCON0, SFR Definition 24.4) enables or disables the baud rate generator, selects the clock source for the baud rate generator, and selects the prescaler value for the timer. The baud rate generator must be enabled for UART0 to function. Registers SBRLH0 and SBRL0 contain a 16-bit reload value for the dedicated 16-bit timer. The internal timer counts up from the reload value on every clock tick. On timer overflows (0xFFFF to 0x0000), the timer is reloaded. The baud rate for UART0 is defined in Equation 24.1, where “BRG Clock” is the baud rate generator’s selected clock source. For reliable UART operation, it is recommended that the UART baud rate is not configured for baud rates faster than SYSCLK/16.

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SFR Definition 26.1. CKCON: Clock Control

Bit	7	6	5	4	3	2	1	0
Name	T3MH	T3ML	T2MH	T2ML	T1M	T0M	SCA[1:0]	
Type	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8E; SFR Page = All Pages

Bit	Name	Function
7	T3MH	Timer 3 High Byte Clock Select. Selects the clock supplied to the Timer 3 high byte (split 8-bit timer mode only). 0: Timer 3 high byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 high byte uses the system clock.
6	T3ML	Timer 3 Low Byte Clock Select. Selects the clock supplied to Timer 3. Selects the clock supplied to the lower 8-bit timer in split 8-bit timer mode. 0: Timer 3 low byte uses the clock defined by the T3XCLK bit in TMR3CN. 1: Timer 3 low byte uses the system clock.
5	T2MH	Timer 2 High Byte Clock Select. Selects the clock supplied to the Timer 2 high byte (split 8-bit timer mode only). 0: Timer 2 high byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 high byte uses the system clock.
4	T2ML	Timer 2 Low Byte Clock Select. Selects the clock supplied to Timer 2. If Timer 2 is configured in split 8-bit timer mode, this bit selects the clock supplied to the lower 8-bit timer. 0: Timer 2 low byte uses the clock defined by the T2XCLK bit in TMR2CN. 1: Timer 2 low byte uses the system clock.
3	T1	Timer 1 Clock Select. Selects the clock source supplied to Timer 1. Ignored when C/T1 is set to 1. 0: Timer 1 uses the clock defined by the prescale bits SCA[1:0]. 1: Timer 1 uses the system clock.
2	T0	Timer 0 Clock Select. Selects the clock source supplied to Timer 0. Ignored when C/T0 is set to 1. 0: Counter/Timer 0 uses the clock defined by the prescale bits SCA[1:0]. 1: Counter/Timer 0 uses the system clock.
1:0	SCA[1:0]	Timer 0/1 Prescale Bits. These bits control the Timer 0/1 Clock Prescaler: 00: System clock divided by 12 01: System clock divided by 4 10: System clock divided by 48 11: External clock divided by 8 (synchronized with the system clock)

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SFR Definition 26.6. TH0: Timer 0 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH0[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8C; SFR Page = All Pages

Bit	Name	Function
7:0	TH0[7:0]	Timer 0 High Byte. The TH0 register is the high byte of the 16-bit Timer 0.

SFR Definition 26.7. TH1: Timer 1 High Byte

Bit	7	6	5	4	3	2	1	0
Name	TH1[7:0]							
Type	R/W							
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8D; SFR Page = All Pages

Bit	Name	Function
7:0	TH1[7:0]	Timer 1 High Byte. The TH1 register is the high byte of the 16-bit Timer 1.

Table 27.2. PCA0CPM and PCA0PWM Bit Settings for PCA Capture/Compare Modules

Operational Mode	PCA0CPMn								PCA0PWM				
	7	6	5	4	3	2	1	0	7	6	5	4-2	1-0
Capture triggered by positive edge on CEXn	X	X	1	0	0	0	0	A	0	X	B	XXX	XX
Capture triggered by negative edge on CEXn	X	X	0	1	0	0	0	A	0	X	B	XXX	XX
Capture triggered by any transition on CEXn	X	X	1	1	0	0	0	A	0	X	B	XXX	XX
Software Timer	X	C	0	0	1	0	0	A	0	X	B	XXX	XX
High Speed Output	X	C	0	0	1	1	0	A	0	X	B	XXX	XX
Frequency Output	X	C	0	0	0	1	1	A	0	X	B	XXX	XX
8-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	0	X	B	XXX	00
9-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	01
10-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	10
11-Bit Pulse Width Modulator (Note 7)	0	C	0	0	E	0	1	A	D	X	B	XXX	11
16-Bit Pulse Width Modulator	1	C	0	0	E	0	1	A	0	X	B	XXX	XX

Notes:

1. X = Don't Care (no functional difference for individual module if 1 or 0).
2. A = 1 to enable interrupts for this module (PCA interrupt triggered on CCFn set to 1).
3. B = 1 to enable 8th, 9th, 10th or 11th bit overflow interrupt (Depends on setting of CLSEL[1:0]).
4. C = When set to 0, the digital comparator is off. For high speed and frequency output modes, the associated pin will not toggle. In any of the PWM modes, this generates a 0% duty cycle (output = 0).
5. D = Selects whether the Capture/Compare register (0) or the Auto-Reload register (1) for the associated channel is accessed via addresses PCA0CPHn and PCA0CPLn.
6. E = When set to 1, a match event will cause the CCFn flag for the associated channel to be set.
7. All modules set to 8, 9, 10 or 11-bit PWM mode use the same cycle length setting.

27.3.1. Edge-triggered Capture Mode

In this mode, a valid transition on the CEXn pin causes the PCA to capture the value of the PCA counter/timer and load it into the corresponding module's 16-bit capture/compare register (PCA0CPLn and PCA0CPHn). The CAPPn and CAPNn bits in the PCA0CPMn register are used to select the type of transition that triggers the capture: low-to-high transition (positive edge), high-to-low transition (negative edge), or either transition (positive or negative edge). When a capture occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. If both CAPPn and CAPNn bits are set to logic 1, then the state of the Port pin associated with CEXn can be read directly to determine whether a rising-edge or falling-edge caused the capture.

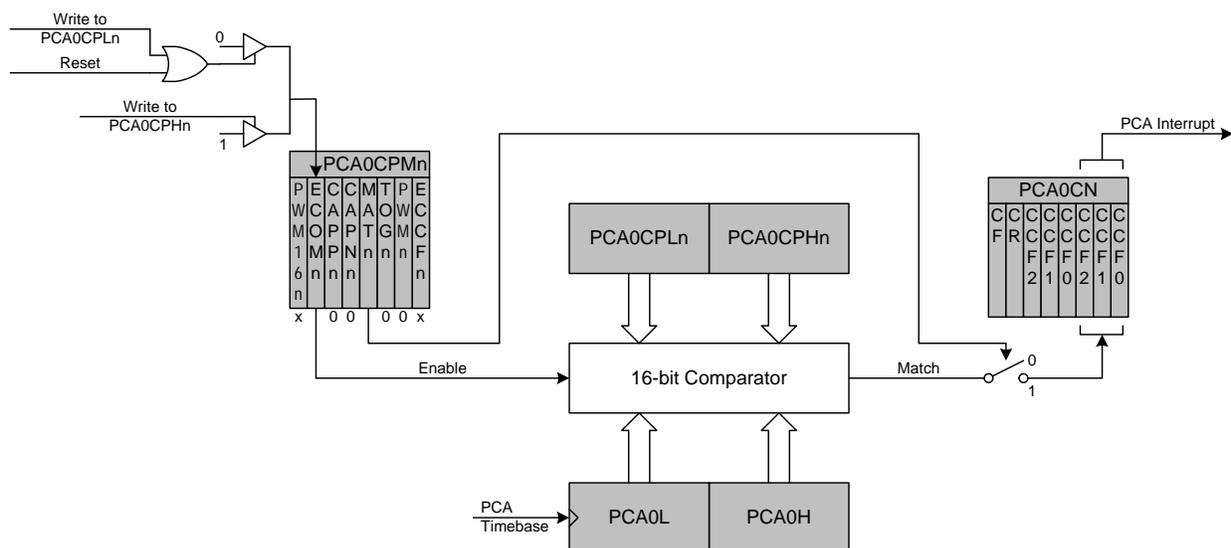


Figure 27.5. PCA Software Timer Mode Diagram

27.3.3. High-Speed Output Mode

In High-Speed Output mode, a module's associated CEXn pin is toggled each time a match occurs between the PCA Counter and the module's 16-bit capture/compare register (PCA0CPHn and PCA0CPLn). When a match occurs, the Capture/Compare Flag (CCFn) in PCA0CN is set to logic 1. An interrupt request is generated if the CCFn interrupt for that module is enabled. The CCFn bit is not automatically cleared by hardware when the CPU vectors to the interrupt service routine, and must be cleared by software. Setting the TOGn, MATn, and ECOMn bits in the PCA0CPMn register enables the High-Speed Output mode. If ECOMn is cleared, the associated pin will retain its state, and not toggle on the next match event.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

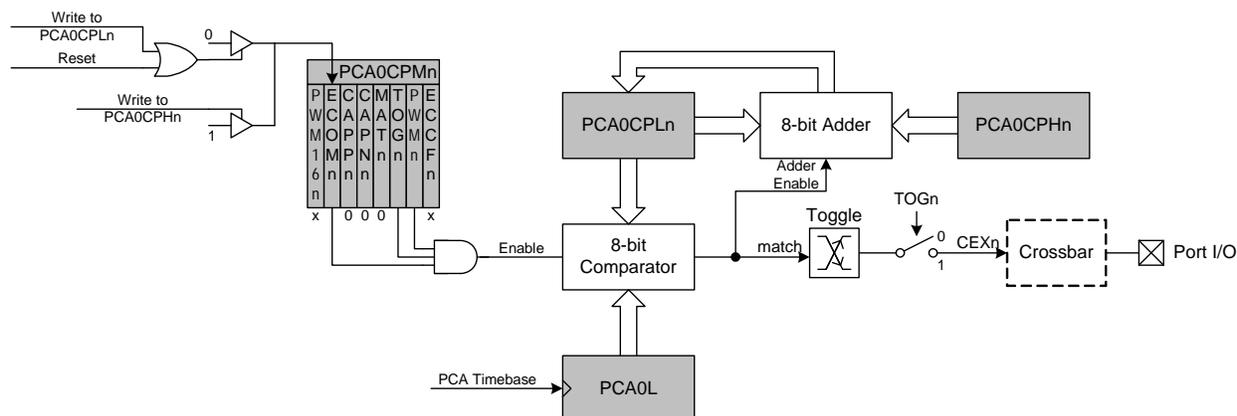


Figure 27.7. PCA Frequency Output Mode

27.3.5. 8-bit, 9-bit, 10-bit and 11-bit Pulse Width Modulator Modes

Each module can be used independently to generate a pulse width modulated (PWM) output on its associated CEXn pin. The frequency of the output is dependent on the timebase for the PCA counter/timer, and the setting of the PWM cycle length (8, 9, 10 or 11-bits). For backwards-compatibility with the 8-bit PWM mode available on other devices, the 8-bit PWM mode operates slightly different than 9, 10 and 11-bit PWM modes. **It is important to note that all channels configured for 8/9/10/11-bit PWM mode will use the same cycle length.** It is not possible to configure one channel for 8-bit PWM mode and another for 11-bit mode (for example). However, other PCA channels can be configured to Pin Capture, High-Speed Output, Software Timer, Frequency Output, or 16-bit PWM mode independently.

27.3.5.1. 8-bit Pulse Width Modulator Mode

The duty cycle of the PWM output signal in 8-bit PWM mode is varied using the module's PCA0CPLn capture/compare register. When the value in the low byte of the PCA counter/timer (PCA0L) is equal to the value in PCA0CPLn, the output on the CEXn pin will be set. When the count value in PCA0L overflows, the CEXn output will be reset (see Figure 27.8). Also, when the counter/timer low byte (PCA0L) overflows from 0xFF to 0x00, PCA0CPLn is reloaded automatically with the value stored in the module's capture/compare high byte (PCA0CPHn) without software intervention. Setting the ECOMn and PWMn bits in the PCA0CPMn register, and setting the CLSEL bits in register PCA0PWM to 00b enables 8-Bit Pulse Width Modulator mode. If the MATn bit is set to 1, the CCFn flag for the module will be set each time an 8-bit comparator match (rising edge) occurs. The COVF flag in PCA0PWM can be used to detect the overflow (falling edge), which will occur every 256 PCA clock cycles. The duty cycle for 8-Bit PWM Mode is given in Equation 27.2.

Important Note About Capture/Compare Registers: When writing a 16-bit value to the PCA0 Capture/Compare registers, the low byte should always be written first. Writing to PCA0CPLn clears the ECOMn bit to 0; writing to PCA0CPHn sets ECOMn to 1.

$$\text{Duty Cycle} = \frac{(256 - \text{PCA0CPHn})}{256}$$

Equation 27.2. 8-Bit PWM Duty Cycle

Using Equation 27.2, the largest duty cycle is 100% (PCA0CPHn = 0), and the smallest duty cycle is 0.39% (PCA0CPHn = 0xFF). A 0% duty cycle may be generated by clearing the ECOMn bit to 0.