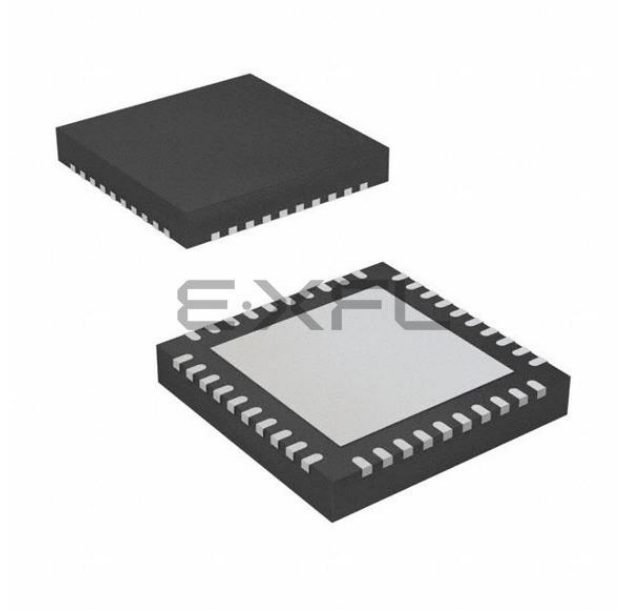

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, SMBus (2-Wire/I²C), CANbus, LINbus, SPI, UART/USART
Peripherals	POR, PWM, Temp Sensor, WDT
Number of I/O	33
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	4.25K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.25V
Data Converters	A/D 32x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	40-VFQFN Exposed Pad
Supplier Device Package	40-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/c8051f508-im

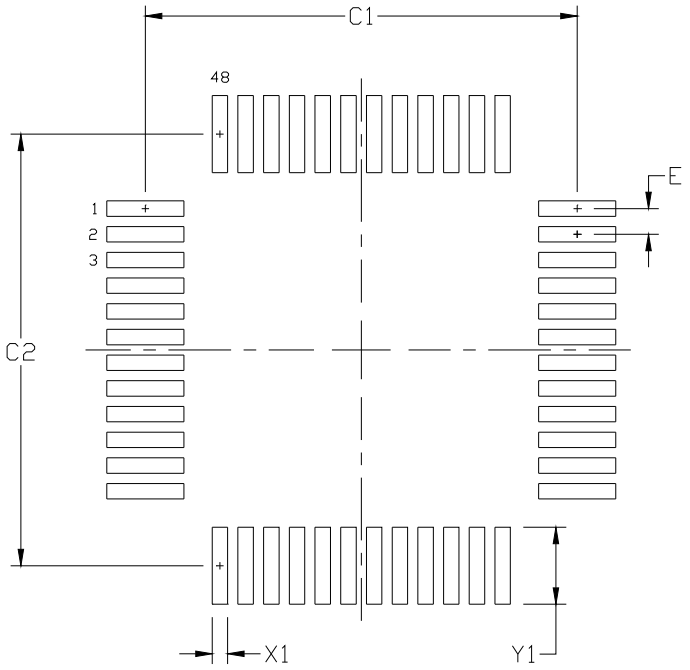

Figure 4.2. QFP-48 Landing Diagram

Table 4.2. QFP-48 Landing Diagram Dimensions

Dimension	Min	Max		Dimension	Min	Max
C1	8.30	8.40		X1	0.20	0.30
C2	8.30	8.40		Y1	1.40	1.50
E	0.50 BSC					

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. This Land Pattern Design is based on the IPC-7351 guidelines.

Solder Mask Design

3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60µm minimum, all the way around the pad.

Stencil Design

4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
5. The stencil thickness should be 0.125mm (5 mils).
6. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.

Card Assembly

7. A No-Clean, Type-3 solder paste is recommended.
8. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

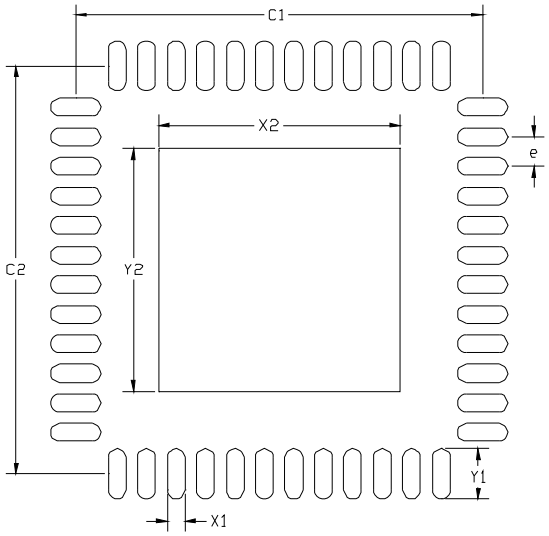

Figure 4.4. QFN-48 Landing Diagram

Table 4.4. QFN-48 Landing Diagram Dimensions

Dimension	Min	Max		Dimension	Min	Max
C1	6.80	6.90		X2	4.00	4.10
C2	6.80	6.90		Y1	0.75	0.85
e	0.50 BSC			Y2	4.00	4.10
X1	0.20	0.30				

Notes:

General

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimension and Tolerancing is per the ANSI Y14.5M-1994 specification.
3. This Land Pattern Design is based on the IPC-SM-7351 guidelines.
4. All dimensions shown are at Maximum Material Condition (MMC). Least Material Condition (LMC) is calculated based on a Fabrication Allowance of 0.05 mm.

Solder Mask Design

5. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

6. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
7. The stencil thickness should be 0.125 mm (5 mils).
8. The ratio of stencil aperture to land pad size should be 1:1 for all perimeter pads.
9. A 3x3 array of 1.20 mm x 1.10 mm openings on a 1.40 mm pitch should be used for the center pad.

Card Assembly

10. A No-Clean, Type-3 solder paste is recommended.
11. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

4.4. QFP-32 Package Specifications

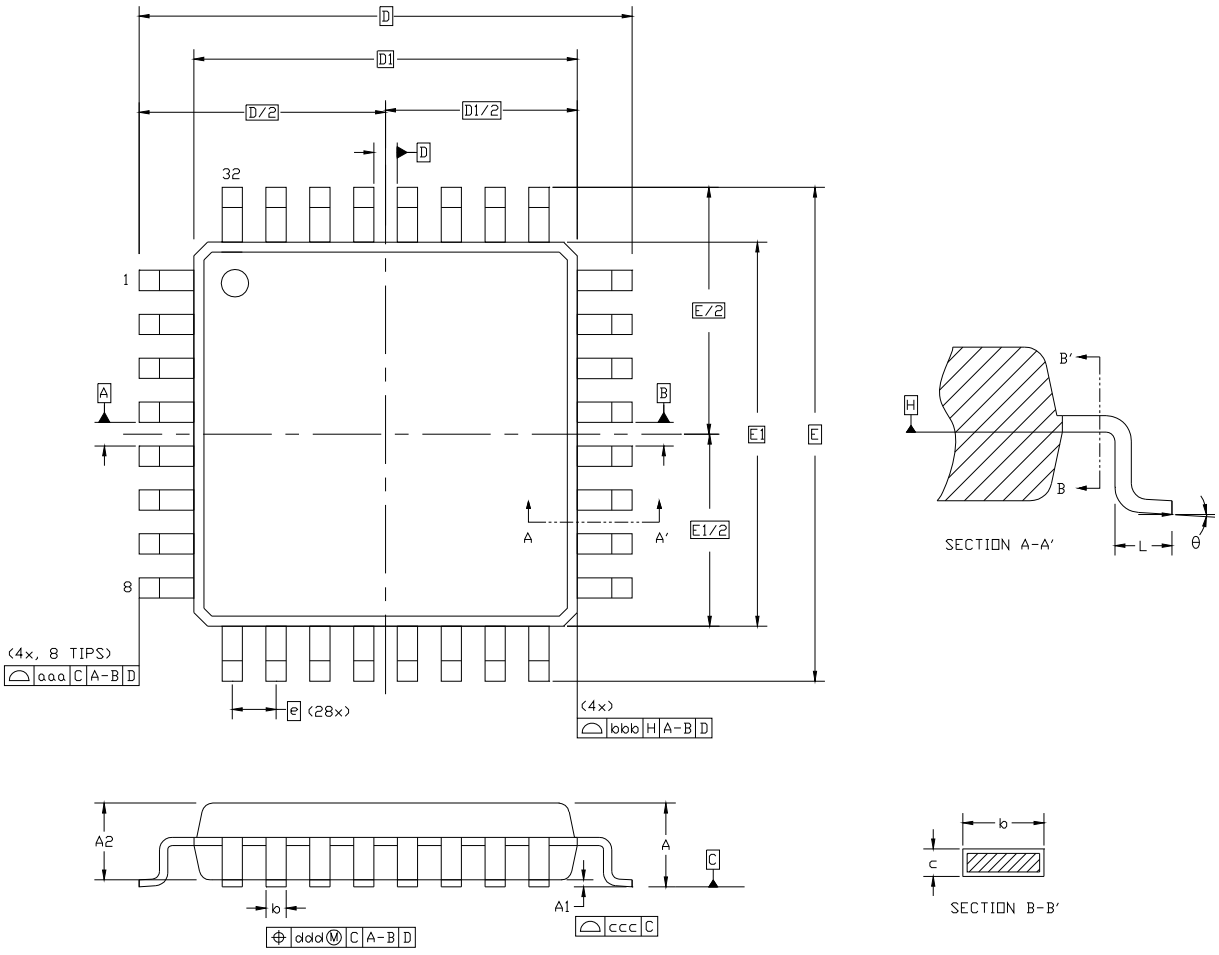

Figure 4.7. QFP-32 Package Drawing

Table 4.7. QFP-32 Package Dimensions

Dimension	Min	Typ	Max
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.30	0.37	0.45
c	0.09	—	0.20
D	9.00 BSC.		
D1	7.00 BSC.		
e	0.80 BSC.		

Dimension	Min	Typ	Max
E	9.00 BSC.		
E1	7.00 BSC.		
L	0.45	0.60	0.75
aaa	0.20		
bbb	0.20		
ccc	0.10		
ddd	0.20		
θ	0°	3.5°	7°

Notes:

1. All dimensions shown are in millimeters (mm) unless otherwise noted.
2. Dimensioning and Tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC outline MS-026, variation BBA.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for Small Body Components.

6.3.2. Setting the Gain Value

The three programmable gain registers are accessed indirectly using the ADC0H and ADC0L registers when the GAINEN bit (ADC0CF.0) bit is set. ADC0H acts as the address register, and ADC0L is the data register. The programmable gain registers can only be written to and cannot be read. See Gain Register Definition 6.1, Gain Register Definition 6.2, and Gain Register Definition 6.3 for more information.

The gain is programmed using the following steps:

1. Set the GAINEN bit (ADC0CF.0)
2. Load the ADC0H with the ADC0GNH, ADC0GNL, or ADC0GNA address.
3. Load ADC0L with the desired value for the selected gain register.
4. Reset the GAINEN bit (ADC0CF.0)

Notes:

1. An ADC conversion should not be performed while the GAINEN bit is set.
2. Even with gain enabled, the maximum input voltage must be less than V_{REGIN} and the maximum voltage of the signal after gain must be less than or equal to V_{REF}.

In code, changing the value to 0.44 gain from the previous example looks like:

```
// in 'C':
ADC0CF |= 0x01;          // GAINEN = 1
ADC0H = 0x04;            // Load the ADC0GNH address
ADC0L = 0x6C;            // Load the upper byte of 0x6CA to ADC0GNH
ADC0H = 0x07;            // Load the ADC0GNL address
ADC0L = 0xA0;            // Load the lower nibble of 0x6CA to ADC0GNL
ADC0H = 0x08;            // Load the ADC0GNA address
ADC0L = 0x01;            // Set the GAINADD bit
ADC0CF &= ~0x01;         // GAINEN = 0

; in assembly
ORL ADC0CF,#01H          ; GAINEN = 1
MOV ADC0H,#04H           ; Load the ADC0GNH address
MOV ADC0L,#06CH          ; Load the upper byte of 0x6CA to ADC0GNH
MOV ADC0H,#07H           ; Load the ADC0GNL address
MOV ADC0L,#0A0H          ; Load the lower nibble of 0x6CA to ADC0GNL
MOV ADC0H,#08H           ; Load the ADC0GNA address
MOV ADC0L,#01H           ; Set the GAINADD bit
ANL ADC0CF,#0FEH         ; GAINEN = 0
```

SFR Definition 9.4. CPT1MD: Comparator1 Mode Selection

Bit	7	6	5	4	3	2	1	0
Name			CP1RIE	CP1FIE			CP1MD[1:0]	
Type	R	R	R/W	R/W	R	R	R/W	
Reset	0	0	0	0	0	0	1	0

SFR Address = 0x9E; SFR Page = 0x00

Bit	Name	Function
7:6	Unused	Read = 00b, Write = Don't Care.
5	CP1RIE	**Comparator1 Rising-Edge Interrupt Enable.** 0: Comparator1 Rising-edge interrupt disabled. 1: Comparator1 Rising-edge interrupt enabled.
4	CP1FIE	**Comparator1 Falling-Edge Interrupt Enable.** 0: Comparator1 Falling-edge interrupt disabled. 1: Comparator1 Falling-edge interrupt enabled.
3:2	Unused	Read = 00b, Write = don't care.
1:0	CP1MD[1:0]	**Comparator1 Mode Select.** These bits affect the response time and power consumption for Comparator1. 00: Mode 0 (Fastest Response Time, Highest Power Consumption) 01: Mode 1 10: Mode 2 11: Mode 3 (Slowest Response Time, Lowest Power Consumption)

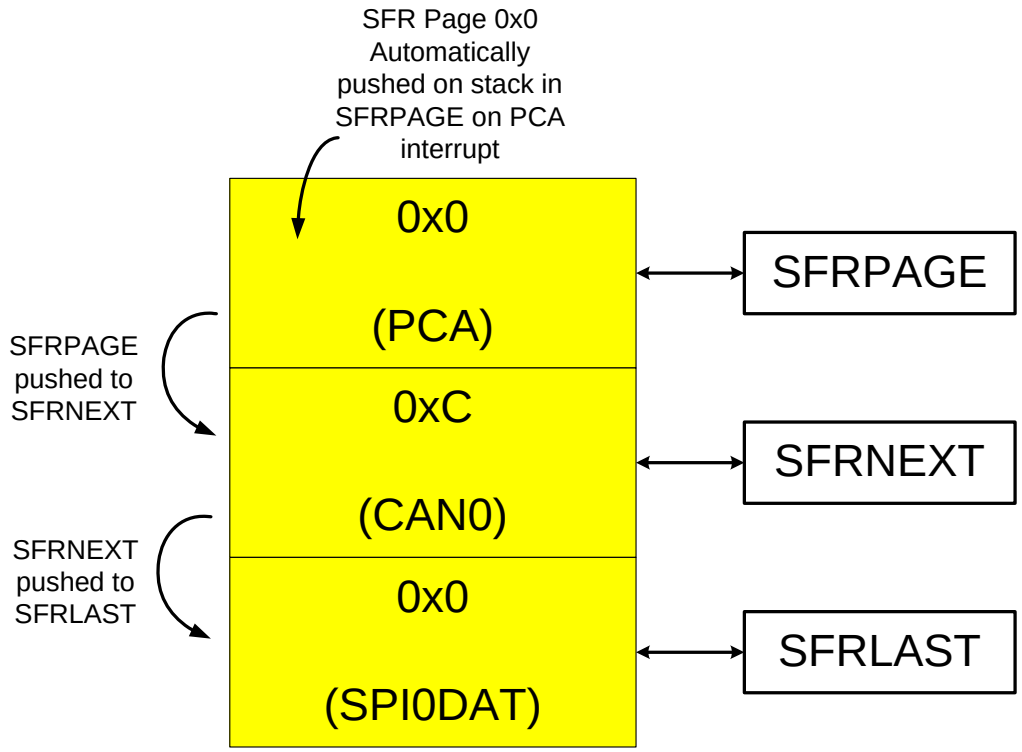

Figure 13.4. SFR Page Stack Upon PCA Interrupt Occurring During a CAN0 ISR

On exit from the PCA interrupt service routine, the CIP-51 will return to the CAN0 ISR. On execution of the RETI instruction, SFR Page 0x00 used to access the PCA registers will be automatically popped off of the SFR Page Stack, and the contents of the SFRNEXT register will be moved to the SFRPAGE register. Software in the CAN0 ISR can continue to access SFRs as it did prior to the PCA interrupt. Likewise, the contents of SFRLAST are moved to the SFRNEXT register. Recall this was the SFR Page value 0x00 being used to access SPI0DAT before the CAN0 interrupt occurred. See Figure 13.5.

Table 13.3. Special Function Registers (Continued)

SFRs are listed in alphabetical order. All undefined SFR locations are reserved

Register	Address	Description	Page
PCA0CPH1	0xEA	PCA Capture 1 High	305
PCA0CPH2	0xEC	PCA Capture 2 High	305
PCA0CPH3	0xEE	PCA Capture 3 High	305
PCA0CPH4	0xFE	PCA Capture 4 High	305
PCA0CPH5	0xCF	PCA Capture 5 High	305
PCA0CPL0	0xFB	PCA Capture 0 Low	305
PCA0CPL1	0xE9	PCA Capture 1 Low	305
PCA0CPL2	0xEB	PCA Capture 2 Low	305
PCA0CPL3	0xED	PCA Capture 3 Low	305
PCA0CPL4	0xFD	PCA Capture 4 Low	305
PCA0CPL5	0xCE	PCA Capture 5 Low	305
PCA0CPM0	0xDA	PCA Module 0 Mode Register	303
PCA0CPM1	0xDB	PCA Module 1 Mode Register	303
PCA0CPM2	0xDC	PCA Module 2 Mode Register	303
PCA0CPM3	0xDD	PCA Module 3 Mode Register	303
PCA0CPM4	0xDE	PCA Module 4 Mode Register	303
PCA0CPM5	0xDF	PCA Module 5 Mode Register	303
PCA0H	0xFA	PCA Counter High	304
PCA0L	0xF9	PCA Counter Low	304
PCA0MD	0xD9	PCA Mode	301
PCA0PWM	0xD9	PCA PWM Configuration	302
PCON	0x87	Power Control	140
PSCTL	0x8F	Program Store R/W Control	134
PSW	0xD0	Program Status Word	95
REF0CN	0xD1	Voltage Reference Control	74
REG0CN	0xD1	Voltage Regulator Control	85
RSTSRC	0xEF	Reset Source Configuration/Status	146
SBCON0	0xAB	UART0 Baud Rate Generator Control	250
SBRLH0	0xAD	UART0 Baud Rate Reload High Byte	251
SBRLL0	0xAC	UART0 Baud Rate Reload Low Byte	251
SBUF0	0x99	UART0 Data Buffer	250
SCON0	0x98	UART0 Control	248
SFR0CN	0x84	SFR Page Control	107
SFRLAST	0x86	SFR Stack Last Page	110
SFRNEXT	0x85	SFR Stack Next Page	109
SFRPAGE	0xA7	SFR Page Select	108

SFR Definition 14.2. IP: Interrupt Priority

Bit	7	6	5	4	3	2	1	0
Name		PSPI0	PT2	PS0	PT1	PX1	PT0	PX0
Type	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Reset	1	0	0	0	0	0	0	0

SFR Address = 0xB8; Bit-Addressable; SFR Page = All Pages

Bit	Name	Function
7	Unused	Read = 1b, Write = Don't Care.
6	PSPI0	**Serial Peripheral Interface (SPI0) Interrupt Priority Control.** This bit sets the priority of the SPI0 interrupt. 0: SPI0 interrupt set to low priority level. 1: SPI0 interrupt set to high priority level.
5	PT2	**Timer 2 Interrupt Priority Control.** This bit sets the priority of the Timer 2 interrupt. 0: Timer 2 interrupt set to low priority level. 1: Timer 2 interrupt set to high priority level.
4	PS0	**UART0 Interrupt Priority Control.** This bit sets the priority of the UART0 interrupt. 0: UART0 interrupt set to low priority level. 1: UART0 interrupt set to high priority level.
3	PT1	**Timer 1 Interrupt Priority Control.** This bit sets the priority of the Timer 1 interrupt. 0: Timer 1 interrupt set to low priority level. 1: Timer 1 interrupt set to high priority level.
2	PX1	**External Interrupt 1 Priority Control.** This bit sets the priority of the External Interrupt 1 interrupt. 0: External Interrupt 1 set to low priority level. 1: External Interrupt 1 set to high priority level.
1	PT0	**Timer 0 Interrupt Priority Control.** This bit sets the priority of the Timer 0 interrupt. 0: Timer 0 interrupt set to low priority level. 1: Timer 0 interrupt set to high priority level.
0	PX0	**External Interrupt 0 Priority Control.** This bit sets the priority of the External Interrupt 0 interrupt. 0: External Interrupt 0 set to low priority level. 1: External Interrupt 0 set to high priority level.

The level of Flash security depends on the Flash access method. The three Flash access methods that can be restricted are reads, writes, and erases from the C2 debug interface, user firmware executing on unlocked pages, and user firmware executing on locked pages. Table 15.1 summarizes the Flash security features of the C8051F50x/F51x devices.

Table 15.1. Flash Security Summary

Action	C2 Debug Interface	User Firmware executing from:	
		an unlocked page	a locked page
Read, Write or Erase unlocked pages (except page with Lock Byte)	Permitted	Permitted	Permitted
Read, Write or Erase locked pages (except page with Lock Byte)	Not Permitted	Flash Error Reset	Permitted
Read or Write page containing Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read or Write page containing Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Read contents of Lock Byte (if no pages are locked)	Permitted	Permitted	Permitted
Read contents of Lock Byte (if any page is locked)	Not Permitted	Flash Error Reset	Permitted
Erase page containing Lock Byte (if no pages are locked)	Permitted	Flash Error Reset	Flash Error Reset
Erase page containing Lock Byte—Unlock all pages (if any page is locked)	C2 Device Erase Only	Flash Error Reset	Flash Error Reset
Lock additional pages (change 1s to 0s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Unlock individual pages (change 0s to 1s in the Lock Byte)	Not Permitted	Flash Error Reset	Flash Error Reset
Read, Write or Erase Reserved Area	Not Permitted	Flash Error Reset	Flash Error Reset

C2 Device Erase—Erases all Flash pages including the page containing the Lock Byte.

Flash Error Reset—Not permitted; Causes Flash Error Device Reset (FERROR bit in RSTSRC is '1' after reset).

- All prohibited operations that are performed via the C2 interface are ignored (do not cause device reset).
- Locking any Flash page also locks the page containing the Lock Byte.
- Once written to, the Lock Byte cannot be modified except by performing a C2 Device Erase.
- If user code writes to the Lock Byte, the Lock does not take effect until the next device reset.

SFR Definition 19.1. CLKSEL: Clock Select

Bit	7	6	5	4	3	2	1	0
Name							CLKSL[1:0]	
Type	R	R	R	R	R	R	R/W	
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x8F; SFR Page = 0x0F;

Bit	Name	Function
7:2	Unused	Read = 000000b; Write = Don't Care
1:0	CLKSL[1:0]	**System Clock Source Select Bits.** 00: SYSCLK derived from the Internal Oscillator and scaled per the IFCN bits in register OSCICN. 01: SYSCLK derived from the External Oscillator circuit. 10: SYSCLK derived from the Clock Multiplier. 11: reserved.

Important Note: If the selected system clock is greater than 25 MHz, please be aware of the following:

- Flash Scale Timing must be configured for the faster system clock. See SFR Definition 15.3 for more details.
- VDD and VDDA voltage must be 2 V or higher.
- It is recommended to enable the VDD monitor as a reset source and configure it for the high threshold. See SFR Definition 17.1 for details on configuring the VDD monitor. If the VDD monitor is configured to the high threshold, the VDD and VDDA voltage must be greater than the VDD monitor high threshold. See Table 5.4 for VDD monitor threshold specifications.

19.4. External Oscillator Drive Circuit

The external oscillator circuit may drive an external crystal, ceramic resonator, capacitor, or RC network. A CMOS clock may also provide a clock input. For a crystal or ceramic resonator configuration, the crystal/resonator must be wired across the XTAL1 and XTAL2 pins as shown in Option 1 of Figure 19.1. A 10 MΩ resistor also must be wired across the XTAL2 and XTAL1 pins for the crystal/resonator configuration. In RC, capacitor, or CMOS clock configuration, the clock source should be wired to the XTAL2 pin as shown in Option 2, 3, or 4 of Figure 19.1. The type of external oscillator must be selected in the OSCXCN register, and the frequency control bits (XFCN) must be selected appropriately (see SFR Definition 19.6).

Important Note on External Oscillator Usage: Port pins must be configured when using the external oscillator circuit. When the external oscillator drive circuit is enabled in crystal/resonator mode, Port pins P0.2 and P0.3 are used as XTAL1 and XTAL2 respectively. When the external oscillator drive circuit is enabled in capacitor, RC, or CMOS clock mode, Port pin P0.3 is used as XTAL2. The Port I/O Crossbar should be configured to skip the Port pins used by the oscillator circuit; see Section “20.3. Priority Crossbar Decoder” on page 180 for Crossbar configuration. Additionally, when using the external oscillator circuit in crystal/resonator, capacitor, or RC mode, the associated Port pins should be configured as **analog inputs**. In CMOS clock mode, the associated pin should be configured as a **digital input**. See Section “20.4. Port I/O Initialization” on page 182 for details on Port input mode selection.

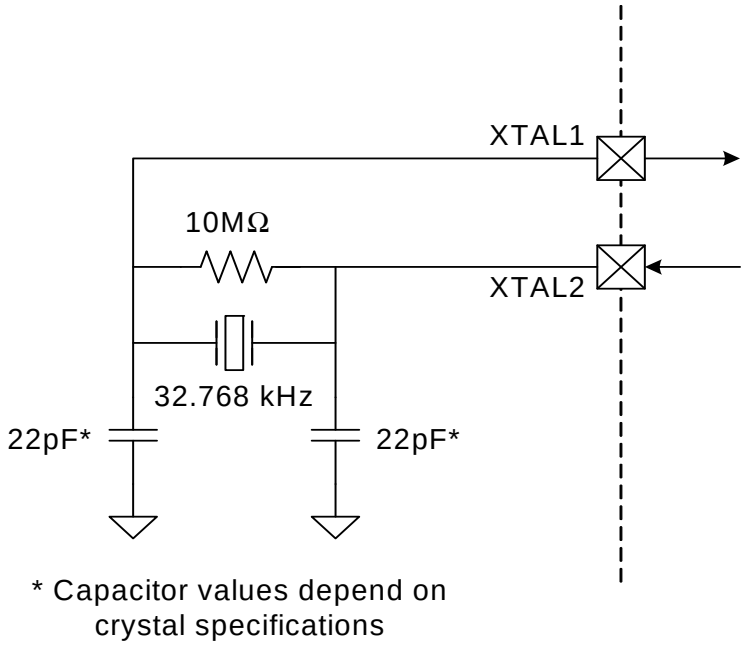

Figure 19.3. External 32.768 kHz Quartz Crystal Oscillator Connection Diagram

19.4.2. External RC Example

If an RC network is used as an external oscillator source for the MCU, the circuit should be configured as shown in Figure 19.1, Option 2. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, first select the RC network value to produce the desired frequency of oscillation, according to Equation , where f = the frequency of oscillation in MHz, C = the capacitor value in pF, and R = the pull-up resistor value in kΩ.

$$f = 1.23 \times 10^3 / (R \times C)$$

Equation 19.1. RC Mode Oscillator Frequency

For example: If the frequency desired is 100 kHz, let R = 246 kΩ and C = 50 pF:

f = 1.23(10^3)/RC = 1.23(10^3)/[246 x 50] = 0.1 MHz = 100 kHz

Referring to the table in SFR Definition 19.6, the required XFCN setting is 010b.

19.4.3. External Capacitor Example

If a capacitor is used as an external oscillator for the MCU, the circuit should be configured as shown in Figure 19.1, Option 3. The capacitor should be no greater than 100 pF; however for very small capacitors, the total capacitance may be dominated by parasitic capacitance in the PCB layout. To determine the required External Oscillator Frequency Control value (XFCN) in the OSCXCN Register, select the capacitor to be used and find the frequency of oscillation according to Equation 19.2, where f = the frequency of oscillation in MHz, C = the capacitor value in pF, and V_{DD} = the MCU power supply in Volts.

LIN Register Definition 21.9. LIN0DIV: LIN0 Divider Register

Bit	7	6	5	4	3	2	1	0
Name	DIVLSB[3:0]							
Type	R/W							
Reset	1	1	1	1	1	1	1	1

Indirect Address = 0x0C

Bit	Name	Function
7:0	DIVLSB	**LIN Baud Rate Divider Least Significant Bits.** The 8 least significant bits for the baud rate divider. The 9th and most significant bit is the DIV9 bit (LIN0MUL.0). The valid range for the divider is 200 to 511.

LIN Register Definition 21.10. LIN0MUL: LIN0 Multiplier Register

Bit	7	6	5	4	3	2	1	0
Name	PRESCL[1:0]		LINMUL[4:0]					DIV9
Type	R/W		R/W					R/W
Reset	1	1	1	1	1	1	1	1

Indirect Address = 0x0D

Bit	Name	Function
7:6	PRESCL[1:0]	**LIN Baud Rate Prescaler Bits.** These bits are the baud rate prescaler bits.
5:1	LINMUL[4:0]	**LIN Baud Rate Multiplier Bits.** These bits are the baud rate multiplier bits. These bits are not used in slave mode.
0	DIV9	**LIN Baud Rate Divider Most Significant Bit.** The most significant bit of the baud rate divider. The 8 least significant bits are in LIN0DIV. The valid range for the divider is 200 to 511.

22.2.4. CAN Register Assignment

The standard Bosch CAN registers are mapped to SFR space as shown below and their full definitions are available in the CAN User's Guide. The name shown in the Name column matches what is provided in the CAN User's Guide. One additional SFR which is not a standard Bosch CAN register, CAN0CFG, is provided to configure the CAN clock. All CAN registers are located on SFR Page 0x0C.

Table 22.2. Standard CAN Registers and Reset Values

CAN Addr.	Name	SFR Name (High)	SFR Addr.	SFR Name (Low)	SFR Addr.	16-bit SFR	Reset Value
0x00	CAN Control Register	—	—	CAN0CN	0xC0	—	0x01
0x02	Status Register	—	—	CAN0STAT	0x94	—	0x00
0x04	Error Counter[1]	CAN0ERRH	0x97	CAN0ERRL	0x96	CAN0ERR	0x0000
0x06	Bit Timing Register[2]	CAN0BTH	0x9B	CAN0BTL	0x9A	CAN0BT	0x2301
0x08	Interrupt Register[1]	CAN0IIDH	0x9D	CAN0IIDL	0x9C	CAN0IID	0x0000
0x0A	Test Register	—	—	CAN0TST	0x9E	—	0x00[3,4]
0x0C	BRP Extension Register[2]	—	—	CAN0BRPE	0xA1	—	0x00
0x10	IF1 Command Request	CAN0IF1CRH	0xBF	CAN0IF1CRL	0xBE	CAN0IF1CR	0x0001
0x12	IF1 Command Mask	CAN0IF1CMH	0xC3	CAN0IF1CML	0xC2	CAN0IF1CM	0x0000
0x14	IF1 Mask 1	CAN0IF1M1H	0xC5	CAN0IF1M1L	0xC4	CAN0IF1M1	0xFFFF
0x16	IF1 Mask 2	CAN0IF1M2H	0xC7	CAN0IF1M2L	0xC6	CAN0IF1M2	0xFFFF
0x18	IF1 Arbitration 1	CAN0IF1A1H	0xCB	CAN0IF1A1L	0xCA	CAN0IF1A1	0x0000
0x1A	IF1 Arbitration 2	CAN0IF1A2H	0xCD	CAN0IF1A2L	0xCC	CAN0IF1A2	0x0000
0x1C	IF1 Message Control	CAN0IF1MCH	0xD3	CAN0IF1MCL	0xD2	CAN0IF1MC	0x0000
0x1E	IF1 Data A 1	CAN0IF1DA1H	0xD5	CAN0IF1DA1L	0xD4	CAN0IF1DA1	0x0000
0x20	IF1 Data A 2	CAN0IF1DA2H	0xD7	CAN0IF1DA2L	0xD6	CAN0IF1DA2	0x0000
0x22	IF1 Data B 1	CAN0IF1DB1H	0xDB	CAN0IF1DB1L	0xDA	CAN0IF1DB1	0x0000
0x24	IF1 Data B 2	CAN0IF1DB2H	0xDD	CAN0IF1DB2L	0xDC	CAN0IF1DB2	0x0000
0x40	IF2 Command Request	CAN0IF2CRH	0xDF	CAN0IF2CRL	0xDE	CAN0IF2CR	0x0001
0x42	IF2 Command Mask	CAN0IF2CMH	0xE3	CAN0IF2CML	0xE2	CAN0IF2CM	0x0000
0x44	IF2 Mask 1	CAN0IF2M1H	0xEB	CAN0IF2M1L	0xEA	CAN0IF2M1	0xFFFF
0x46	IF2 Mask 2	CAN0IF2M2H	0xED	CAN0IF2M2L	0xEC	CAN0IF2M2	0xFFFF
0x48	IF2 Arbitration 1	CAN0IF2A1H	0xEF	CAN0IF2A1L	0xEE	CAN0IF2A1	0x0000
0x4A	IF2 Arbitration 2	CAN0IF2A2H	0xF3	CAN0IF2A2L	0xF2	CAN0IF2A2	0x0000
0x4C	IF2 Message Control	CAN0IF2MCH	0xCF	CAN0IF2MCL	0xCE	CAN0IF2MC	0x0000
0x4E	IF2 Data A 1	CAN0IF2DA1H	0xF7	CAN0IF2DA1L	0xF6	CAN0IF2DA1	0x0000

Notes:
1. Read-only register.
2. Write-enabled by CCE.
3. The reset value of CAN0TST could also be r0000000b, where r signifies the value of the CAN RX pin.
4. Write-enabled by Test.

23.5.3. Write Sequence (Slave)

During a write sequence, an SMBus master writes data to a slave device. The slave in this transfer will be a receiver during the address byte, and a receiver during all data bytes. When slave events are enabled (INH = 0), the interface enters Slave Receiver Mode when a START followed by a slave address and direction bit (WRITE in this case) is received. Upon entering Slave Receiver Mode, an interrupt is generated and the ACKRQ bit is set. The software must respond to the received slave address with an ACK, or ignore the received slave address with a NACK.

If the received slave address is ignored, slave interrupts will be inhibited until the next START is detected. If the received slave address is acknowledged, zero or more data bytes are received. Software must write the ACK bit at that time to ACK or NACK the received byte.

The interface exits Slave Receiver Mode after receiving a STOP. Note that the interface will switch to Slave Transmitter Mode if SMB0DAT is written while an active Slave Receiver. Figure 23.7 shows a typical slave write sequence. Two received data bytes are shown, though any number of bytes may be received. Notice that the 'data byte transferred' interrupts occur **before** the ACK in this mode.

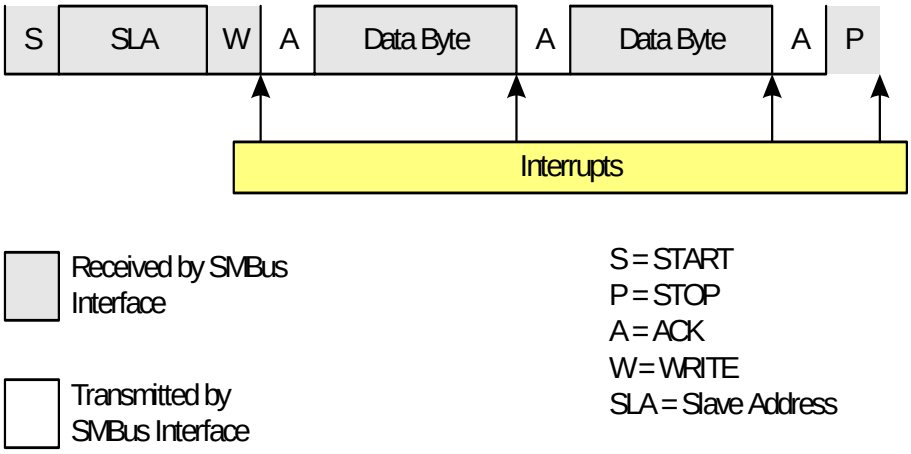

Figure 23.7. Typical Slave Write Sequence

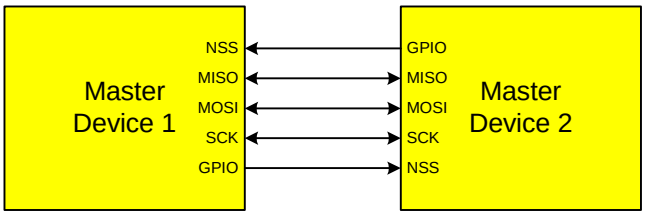

Figure 25.2. Multiple-Master Mode Connection Diagram

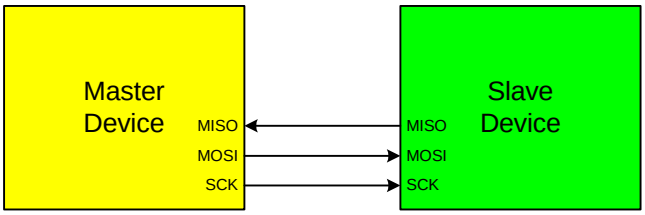

Figure 25.3. 3-Wire Single Master and 3-Wire Single Slave Mode Connection Diagram

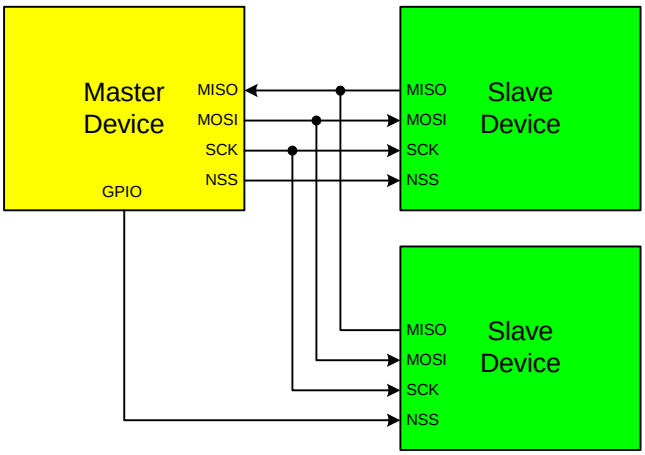

Figure 25.4. 4-Wire Single Master Mode and 4-Wire Slave Mode Connection Diagram

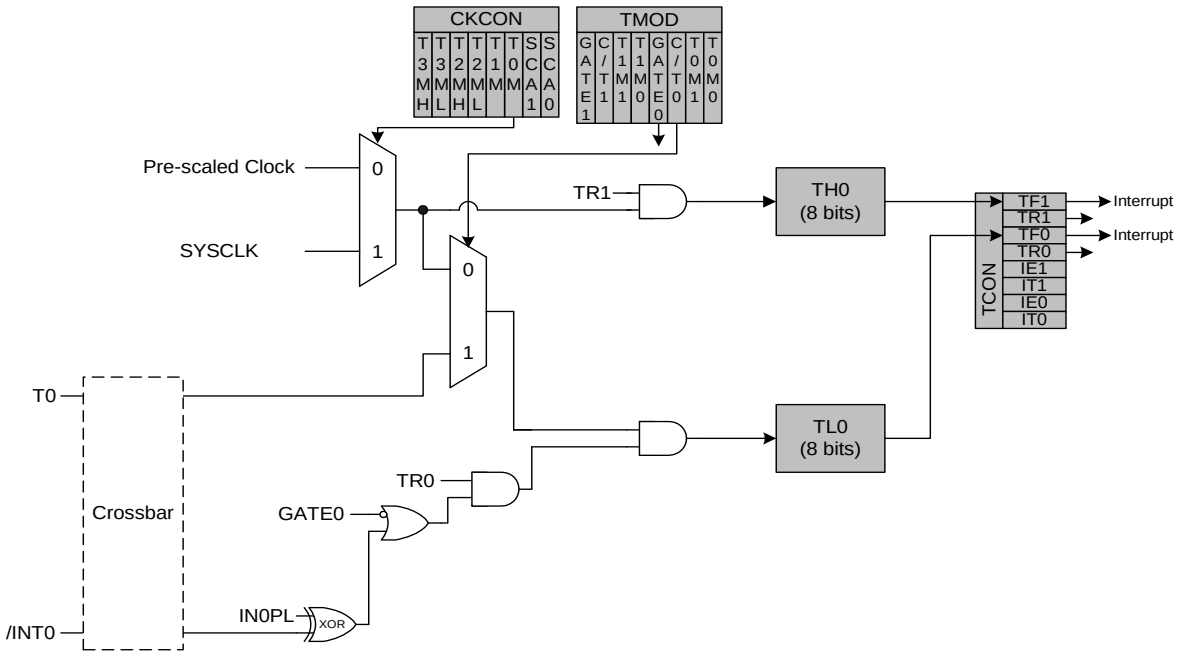

Figure 26.3. T0 Mode 3 Block Diagram

SFR Definition 26.13. TMR3CN: Timer 3 Control

Bit	7	6	5	4	3	2	1	0
Name	TF3H	TF3L	TF3LEN	TF3CEN	T3SPLIT	TR3		T3XCLK
Type	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W
Reset	0	0	0	0	0	0	0	0

SFR Address = 0x91; SFR Page = 0x00

Bit	Name	Function
7	TF3H	**Timer 3 High Byte Overflow Flag.** Set by hardware when the Timer 3 high byte overflows from 0xFF to 0x00. In 16 bit mode, this will occur when Timer 3 overflows from 0xFFFF to 0x0000. When the Timer 3 interrupt is enabled, setting this bit causes the CPU to vector to the Timer 3 interrupt service routine. This bit is not automatically cleared by hardware.
6	TF3L	**Timer 3 Low Byte Overflow Flag.** Set by hardware when the Timer 3 low byte overflows from 0xFF to 0x00. TF3L will be set when the low byte overflows regardless of the Timer 3 mode. This bit is not automatically cleared by hardware.
5	TF3LEN	**Timer 3 Low Byte Interrupt Enable.** When set to 1, this bit enables Timer 3 Low Byte interrupts. If Timer 3 interrupts are also enabled, an interrupt will be generated when the low byte of Timer 3 overflows.
4	TF3CEN	**Timer 3 Capture Mode Enable.** 0: Timer 3 Capture Mode is disabled. 1: Timer 3 Capture Mode is enabled.
3	T3SPLIT	**Timer 3 Split Mode Enable.** When this bit is set, Timer 3 operates as two 8-bit timers with auto-reload. 0: Timer 3 operates in 16-bit auto-reload mode. 1: Timer 3 operates as two 8-bit auto-reload timers.
2	TR3	**Timer 3 Run Control.** Timer 3 is enabled by setting this bit to 1. In 8-bit mode, this bit enables/disables TMR3H only; TMR3L is always enabled in split mode.
1	Unused	Read = 0b; Write = Don't Care
0	T3XCLK	**Timer 3 External Clock Select.** This bit selects the external clock source for Timer 3. If Timer 3 is in 8-bit mode, this bit selects the external oscillator clock source for both timer bytes. However, the Timer 3 Clock Select bits (T3MH and T3ML in register CKCON) may still be used to select between the external clock and the system clock for either timer. 0: Timer 3 clock is the system clock divided by 12. 1: Timer 3 clock is the external clock divided by 8 (synchronized with SYSCLK).