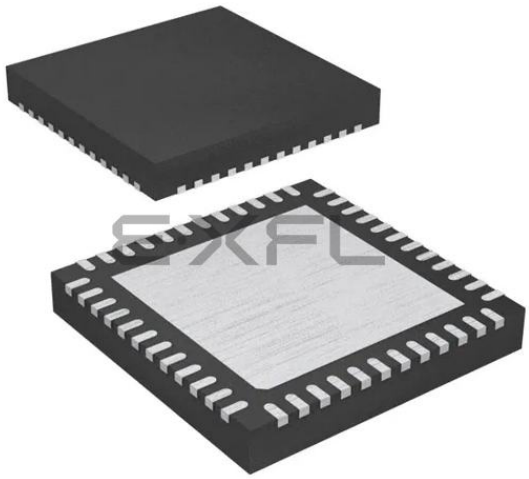

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	Ethernet, I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	38
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN-EP (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51cn128cgt

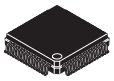
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MCF51CN128
Rev. 4, 5/2009

MCF51CN128

MCF51CN128 ColdFire Microcontroller Cover: MCF51CN128


80 LQFP
14 mm × 14 mm


64 LQFP
10 mm × 10 mm


48 QFN
7 mm × 7 mm

The MCF51CN128 device is a low-cost, low-power, high-performance 32-bit ColdFire V1 microcontroller (MCU) featuring 10/100 BASE-T/TX fast ethernet controller (FEC), media independent interface (MII) to connect an external physical transceiver (PHY), and multi-function external bus interface.

MCF51CN128 also has multiple communication interfaces for various ethernet gateway applications. MCF51CN128 is the first ColdFire V1 device to incorporate ethernet and external bus interface along with new features to minimize power consumption and increase functionality in low-power modes.

The MCF51CN128 features the following functional units:

- 32-bit ColdFire V1 Central Processing Unit (CPU)
  - Up to 50.33 MHz ColdFire CPU from 3.6 V to 3.0 V, up to 40 MHz CPU from 3.0 V to 2.1 V, and up to 20 MHz CPU from 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
  - Provides 0.94 Dhrystone 2.1 MIPS per MHz performance when running from internal RAM (0.76 DMIPS/MHz from flash)
  - ColdFire Instruction Set Revision C (ISA_C)
  - Support for up to 45 peripheral interrupt requests and 7 software interrupts
- On-Chip Memory
  - 128 KB Flash, 24 KB RAM
  - Flash read/program/erase over full operating voltage and temperature
  - On-chip memory aliased to create a contiguous memory space with off-chip memory
  - Security circuitry to prevent unauthorized access to Peripherals, RAM, and flash contents
- Ethernet
  - FEC—10/100 BASE-T/TX, bus-mastering fast ethernet controller with direct memory access (DMA); supports half or full duplex; operation is limited to 3.0 V to 3.6 V
  - MII—media independent interface to connect ethernet controller to external PHY; includes output clock for external PHY
- External Bus
  - Mini-FlexBus—Multi-function external bus interface; supports up to 1 MB memories, gate-array logic, simple slave device or glueless interfaces to standard chip-selected asynchronous memories
  - Programmable options: access time per chip select, burst and burst-inhibited transfers per chip select, transfer direction, and address setup and hold times
- Power-Saving Modes
  - Two low-power stop modes, one of which allows limited use of some peripherals (ADC, KBI, RTC)
  - Reduced-power wait mode shuts off CPU and allows full use of all peripherals; FEC can remain active and conduct DMA transfers to RAM and assert an interrupt to wake up the CPU upon completion
  - Low-power run and wait modes allow peripherals to run while the voltage regulator is in standby
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low-power external oscillator that can be used in stop3 mode to provide accurate clock source to active peripherals
  - Low-power real-time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6 µs typical wake-up time from stop3 mode
  - Pins and clocks to peripherals not available in smaller packages are automatically disabled for reduced current consumption; no user interaction is needed
- Clock Source Options
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 25 MHz
  - Multi-Purpose Clock Generator (MCG) — Flexible clock source module with either frequency-locked-loop (FLL) or phase-lock loop (PLL) clock options. FLL can be controlled by internal or external reference and

2 Pin Assignments

This section describes the pin assignments for the available packages. See for pin availability by package pin-count.

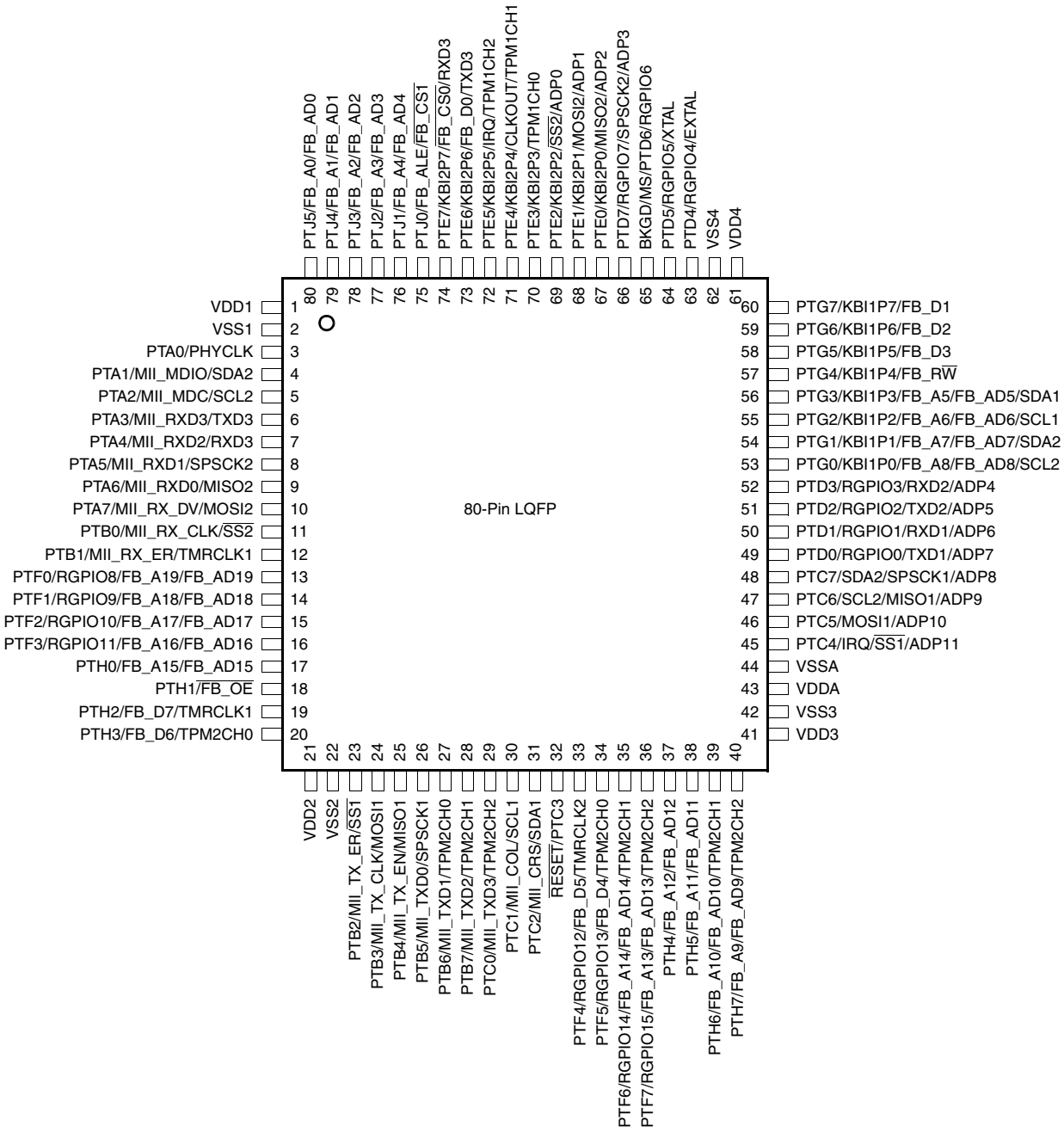


Figure 2. Pin Assignments in 80-Pin LQFP Package

Table 2. Package Pin Assignments (continued)

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
4	4	4	PTA1	MII_MDIO	—	SDA2	—
5	5	5	PTA2	MII_MDC	—	SCL2	—
6	6	6	PTA3	MII_RXD3	TXD3	—	—
7	7	7	PTA4	MII_RXD2	RXD3	—	—
8	8	8	PTA5	MII_RXD1	SPSCK2	—	—
9	9	9	PTA6	MII_RXD0	MISO2	—	—
10	10	10	PTA7	MII_RX_DV	MOSI2	—	—
11	11	11	PTB0	MII_RX_CLK	$\overline{SS2}$	—	—
12	12	12	PTB1	MII_RX_ER	—	TMRCLK1	—
13	13	—	PTF0/RGPIO8	—	FB_A19/FB_AD19	—	RGPIO_ENB selects between standard GPIO and RGPIO
14	14	—	PTF1/RGPIO9	—	FB_A18/FB_AD18	—	
15	15	—	PTF2/RGPIO10	—	FB_A17/FB_AD17	—	
16	16	—	PTF3/RGPIO11	—	FB_A16/FB_AD16	—	
17	—	—	PTH0	—	FB_A15/FB_AD15	—	—
18	—	—	PTH1	—	$\overline{FB\_OE}$	—	—
19	—	—	PTH2	—	FB_D7	TMRCLK1	—
20	—	—	PTH3	—	FB_D6	TPM2CH0	—
21	17	13	VDD2	—	—	—	—
22	18	14	VSS2	—	—	—	—
23	19	15	PTB2	MII_TX_ER	$\overline{SS1}$	—	—
24	20	16	PTB3	MII_TX_CLK	MOSI1	—	—
25	21	17	PTB4	MII_TX_EN	MISO1	—	—
26	22	18	PTB5	MII_TXD0	SPSCK1	—	—
27	23	19	PTB6	MII_TXD1	—	TPM2CH0	—
28	24	20	PTB7	MII_TXD2	—	TPM2CH1	—
29	25	21	PTC0	MII_TXD3	—	TPM2CH2	—
30	26	22	PTC1	MII_COL	—	SCL1	—
31	27	23	PTC2	MII_CRS	—	SDA1	—

3.2 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 3. Parameter Classifications

P	These parameters are guaranteed during production testing on each individual device.
C	These parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	These parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	These parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

3.3 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 4 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}) or the programmable pull-up resistor associated with the pin is enabled.

Table 4. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to +3.8	V
Maximum current into V_{DD}	I_{DD}	120	mA
Digital input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	± 25	mA
Storage temperature range	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low (which would reduce overall power consumption).

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H (–40 to 85 or 0 to 70)[1]	°C
Maximum junction temperature		T_{JM}	95	°C
Thermal resistance Single-layer board				
	48-pin QFN	θ_{JA}	81	°C/W
	64-pin LQFP		69	
	80-pin LQFP		60	
Thermal resistance Four-layer board				
	48-pin QFN	θ_{JA}	26	°C/W
	64-pin LQFP		50	
	80-pin LQFP		47	

1 Depending on device.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
17	P	Low-voltage detection threshold — low range[8]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.70 1.80	1.83 1.89	1.95 2.00	V
18	P	Low-voltage warning threshold — high range[8]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.50 2.50	2.62 2.62	2.70 2.70	V
19	P	Low-voltage warning threshold — low range[8]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.25 2.29	2.32 2.39	2.45 2.49	V
20	P	Bandgap Voltage Reference[10]	V_{BG}	—	1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 As an exception, the Fast Ethernet Controller (FEC) is only operational above the operating voltage of 3 V.

3 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 Maximum is highest voltage that POR is guaranteed.

8 Low voltage detection and warning limits measured at 1 MHz bus frequency.

9 Run at 1 MHz bus frequency

10 Factory trimmed at V_{DD} = 3.3 V, Temp = 25 °C

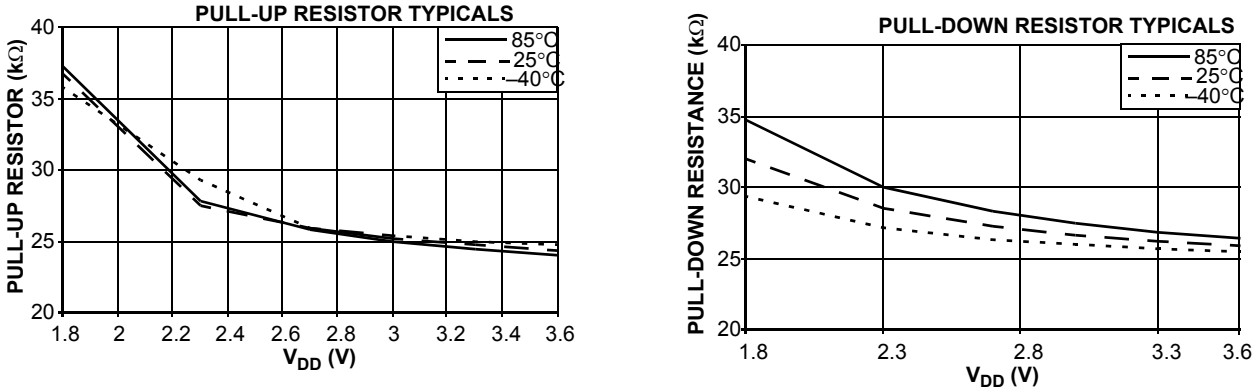


Figure 5. Pull-up and Pull-down Typical Resistor Values

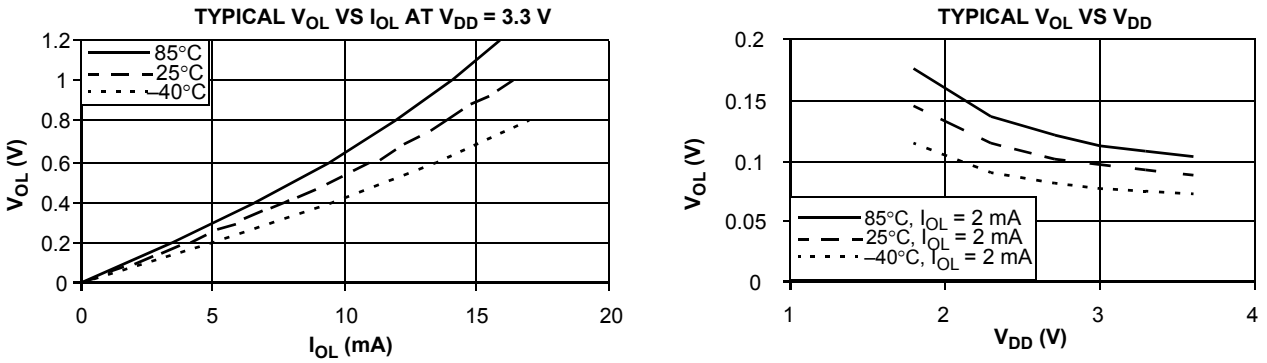


Figure 6. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

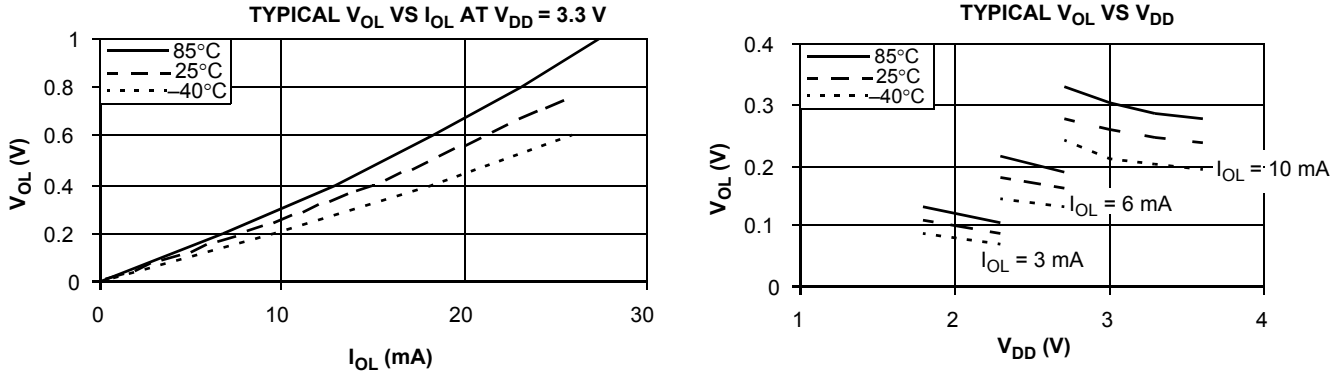


Figure 7. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

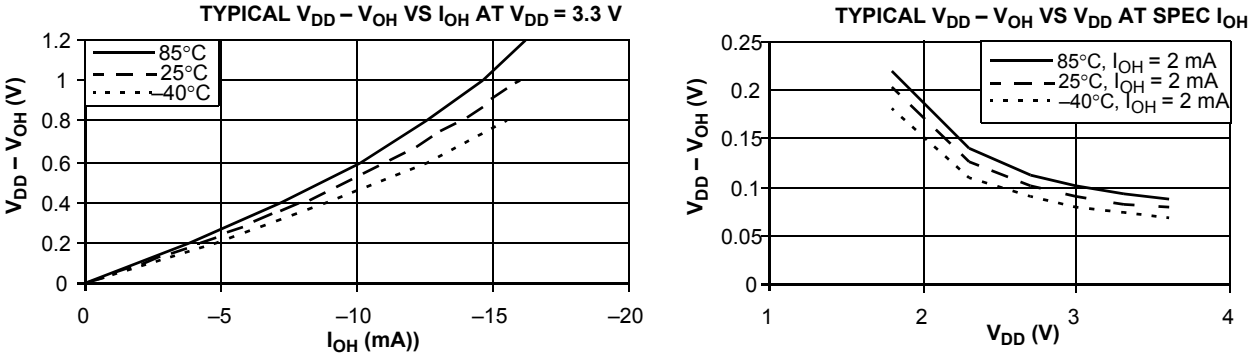


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

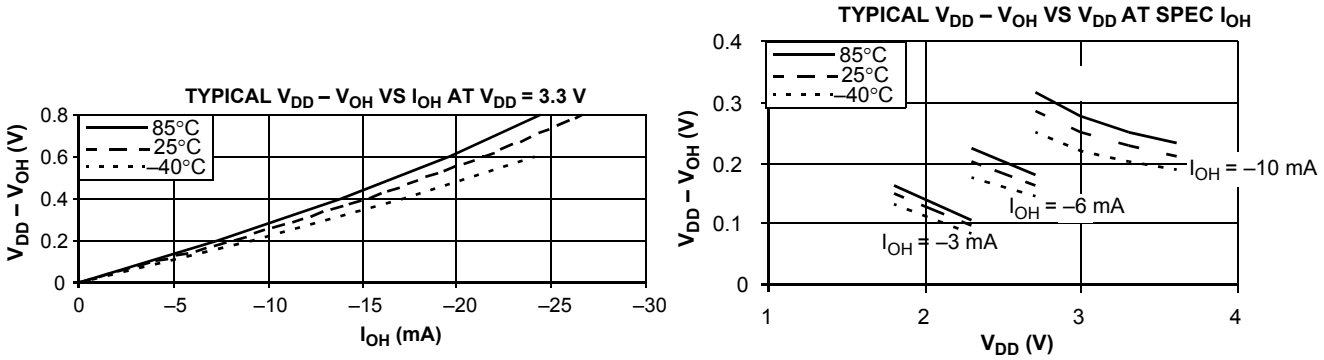


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25 MHz	3.3	60	75	mA	–40 to 85 °C
	T			20 MHz		49	—		
	T			8 MHz		21	—		
	T			1 MHz		4.6	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25 MHz	3.3	44	47	mA	–40 to 85 °C
	T			20 MHz		36	—		
	T			8 MHz		15.5	—		
	T			1 MHz		3.9	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3.3	203	—	µA	–40 to 85 °C
	T			16 kHz FBELP		154	—		
4	T	Run supply current LPRS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3.3	50	—	µA	–40 to 85 °C
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25 MHz	3.3	11	13.7	µA	–-40 to 85 °C
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3.3	0.35	11	µA	0 to 70 °C
	P						45		–40 to 85 °C
	C				1.8	0.35	12		0 to 70 °C
	C						16.2		–40 to 85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
7	C	Stop3 mode supply current No clocks active		$S3I_{DD}$	n/a	3.3	0.52	14	µA	0 to 70 °C
	P							55		–40 to 85 °C
	C					1.8	0.52	15		0 to 70 °C
	C							32.4		–40 to 85 °C
8	T	Low power mode adders:	EREFSTEN=1	—	32 kHz	3.3	500	—	nA	–40 to 85 °C
9	T		IREFSTEN=1		32 kHz		70	—	µA	–40 to 85 °C
10	T		TPM PWM		100 Hz		12	—	µA	–40 to 85 °C
11	T		SCI, SPI, or IIC		300 bps		15	—	µA	–40 to 85 °C
12	T		RTC using LPO		1 kHz		200	—	nA	–40 to 85 °C
13	T		RTC using ICSERCLK		32 kHz		1	—	µA	–40 to 85 °C
14	T		LVD		n/a		100	—	µA	–40 to 85 °C

[1] Data in Typical column was characterized at 3.3 V, 25 °C or is typical recommended value.

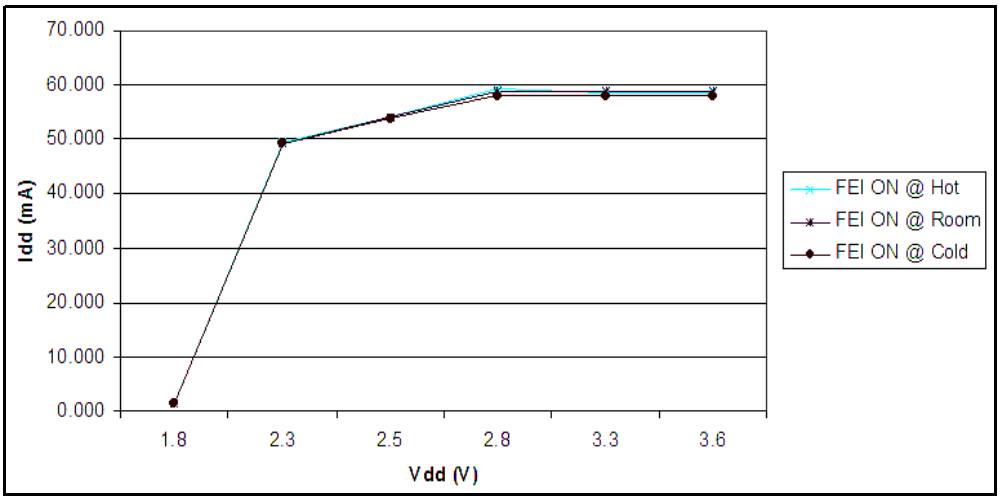


Figure 10. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ADC off, All Other Modules Enabled)

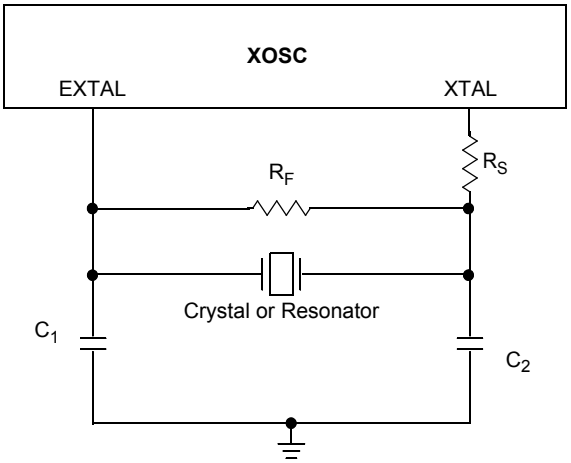


Figure 11. Typical Crystal or Resonator Circuit: High Range and Low Range/High Gain

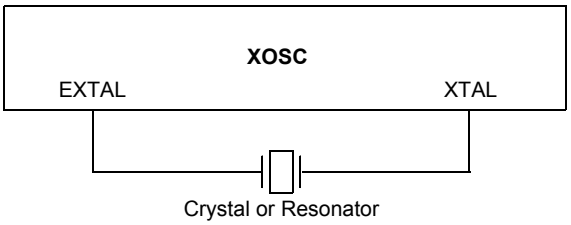


Figure 12. Typical Crystal or Resonator Circuit: Low Range/Low Gain

3.9 Multipurpose Clock Generator (MCG) Specifications

Table 11. MCG Frequency Specifications (Temperature Range = –40 to 125 °C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	P	Internal reference frequency - factory trimmed at V_{DD} = and temperature = 25 °C	f_{int_ft}	—	32.768	—	kHz
2	P	Average internal reference frequency - untrimmed [1]	f_{int_ut}	25	—	41.66	kHz
3	P	Average internal reference frequency - user trimmed	f_{int_t}	31.25	—	39.06	kHz
4	D	Internal reference startup time	t_{irefst}	—	60	100	us
5	—	DCO output frequency range - untrimmed [1] value provided for reference: f_{dco_ut} = 1024 X f_{int_ut}	f_{dco_ut}	25.6	33.48	42.66	MHz
6	P	DCO output frequency range - trimmed	f_{dco_t}	32	—	40	MHz
7	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.1	± 0.2	$\%f_{dco}$

Table 11. MCG Frequency Specifications (continued)(Temperature Range = –40 to 125 °C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
9	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
11	C	FLL acquisition time [2]	$t_{fll\_acquire}$	—	—	1	ms
12	D	PLL acquisition time [3]	$t_{pll\_acquire}$	—	—	1	ms
13	C	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
14	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
15	D	Lock entry frequency tolerance[5]	D_{lock}	± 1.49	—	± 2.98	%
16	D	Lock exit frequency tolerance[6]	D_{unl}	± 4.47	—	± 5.97	%
17	D	Lock time - FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time - PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency - RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG does not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG does not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

3.10 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 12. Mini-FlexBus AC Timing Specifications

Num	C	Characteristic	Min	Max	Unit	Notes
—	—	Frequency of Operation	—	25.1666	MHz	—
MB1	D	Clock Period	39.73	—	ns	—
MB2	P	Output Valid	—	20	ns	1
MB3	D	Output Hold	1.0	—	ns	1
MB4	P	Input Setup	22	—	ns	2
MB5	D	Input Hold	10	—	ns	2

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

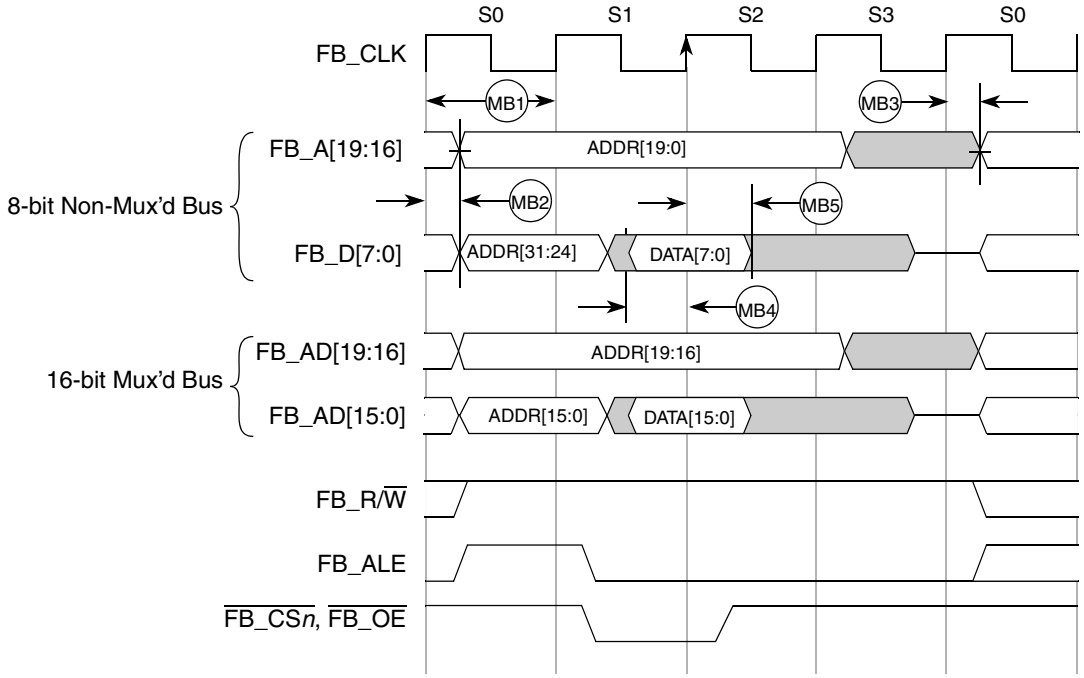


Figure 13. Mini-FlexBus Read Timing

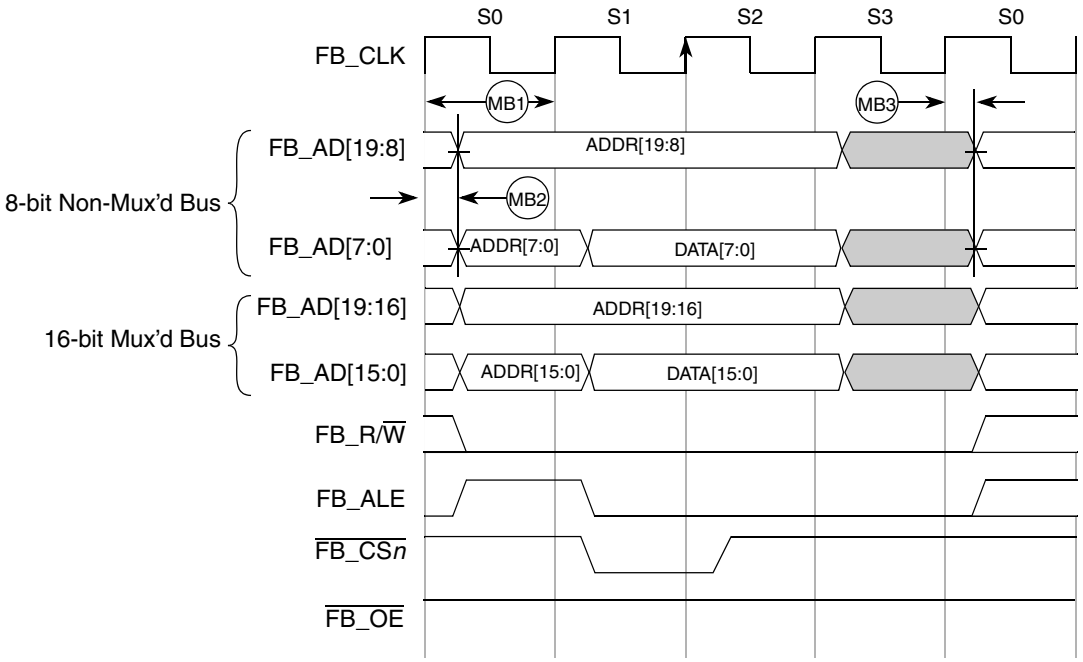


Figure 14. Mini-FlexBus Write Timing

3.11 Fast Ethernet Timing Specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 13. Receive Signal Timing

Num	C	Characteristic	MII Mode		Unit
			Min	Max	
—	—	RXCLK frequency	—	25	MHz
E1	P	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
E2	D	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
E3	D	RXCLK pulse width high	35%	65%	RXCLK period
E4	D	RXCLK pulse width low	35%	65%	RXCLK period

Table 17. Control Timing (continued)

Num	C	Rating	Symbol	Min	Typ[1]	Max	Unit
6	D	BKGD/MS hold time after issuing background debug force reset to enter user or BDM modes [3]	t_{MSH}	100	—	—	µs
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 2 x t_{cyc}	— —	— —	ns
8	D	Keyboard interrupt pulse width Asynchronous path[2] Synchronous path[4]	t_{ILIH}, t_{IHIL}	100 2 x t_{cyc}	— —	— —	ns
9	C	Port rise and fall time — Low output drive (PTxDS = 0) (load = 50 pF)[5] Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	16 23	— —	ns
		Port rise and fall time — High output drive (PTxDS = 1) (load = 50 pF) Slew rate control disabled (PTxSE = 0) Slew rate control enabled (PTxSE = 1)	t_{Rise}, t_{Fall}	— —	5 9	— —	ns
10	C	Stop3 recovery time, from interrupt event to vector fetch	t_{STPREC}	—	6	10	µs

1 Typical values are based on characterization data at V_{DD} = 3.3 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a reset or interrupt pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 To enter BDM mode following a POR, BKGD/MS should be held low during the power-up and for a hold time of t_{MSH} after V_{DD} rises above V_{LVD}.

4 This is the minimum assertion time in which the interrupt may be recognized. The correct protocol is to assert the interrupt request until it is explicitly negated by the interrupt service routine.

5 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40 °C to 85 °C.

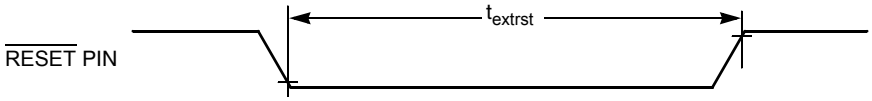


Figure 19. Reset Timing

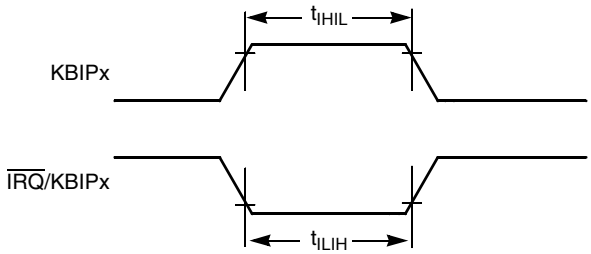


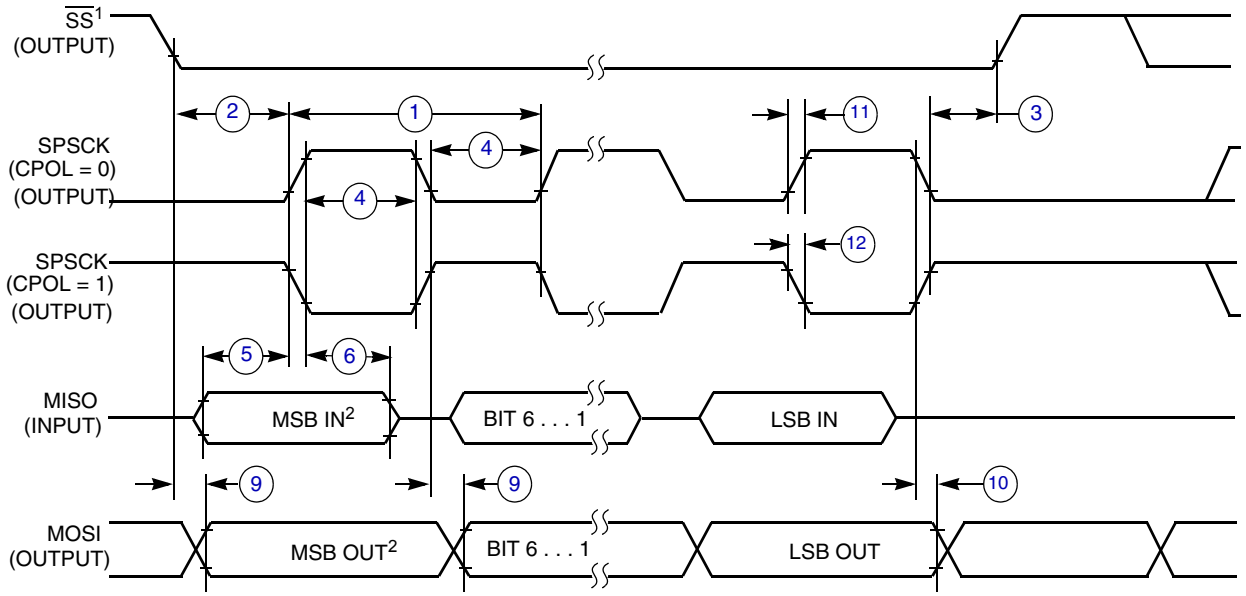
Figure 20. IRQ/KBIPx Timing

3.12.3 SPI Timing

Table 19 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

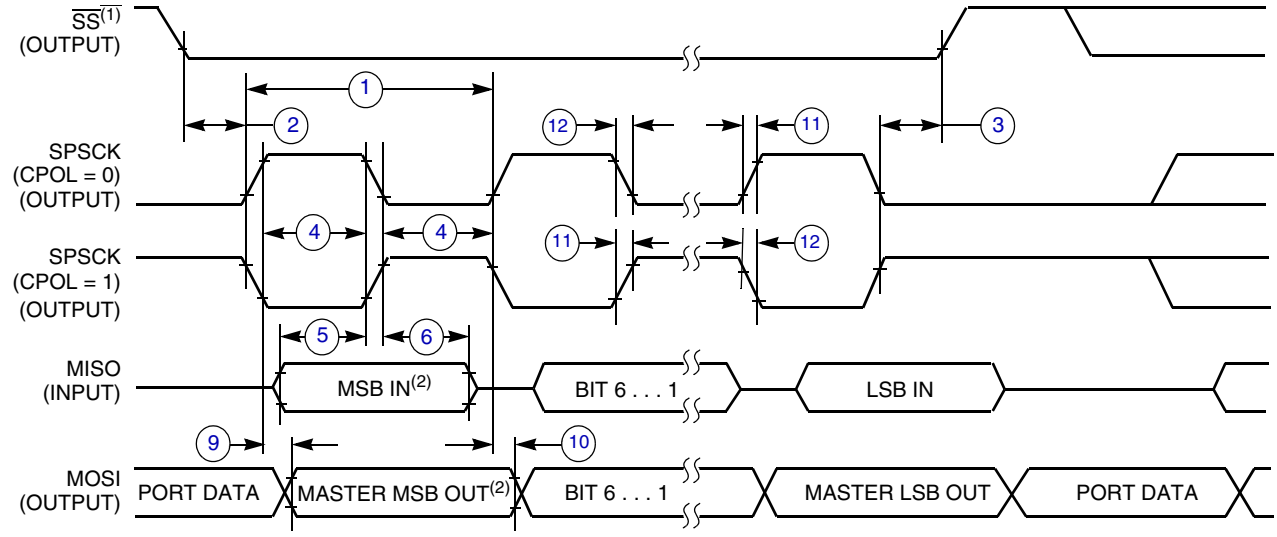
Table 19. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 23. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. SPI Master Timing (CPHA =1)

3.12.4 ADC Characteristics

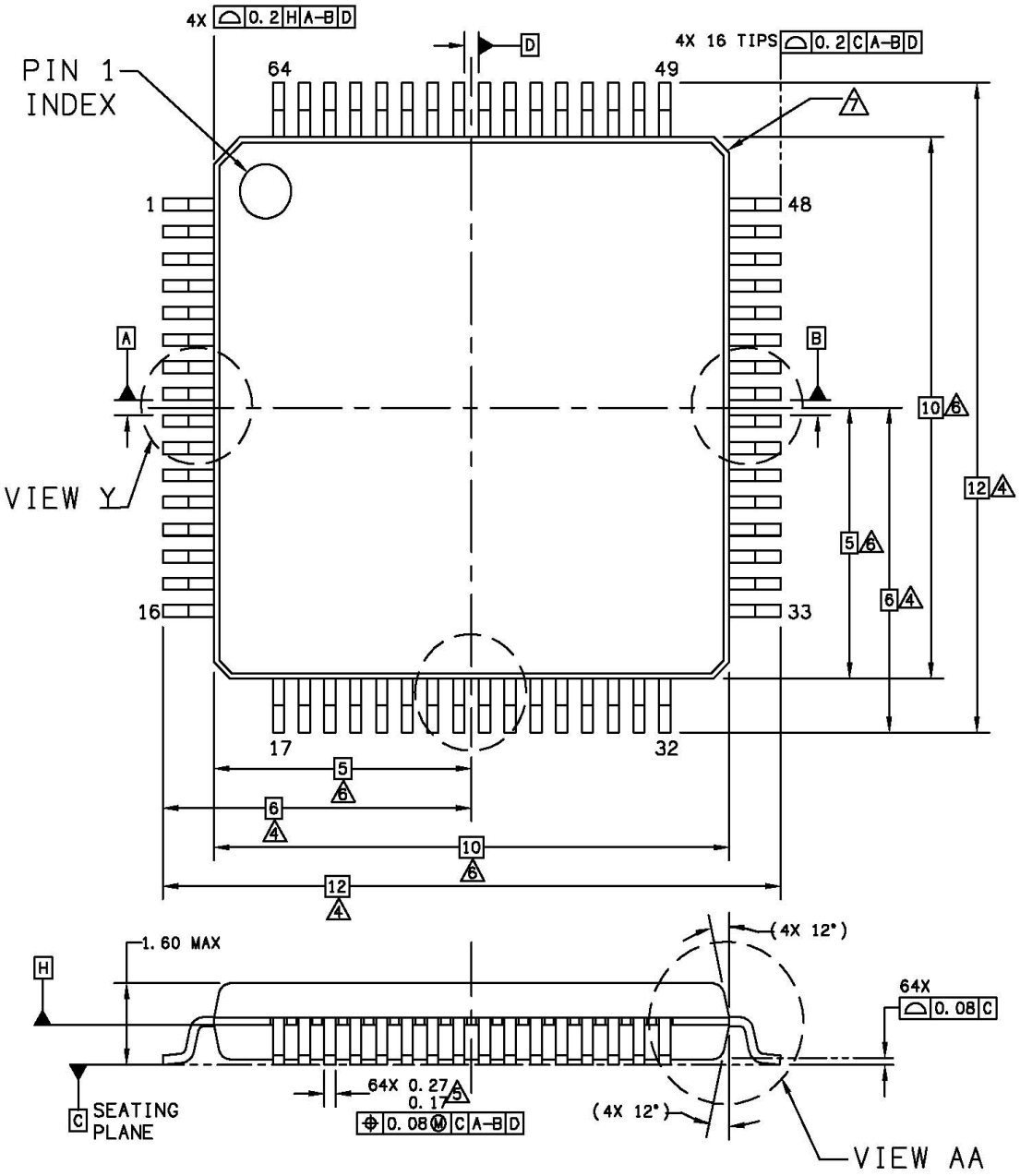
Table 20. 12-bit ADC Operating Conditions

C	Characteristic	Conditions	Symb	Min	Typ[1]	Max	Unit	Comment
D	Supply voltage	Absolute	V_{DDAD}	1.8	—	3.6	V	
		Delta to V_{DD} (V_{DD}-V_{DDAD})[2]	ΔV_{DDAD}	-100	0	+100	mV	
D	Ground voltage	Delta to V_{SS} (V_{SS}-V_{SSAD})[2]	ΔV_{SSAD}	-100	0	+100	mV	
D	Ref Voltage High		V_{REFH}	1.8	V_{DDAD}	V_{DDAD}	V	
D	Ref Voltage Low		V_{REFL}	V_{SSAD}	V_{SSAD}	V_{SSAD}	V	
D	Input Voltage		V_{ADIN}	V_{REFL}	—	V_{REFH}	V	
C	Input Capacitance		C_{ADIN}	—	4.5	5.5	pF	
C	Input Resistance		R_{ADIN}	—	5	7	kΩ	
C	Analog Source Resistance	12 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
		10 bit mode f_{ADCK} > 4MHz f_{ADCK} < 4MHz		 — —	 — —	 5 10		
		8 bit mode (all valid f_{ADCK})		—	—	10		
D	ADC Conversion Clock Freq.	High Speed (ADLPC=0)	f_{ADCK}	0.4	—	8.0	MHz	
		Low Power (ADLPC=1)		0.4	—	4.0		

1 Typical values assume V_{DDAD} = 3.3 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

6.2 64-pin LQFP



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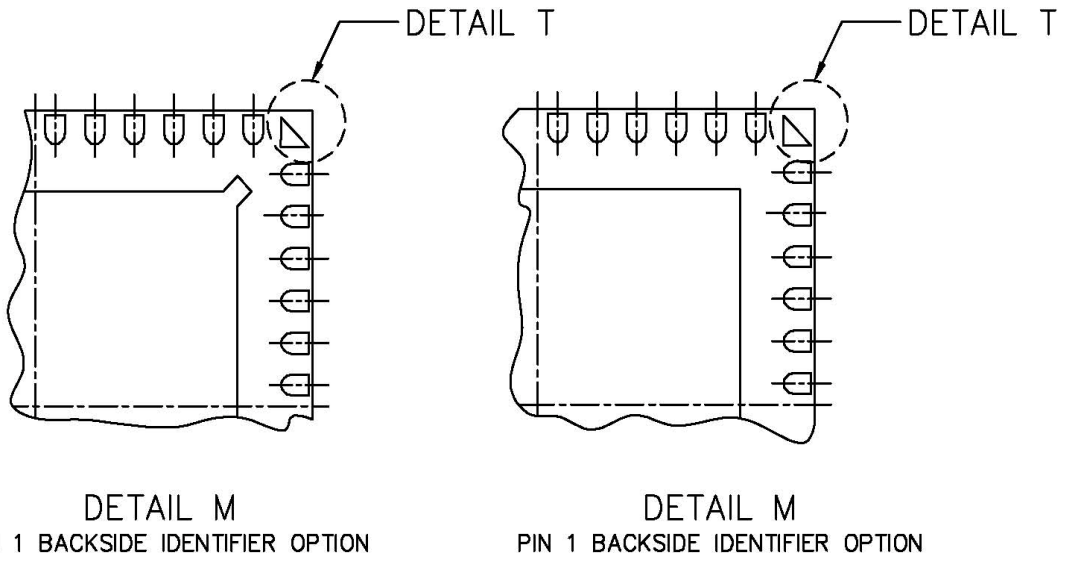
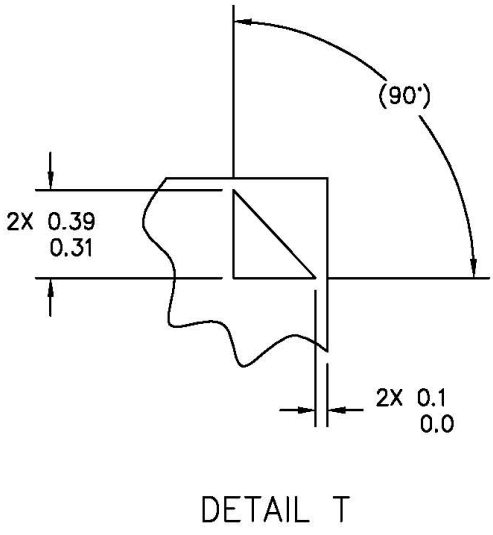
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	





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TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
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