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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	Ethernet, I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	54
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51cn128clh

Part Number	Package Description	Original (gold wire) package document number	Current (copper wire) package document number
MC68HC908JW32	48 QFN	98ARH99048A	98ASA00466D
MC9S08AC16			
MC9S908AC60			
MC9S08AC128			
MC9S08AW60			
MC9S08GB60A			
MC9S08GT16A			
MC9S08JM16			
MC9S08JM60			
MC9S08LL16			
MC9S08QE128			
MC9S08QE32			
MC9S08RG60			
MCF51CN128			
MC9RS08LA8	48 QFN	98ARL10606D	98ASA00466D
MC9S08GT16A	32 QFN	98ARH99035A	98ASA00473D
MC9S908QE32	32 QFN	98ARE10566D	98ASA00473D
MC9S908QE8	32 QFN	98ASA00071D	98ASA00736D
MC9S08JS16	24 QFN	98ARL10608D	98ASA00734D
MC9S08QB8			
MC9S08QG8	24 QFN	98ARL10605D	98ASA00474D
MC9S08SH8	24 QFN	98ARE10714D	98ASA00474D
MC9RS08KB12	24 QFN	98ASA00087D	98ASA00602D
MC9S08QG8	16 QFN	98ARE10614D	98ASA00671D
MC9RS08KB12	8 DFN	98ARL10557D	98ASA00672D
MC9S08QG8			
MC9RS08KA2	6 DFN	98ARL10602D	98ASA00735D

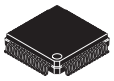
Freescale Semiconductor
Data Sheet: Technical Data

Document Number: MCF51CN128
Rev. 4, 5/2009

MCF51CN128

MCF51CN128 ColdFire Microcontroller Cover: MCF51CN128


80 LQFP
14 mm × 14 mm


64 LQFP
10 mm × 10 mm


48 QFN
7 mm × 7 mm

The MCF51CN128 device is a low-cost, low-power, high-performance 32-bit ColdFire V1 microcontroller (MCU) featuring 10/100 BASE-T/TX fast ethernet controller (FEC), media independent interface (MII) to connect an external physical transceiver (PHY), and multi-function external bus interface.

MCF51CN128 also has multiple communication interfaces for various ethernet gateway applications. MCF51CN128 is the first ColdFire V1 device to incorporate ethernet and external bus interface along with new features to minimize power consumption and increase functionality in low-power modes.

The MCF51CN128 features the following functional units:

- 32-bit ColdFire V1 Central Processing Unit (CPU)
  - Up to 50.33 MHz ColdFire CPU from 3.6 V to 3.0 V, up to 40 MHz CPU from 3.0 V to 2.1 V, and up to 20 MHz CPU from 2.1 V to 1.8 V across temperature range of –40 °C to 85 °C
  - Provides 0.94 Dhrystone 2.1 MIPS per MHz performance when running from internal RAM (0.76 DMIPS/MHz from flash)
  - ColdFire Instruction Set Revision C (ISA_C)
  - Support for up to 45 peripheral interrupt requests and 7 software interrupts
- On-Chip Memory
  - 128 KB Flash, 24 KB RAM
  - Flash read/program/erase over full operating voltage and temperature
  - On-chip memory aliased to create a contiguous memory space with off-chip memory
  - Security circuitry to prevent unauthorized access to Peripherals, RAM, and flash contents
- Ethernet
  - FEC—10/100 BASE-T/TX, bus-mastering fast ethernet controller with direct memory access (DMA); supports half or full duplex; operation is limited to 3.0 V to 3.6 V
  - MII—media independent interface to connect ethernet controller to external PHY; includes output clock for external PHY
- External Bus
  - Mini-FlexBus—Multi-function external bus interface; supports up to 1 MB memories, gate-array logic, simple slave device or glueless interfaces to standard chip-selected asynchronous memories
  - Programmable options: access time per chip select, burst and burst-inhibited transfers per chip select, transfer direction, and address setup and hold times
- Power-Saving Modes
  - Two low-power stop modes, one of which allows limited use of some peripherals (ADC, KBI, RTC)
  - Reduced-power wait mode shuts off CPU and allows full use of all peripherals; FEC can remain active and conduct DMA transfers to RAM and assert an interrupt to wake up the CPU upon completion
  - Low-power run and wait modes allow peripherals to run while the voltage regulator is in standby
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Low-power external oscillator that can be used in stop3 mode to provide accurate clock source to active peripherals
  - Low-power real-time counter for use in run, wait, and stop modes with internal and external clock sources
  - 6 µs typical wake-up time from stop3 mode
  - Pins and clocks to peripherals not available in smaller packages are automatically disabled for reduced current consumption; no user interaction is needed
- Clock Source Options
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 25 MHz
  - Multi-Purpose Clock Generator (MCG) — Flexible clock source module with either frequency-locked-loop (FLL) or phase-lock loop (PLL) clock options. FLL can be controlled by internal or external reference and

includes precision trimming of internal reference, allowing 0.2% resolution and 2% deviation over temperature and voltage. PLL derives a higher accuracy clock source derived by an external reference

- System Protection
  - Watchdog computer operating properly (COP) reset with option to run from dedicated 1-kHz internal clock source or bus clock
  - Low-voltage detection with reset or interrupt; selectable trip points
  - Illegal opcode and illegal address detection with programmable reset or exception response
  - Flash block protection
- Development Support
  - Single-wire background debug module (BDM) interface; supports same electrical interface used by the S08, 9S12, and 9S12x families debug modules
  - 4 PC plus 2 address (optional data) breakpoint registers with programmable 1- or 2-level trigger response
  - 64-entry processor status and debug data trace buffer with programmable start/stop conditions
- Peripherals
  - ADC—Up to 12 channel, 12-bit resolution; 2.5 µs conversion time; automatic compare function; 1.7 mV/°C temperature sensor; internal bandgap reference channel; operation in stop3; fully functional from 3.6 V to 1.8 V
  - SCI—Three modules with optional 13-bit break
  - SPI—Two interfaces with full-duplex or single-wire bi-directional; double-buffered transmit and receive; master or slave mode; MSB-first or LSB-first shifting
  - IIC—Two IICs with up to 100 kbps with maxmimum bus loading; multi-master operation; programmable slave address; interrupt-driven byte-by-byte data transfer; supports broadcast mode and 11-bit addressing
  - TPM—Two 3-channel, 16-bit resolution modules; selectable input capture, output compare, or buffered edge- or center-aligned PWM on each channel
  - RTC—8-bit modulus counter with binary- or decimal-based prescaler; external clock source for precise time base, time-of-day, calendar- or task-scheduling functions; free-running on-chip low-power oscillator (1 kHz) for cyclic wake-up without external components; runs in all MCU modes
  - MTIM—Two 8-bit resolution modulo timers with 8-bit prescaler
- Input/Output
  - Up to 70 general-purpose input/output (GPIO) pins, all with pin mux controls to select alternate functions
  - 16 keyboard interrupt (KBI) pins with selectable polarity
  - Hysteresis and configurable pull-up device or input filtering on all input pins; configurable slew rate and drive strength on all output pins
  - 16 Rapid GPIO pins connected to the CPU's high-speed local bus with set, clear, and toggle functionality (PTD and PTF)

2 Pin Assignments

This section describes the pin assignments for the available packages. See for pin availability by package pin-count.

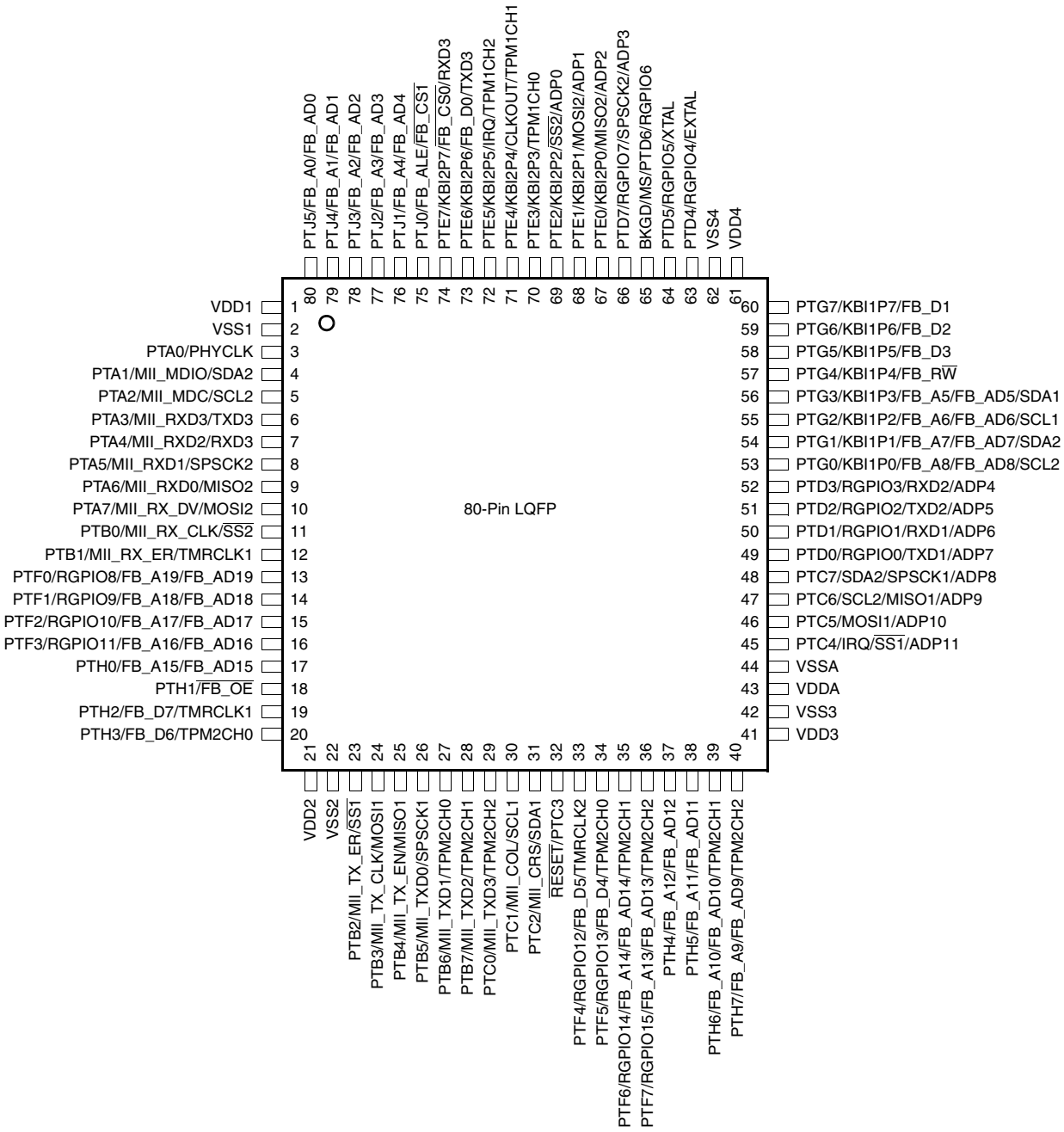


Figure 2. Pin Assignments in 80-Pin LQFP Package

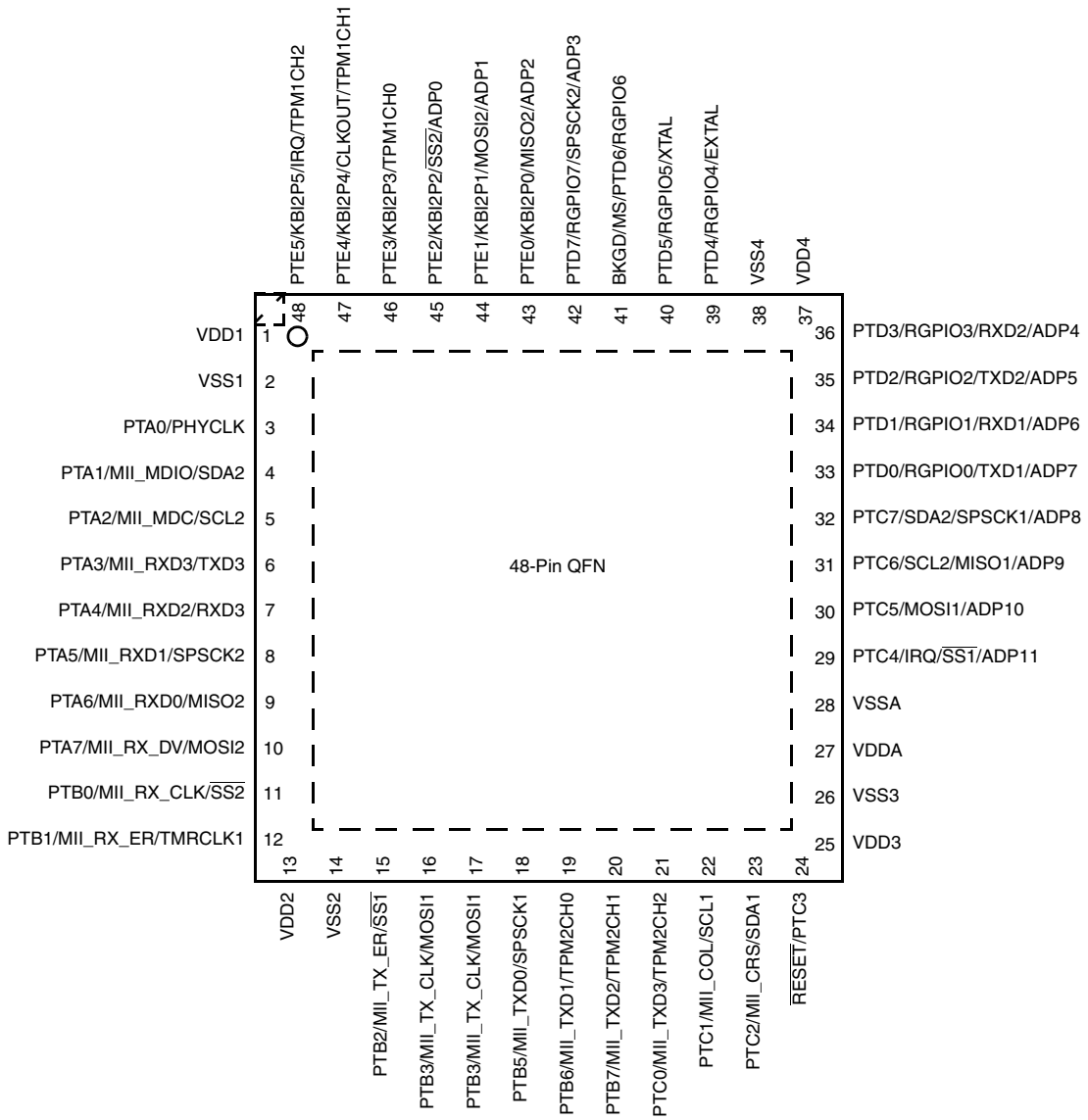


Figure 4. Pin Assignments in 48-Pin QFN Package

NOTE

There is no electrical connection to the flag for 48-pin QFN packages.

Table 2. Package Pin Assignments

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
1	1	1	VDD1	—	—	—	—
2	2	2	VSS1	—	—	—	—
3	3	3	PTA0	PHYCLK	—	—	—

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H (–40 to 85 or 0 to 70)[1]	°C
Maximum junction temperature		T_{JM}	95	°C
Thermal resistance Single-layer board				
	48-pin QFN	θ_{JA}	81	°C/W
	64-pin LQFP		69	
	80-pin LQFP		60	
Thermal resistance Four-layer board				
	48-pin QFN	θ_{JA}	26	°C/W
	64-pin LQFP		50	
	80-pin LQFP		47	

1 Depending on device.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

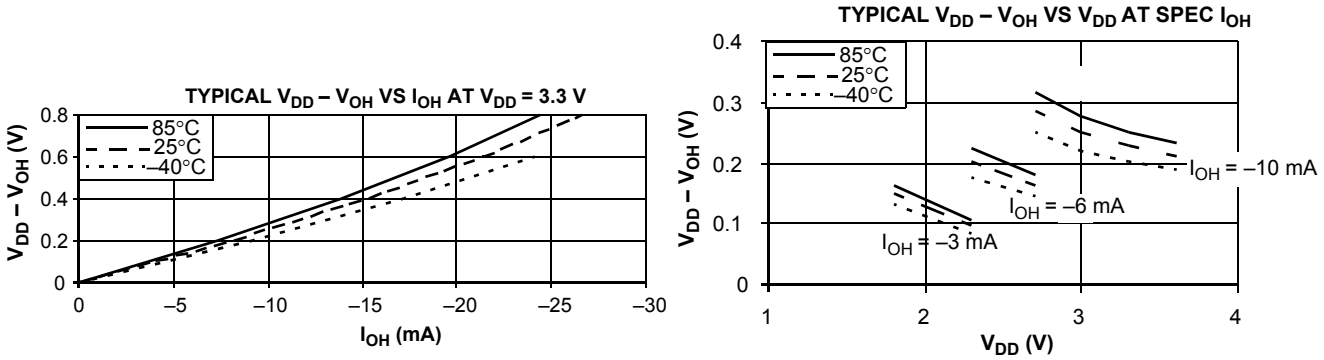


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25 MHz	3.3	60	75	mA	–40 to 85 °C
	T			20 MHz		49	—		
	T			8 MHz		21	—		
	T			1 MHz		4.6	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25 MHz	3.3	44	47	mA	–40 to 85 °C
	T			20 MHz		36	—		
	T			8 MHz		15.5	—		
	T			1 MHz		3.9	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3.3	203	—	µA	–40 to 85 °C
	T			16 kHz FBELP		154	—		
4	T	Run supply current LPRS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3.3	50	—	µA	–40 to 85 °C
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25 MHz	3.3	11	13.7	µA	–-40 to 85 °C
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3.3	0.35	11	µA	0 to 70 °C
	P						45		–40 to 85 °C
	C				1.8	0.35	12		0 to 70 °C
	C						16.2		–40 to 85 °C

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 25 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	 Ω KΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 200 400 5 15	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) External with FLL / PLL enabled (FEE / PEE) External with bypass (FBE.FBELP,PBE, PBELP)	f_{extal}	 0.03125 0	 — —	 50.33 50.33	 MHz MHz

1 Data in Typical column was characterized at 3.3 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

Table 11. MCG Frequency Specifications (continued)(Temperature Range = –40 to 125 °C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
9	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
11	C	FLL acquisition time [2]	$t_{fll\_acquire}$	—	—	1	ms
12	D	PLL acquisition time [3]	$t_{pll\_acquire}$	—	—	1	ms
13	C	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
14	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
15	D	Lock entry frequency tolerance[5]	D_{lock}	± 1.49	—	± 2.98	%
16	D	Lock exit frequency tolerance[6]	D_{unl}	± 4.47	—	± 5.97	%
17	D	Lock time - FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time - PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency - RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG does not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG does not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

3.10 Mini-FlexBus Timing Specifications

A multi-function external bus interface called Mini-FlexBus is provided with basic functionality to interface to slave-only devices up to a maximum bus frequency of 25.1666 MHz. It can be directly connected to asynchronous or synchronous devices such as external boot ROMs, flash memories, gate-array logic, or other simple target (slave) devices with little or no additional circuitry. For asynchronous devices a simple chip-select based interface can be used.

All processor bus timings are synchronous; that is, input setup/hold and output delay are given in respect to the rising edge of a reference clock, MB_CLK. The MB_CLK frequency is half the internal system bus frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Mini-FlexBus output clock (MB_CLK). All other timing relationships can be derived from these values.

Table 12. Mini-FlexBus AC Timing Specifications

Num	C	Characteristic	Min	Max	Unit	Notes
—	—	Frequency of Operation	—	25.1666	MHz	—
MB1	D	Clock Period	39.73	—	ns	—
MB2	P	Output Valid	—	20	ns	1
MB3	D	Output Hold	1.0	—	ns	1
MB4	P	Input Setup	22	—	ns	2
MB5	D	Input Hold	10	—	ns	2

1 Specification is valid for all MB_A[19:0], MB_D[7:0], $\overline{\text{MB\_CS}}$[1:0], $\overline{\text{MB\_OE}}$, MB_R/$\overline{\text{W}}$, and MB_ALE.

2 Specification is valid for all MB_D[7:0].

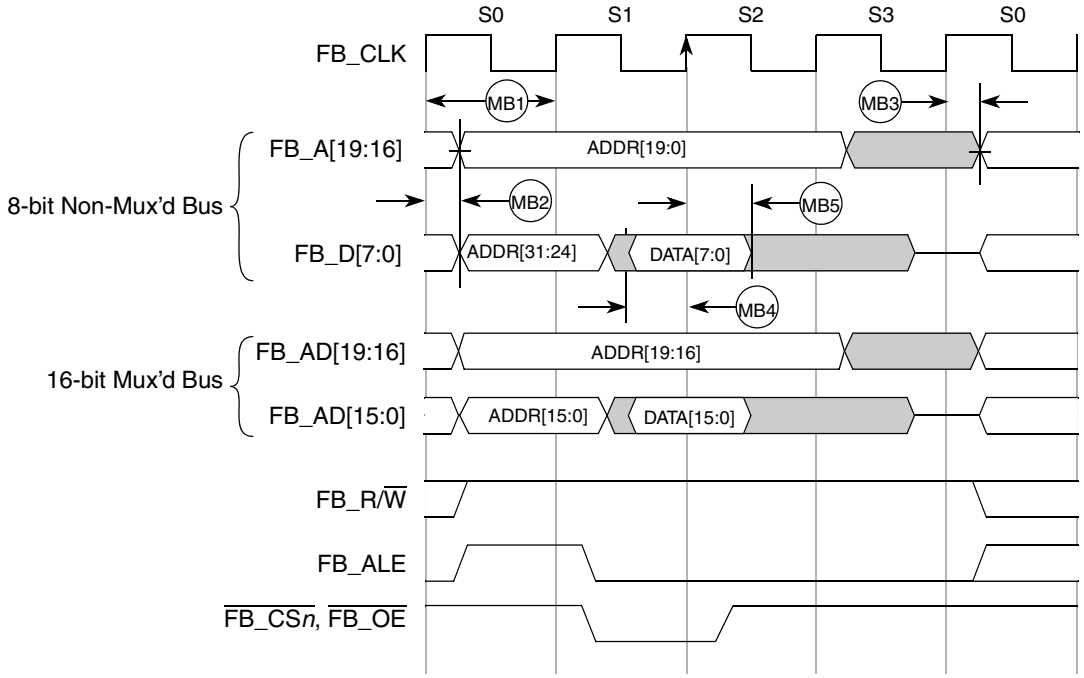


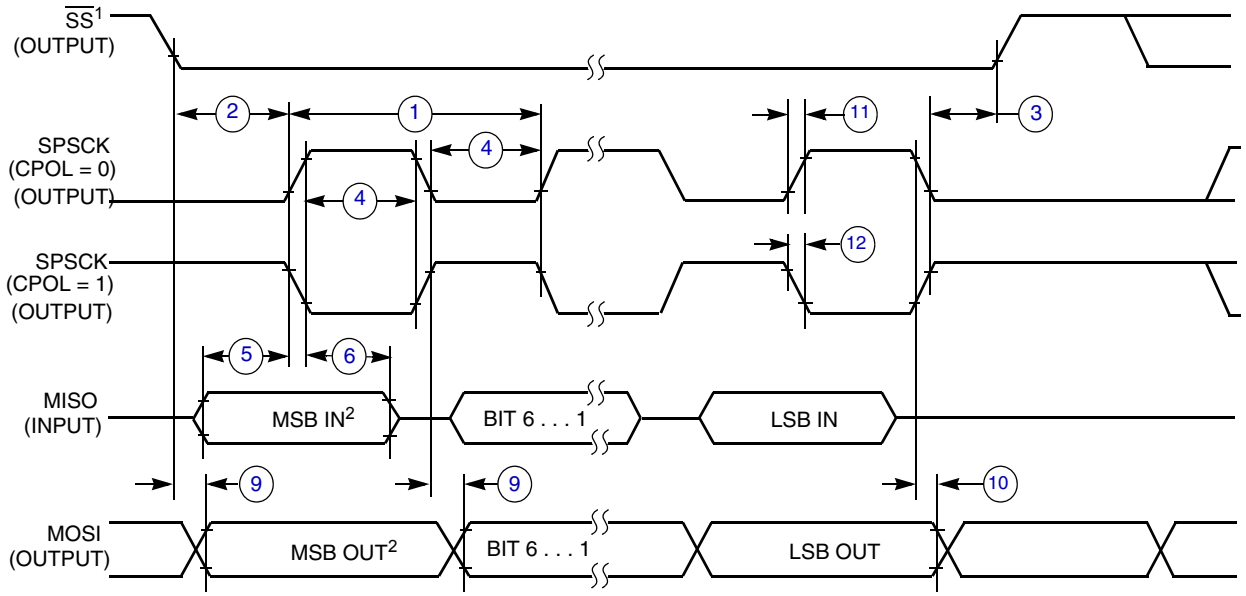
Figure 13. Mini-FlexBus Read Timing

3.12.3 SPI Timing

Table 19 and Figure 23 through Figure 26 describe the timing requirements for the SPI system.

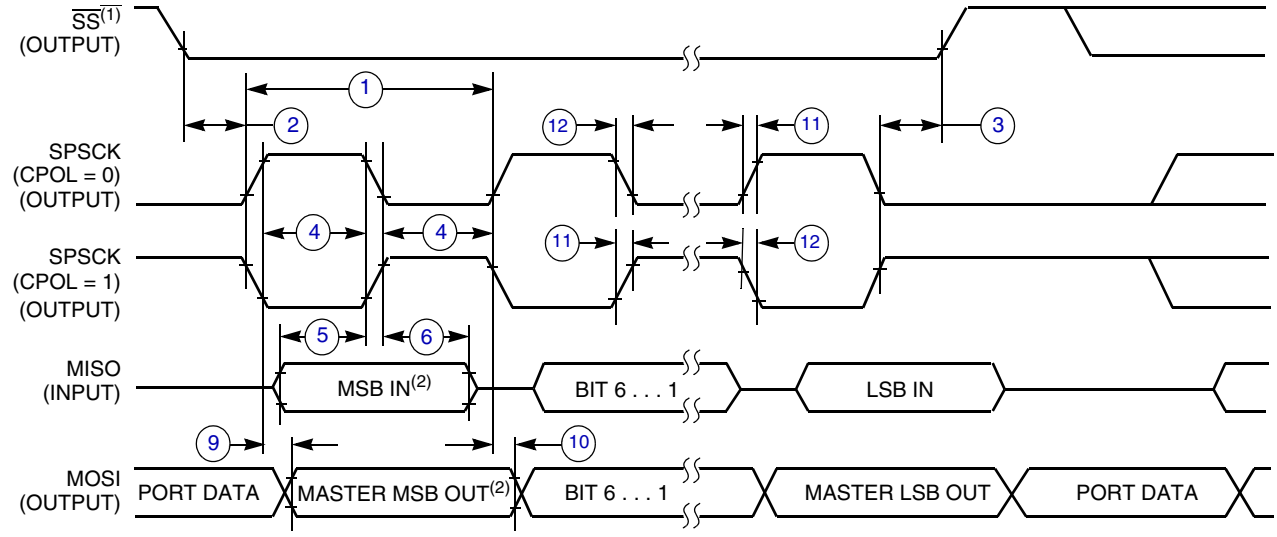
Table 19. SPI Timing

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	 $f_{Bus}/2048$ 0	 $f_{Bus}/2$ $f_{Bus}/4$	 Hz Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	 2 4	 2048 —	 t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	 1/2 1	 — —	 t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	 $t_{cyc} - 30$ $t_{cyc} - 30$	 1024 t_{cyc} —	 ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	 15 15	 — —	 ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	 0 25	 — —	 ns ns
7	D	Slave access time	t_a	—	1	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	1	t_{cyc}
9	D	Data valid (after SPSCK edge) Master Slave	t_v	 — —	 25 25	 ns ns
10	D	Data hold time (outputs) Master Slave	t_{HO}	 0 0	 — —	 ns ns
11	D	Rise time Input Output	 t_{RI} t_{RO}	 — —	 $t_{cyc} - 25$ 25	 ns ns
12	D	Fall time Input Output	 t_{FI} t_{FO}	 — —	 $t_{cyc} - 25$ 25	 ns ns



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 23. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 24. SPI Master Timing (CPHA =1)

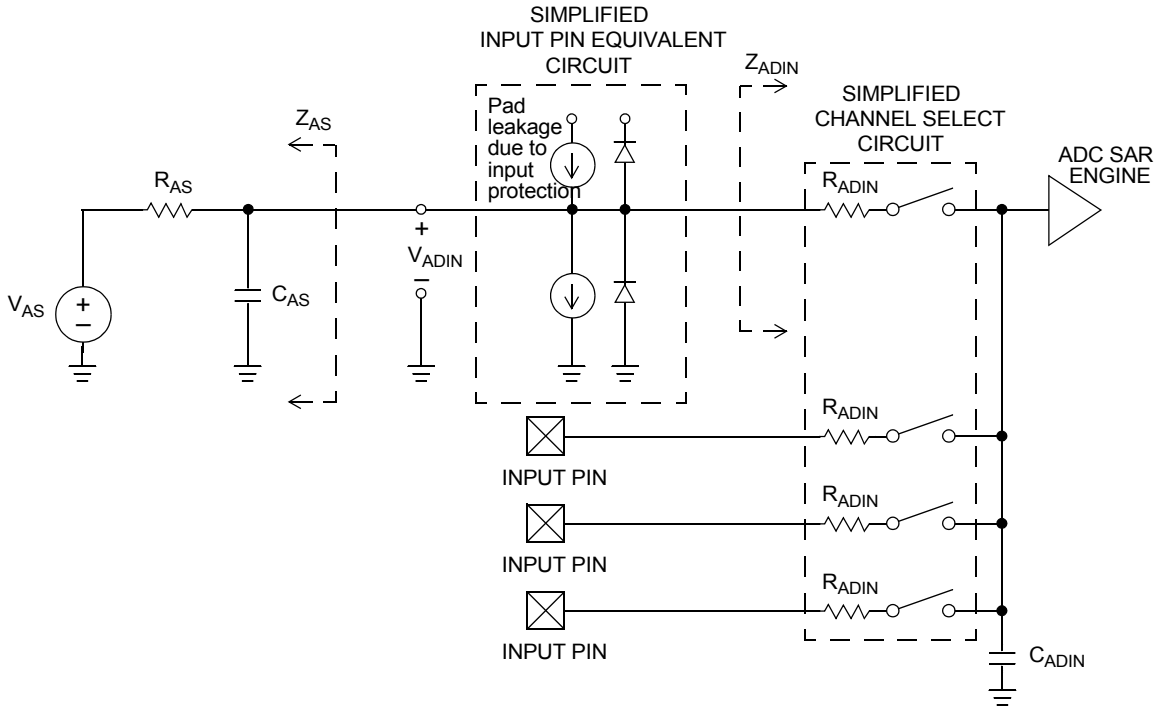


Figure 27. ADC Input Impedance Equivalency Diagram

Table 21. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	202	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	288	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	D	I_{DDAD}	—	0.007	0.8	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)	C		1.25	2	3.3		

Table 21. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD}) (continued)

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Conversion Time (Including sample time)	Short Sample (ADLSMP=0)	P	t_{ADC}	—	20	—	ADCK cycles	See the ADC chapter in the *MCF51CN128 Reference Manual* for conversion time variances
	Long Sample (ADLSMP=1)	C		—	40	—		
Sample Time	Short Sample (ADLSMP=0)	P	t_{ADS}	—	3.5	—	ADCK cycles	
	Long Sample (ADLSMP=1)	C		—	23.5	—		
Total Unadjusted Error	12 bit mode	T	E_{TUE}	—	±3.0	—	LSB[2]	Includes Quantization
	10 bit mode	P		—	±1	±2.5		
	8 bit mode	T		—	±0.5	±1.0		
Differential Non-Linearity	12 bit mode	T	DNL	—	±1.75	—	LSB[2]	
	10 bit mode[3]	P		—	±0.5	±1.0		
	8 bit mode[3]	T		—	±0.3	±0.5		
Integral Non-Linearity	12 bit mode	T	INL	—	±1.5	—	LSB[2]	
	10 bit mode	P		—	±0.5	±1.0		
	8 bit mode	T		—	±0.3	±0.5		
Zero-Scale Error	12 bit mode	T	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	10 bit mode	P		—	±0.5	±1.5		
	8 bit mode	T		—	±0.5	±0.5		
Full-Scale Error	12 bit mode	T	E_{FS}	—	±1.0	—	LSB[2]	V_{ADIN} = V_{DDAD}
	10 bit mode	P		—	±0.5	±1		
	8 bit mode	T		—	±0.5	±0.5		
Quantization Error	12 bit mode	D	E_Q	—	-1 to 0	—	LSB[2]	
	10 bit mode			—	—	±0.5		
	8 bit mode			—	—	±0.5		
Input Leakage Error	12 bit mode	D	E_{IL}	—	±2	—	LSB[2]	Pad leakage[4] * $R_{AS\{test=pad\ leakage\ test\}}$
	10 bit mode			—	±0.2	±4		
	8 bit mode			—	±0.1	±1.2		
Temp Sensor Slope	-40°C to 25°C	D	m	—	1.646	—	mV/°C	
	25°C to 85°C			—	1.769	—		
Temp Sensor Voltage	25°C	D	V_{TEMP25}	—	701.2	—	mV	

1 Typical values assume V_{DDAD} = 3.3 V, Temp = 25 °C, f_{ADCK}=1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

3.13.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

4 Ordering Information

This section contains ordering information for MCF51CN128 devices.

Table 23. Ordering Information

Freescale Part Number[1]	Memory		Temperature Range (°C)	Package[2]
	Flash	RAM		
MCF51CN128CLK	128K	24K	–40 to +85	80-pin LQFP
MCF51CN128CLH	128K	24K	–40 to +85	64-pin LQFP
MCF51CN128CGT	128K	24K	–40 to +85	48-pin QFN

1 See the *MCF51CN128 Reference Manual* (document MCF51CN128RM), for a complete description of modules included on each device.

2 See Table 24 for package information.

5 Package Information

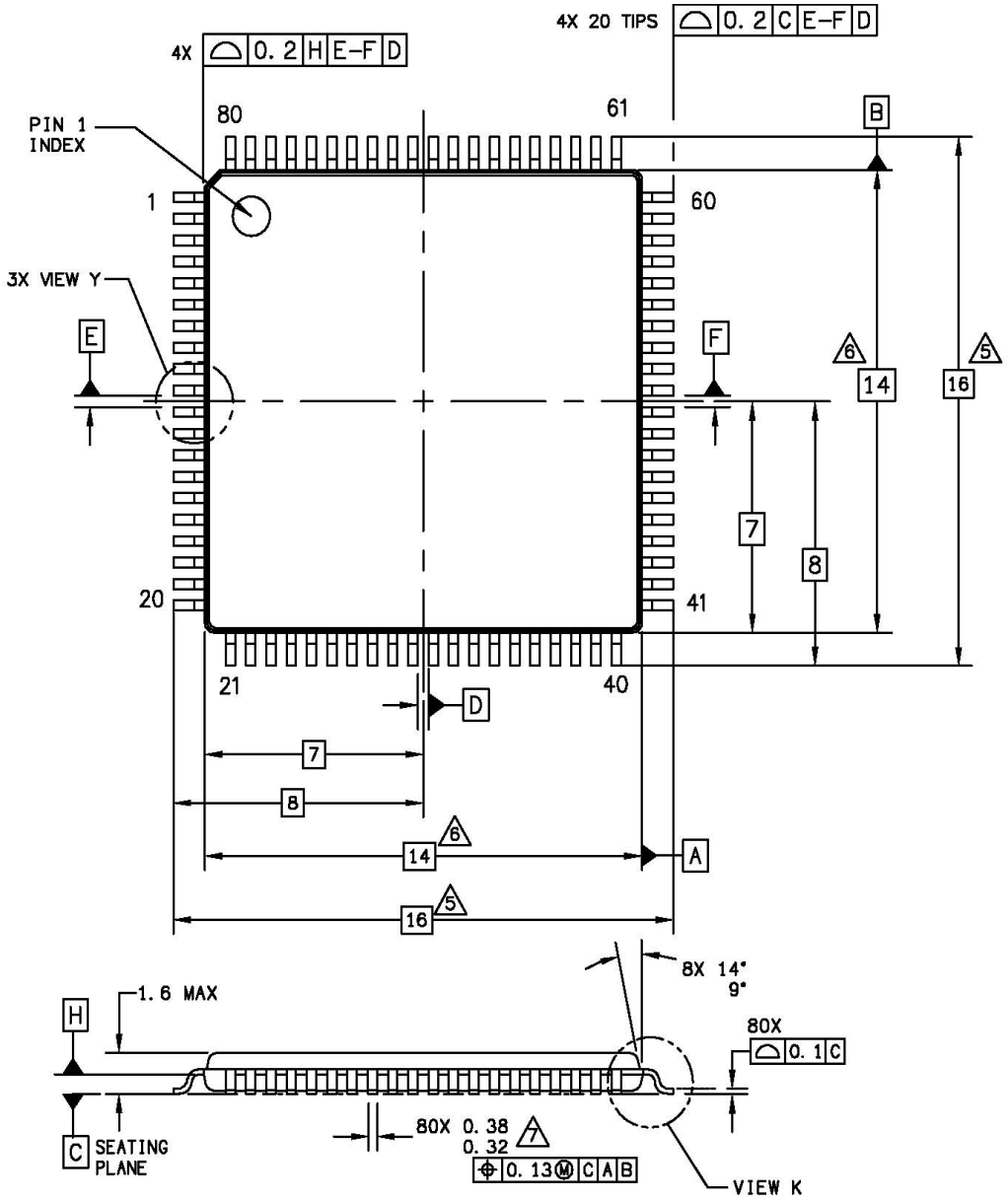
Table 24. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
48	Quad Flat No-Leads	QFN	GT	1314	98ARH99048A

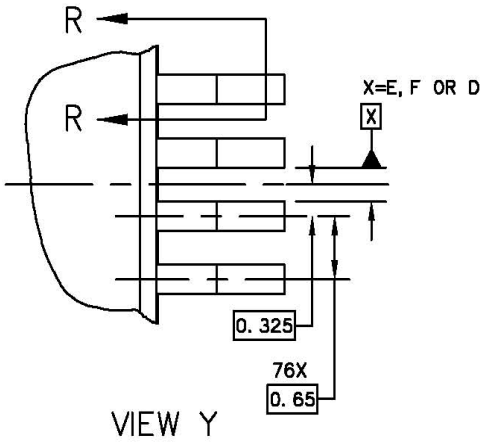
6 Mechanical Outline Drawings

The following pages are mechanical drawings for the packages described in Table 24. For the latest available drawings, visit freescale web site (http://www.freescale.com) and enter the package's document number into the keyword search box.

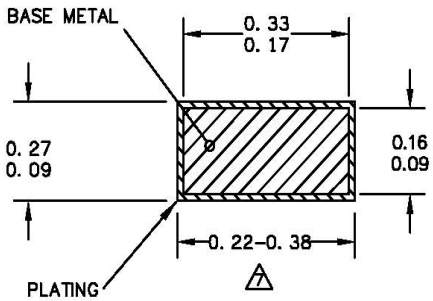
6.1 80-pin LQFP



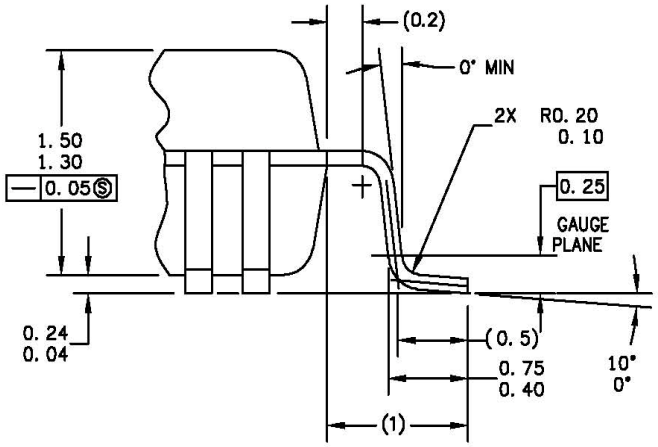
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23237W	REV: E
	CASE NUMBER: 917A-03	28 APR 2006
	STANDARD: NON-JEDEC	



VIEW Y



SECTION R–R
ROTATED 90° CW



VIEW K

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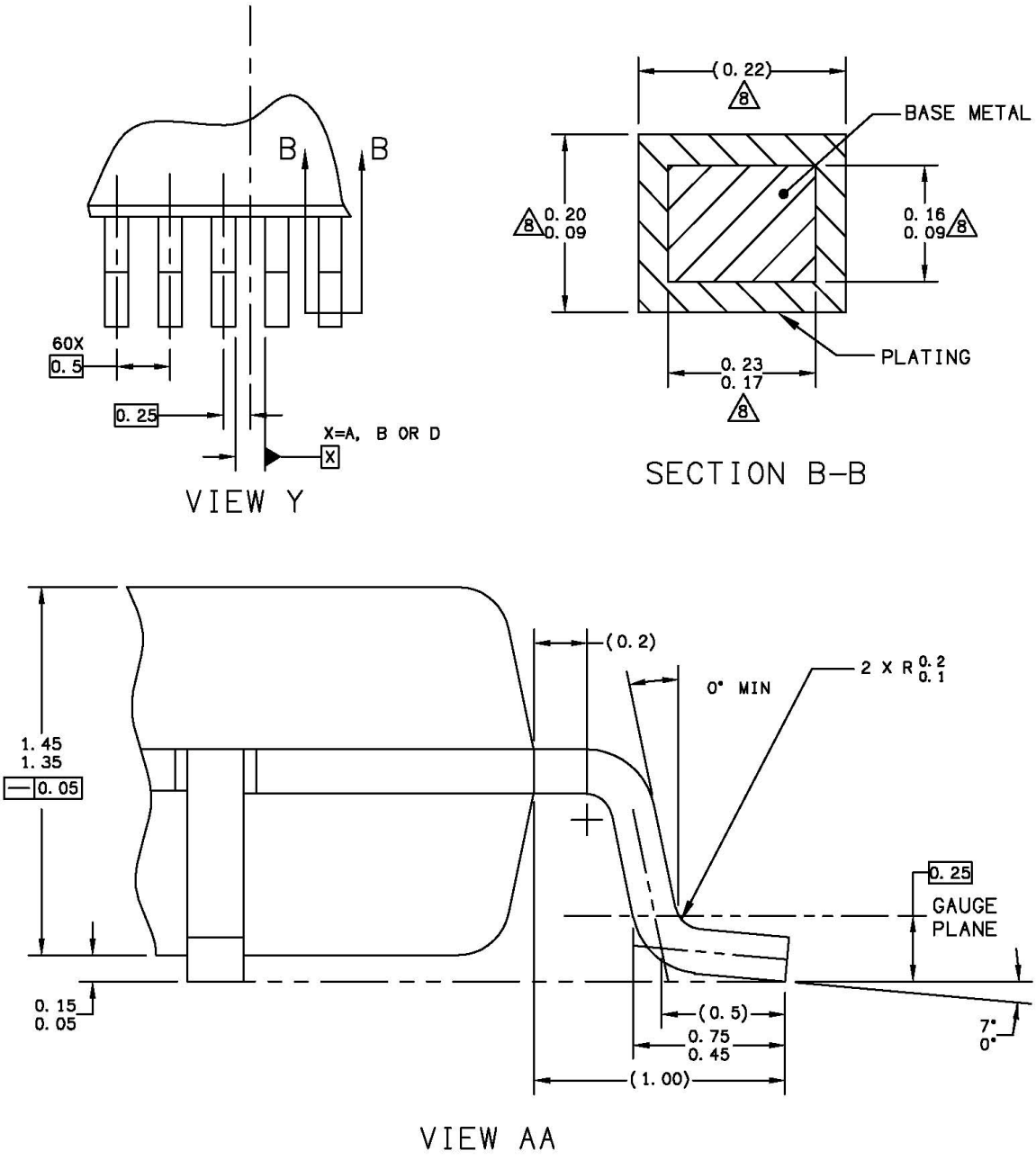
TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	DOCUMENT NO: 98ASS23237W	REV: E
	CASE NUMBER: 917A-03	28 APR 2006
	STANDARD: NON-JEDEC	



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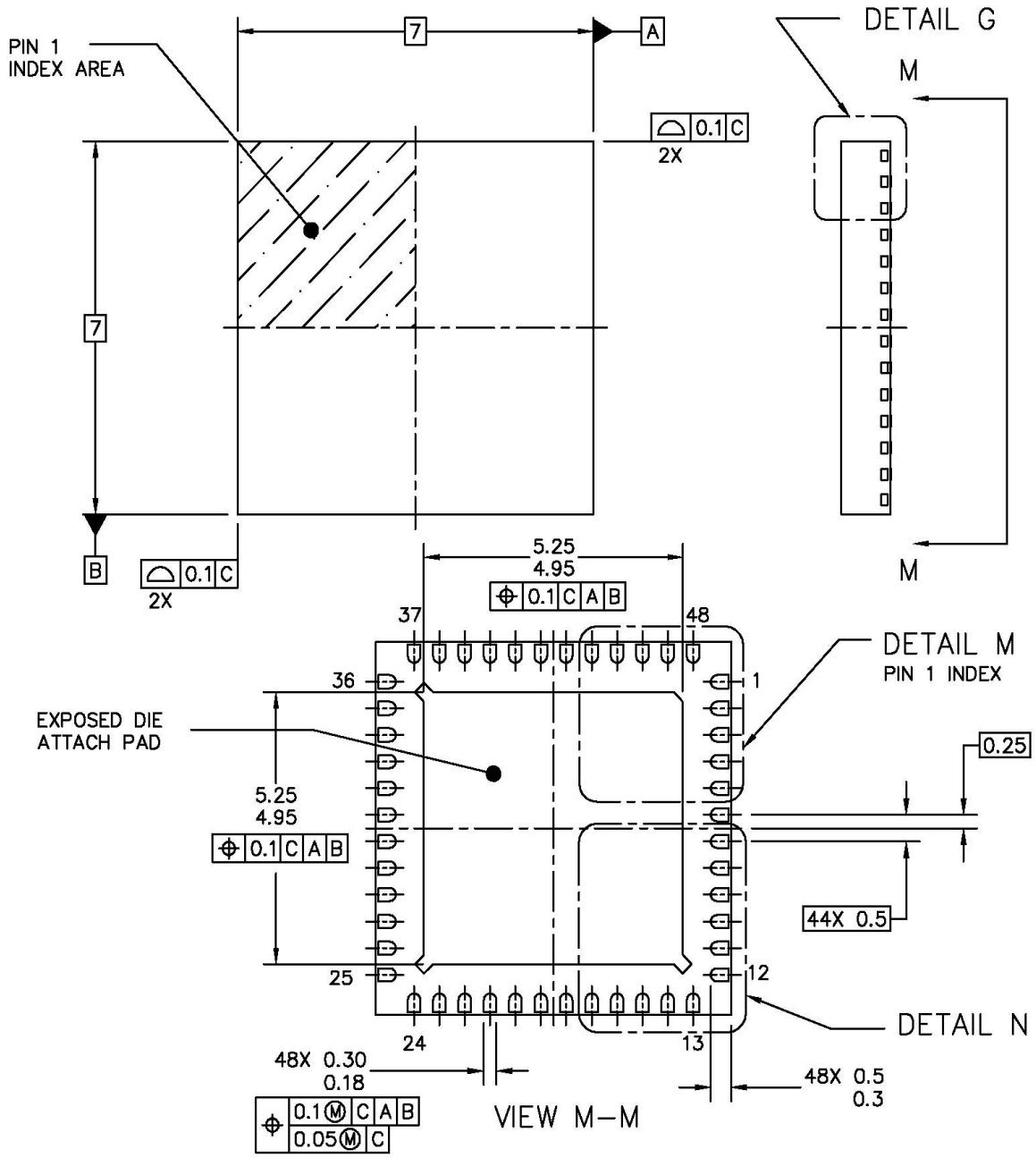
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	

6.3 48-pin QFN



© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	