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What is "Embedded - Microcontrollers"?

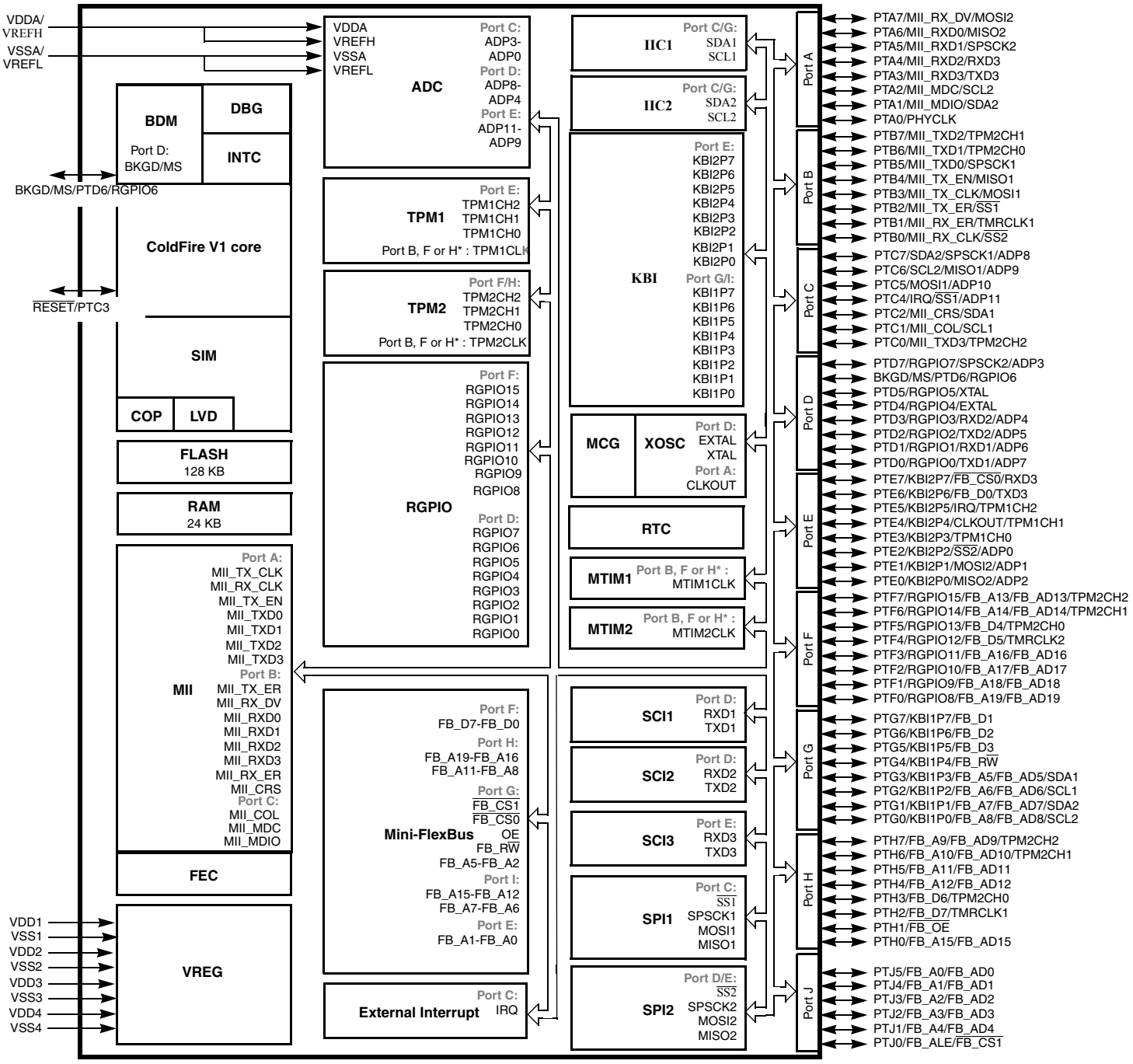
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	EBI/EMI, Ethernet, I²C, SCI, SPI
Peripherals	LVD, PWM, WDT
Number of I/O	70
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	24K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51cn128clk

1.2 Block Diagram

The following figure shows the connections between the MCF51CN128 series pins and modules.



* TPMx and MTIMx external clocks each have the choice of being assigned to either TMRCLK1 or TMRCLK2.

Figure 1. MCF51CN128 Series Block Diagram

2 Pin Assignments

This section describes the pin assignments for the available packages. See for pin availability by package pin-count.

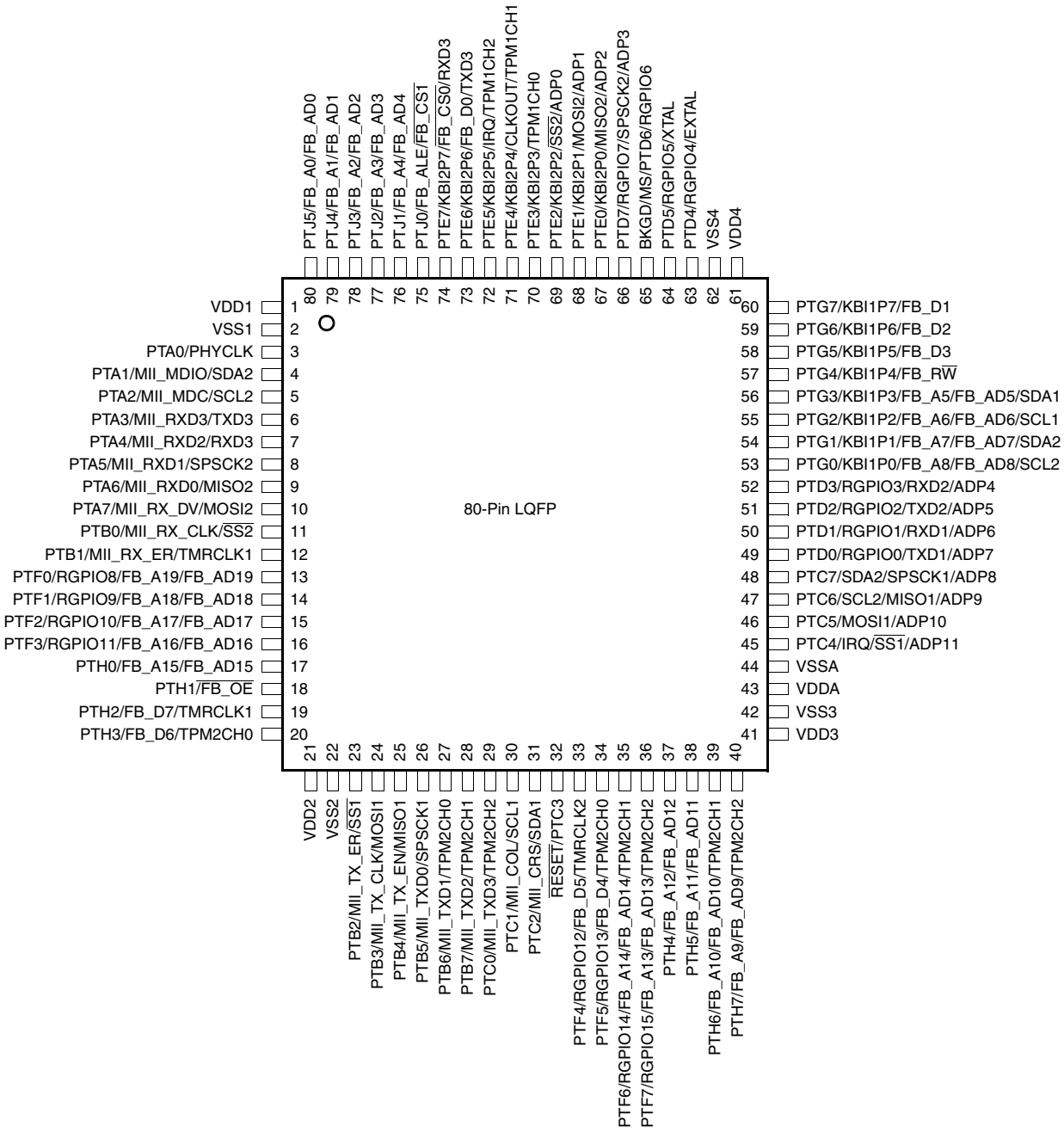


Figure 2. Pin Assignments in 80-Pin LQFP Package

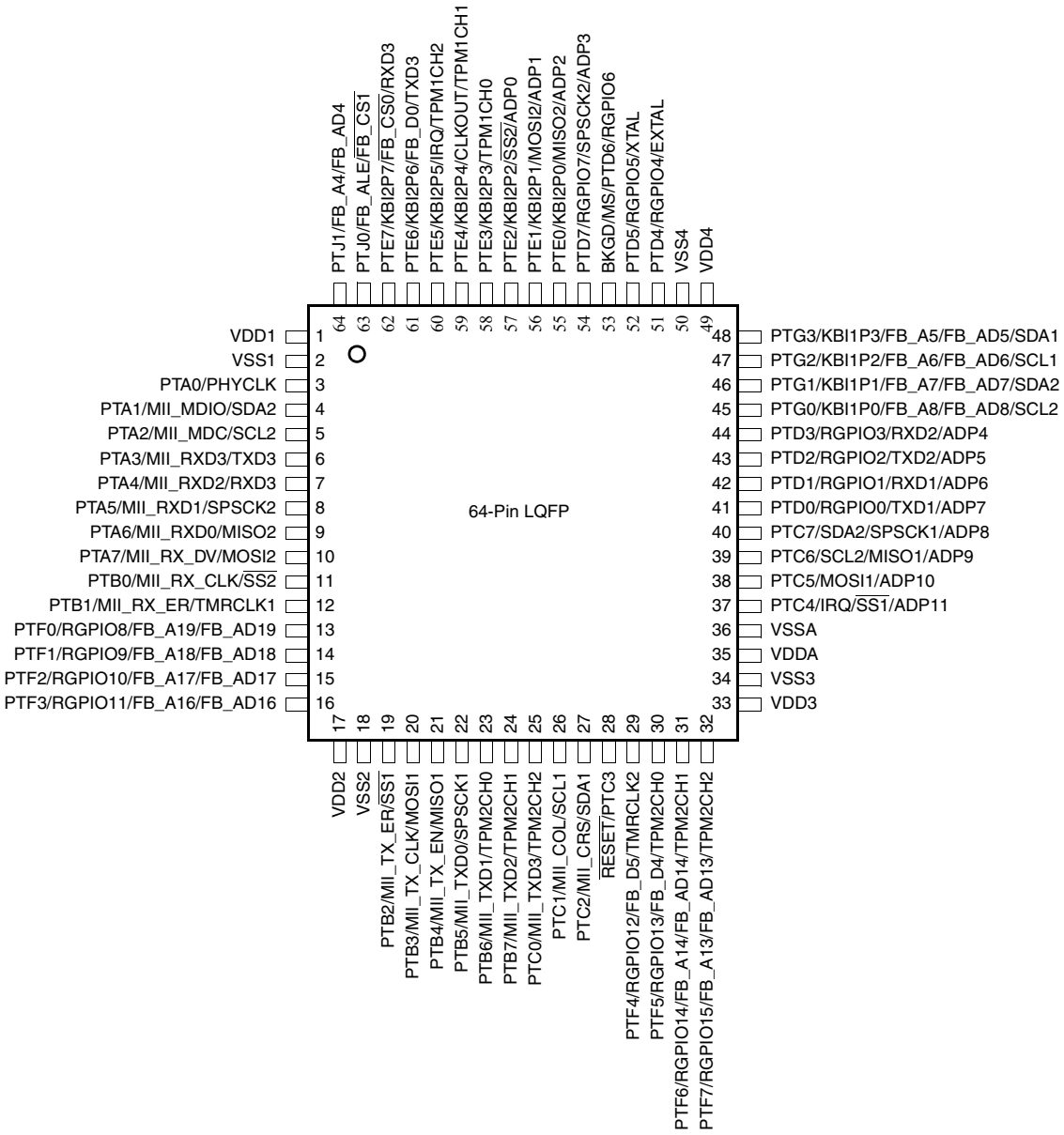


Figure 3. Pin Assignments in 64-Pin LQFP Package

Table 2. Package Pin Assignments (continued)

80-Pin	64-Pin	48-Pin	Default Function	Alt 1	Alt 2	Alt 3	Comment
60	—	—	PTG7	KBI1P7	FB_D1	—	—
61	49	37	VDD4	—	—	—	—
62	50	38	VSS4	—	—	—	—
63	51	39	PTD4/RGPIO4	—	—	EXTAL	RGPIO_ENB selects between standard GPIO and RGPIO
64	52	40	PTD5/RGPIO5	—	—	XTAL	
65	53	41	BKGD/MS	PTD6/RGPIO6	—	—	This pin has an internal pullup. PTD6/RGPIO6 can only be programmed as an output.[1]
66	54	42	PTD7RGPIO7	—	SPSCK2	ADP3	RGPIO_ENB selects between standard GPIO and RGPIO
67	55	43	PTE0	KBI2P0	MISO2	ADP2	—
68	56	44	PTE1	KBI2P1	MOSI2	ADP1	—
69	57	45	PTE2	KBI2P2	$\overline{SS2}$	ADP0	—
70	58	46	PTE3	KBI2P3	—	TPM1CH0	—
71	59	47	PTE4	KBI2P4	CLKOUT	TPM1CH1	—
72	60	48	PTE5	KBI2P5	IRQ	TPM1CH2	—
73	61	—	PTE6	KBI2P6	FB_D0	TXD3	—
74	62	—	PTE7	KBI2P7	$\overline{FB\_CS0}$	RXD3	—
75	63	—	PTJ0	FB_ALE	$\overline{FB\_CS1}$	—	—
76	64	—	PTJ1	—	FB_A4/FB_AD4	—	—
77	—	—	PTJ2	—	FB_A3/FB_AD3	—	—
78	—	—	PTJ3	—	FB_A2/FB_AD2	—	—
79	—	—	PTJ4	—	FB_A1/FB_AD1	—	—
80	—	—	PTJ5	—	FB_A0/FB_AD0	—	—

[1] RGPIO_ENB selects between standard GPIO and RGPIO. When PTD6 is set as RGPIO output, and "1" is driven to PTD6 via RGPIO function, a read of register RGPIODATA6 always returns a "0" because V1 RGPIO design looks for IO enable when the return value of RGPIO function reads data. As PTD6 is set to RGPIO output only, it returns "0" always to RGPIODATA6, athough PTD6 pin is driven to high.

3 Electrical Characteristics

3.1 Introduction

This section contains electrical and timing specifications for the MCF51CN128 series of microcontrollers available at the time of publication.

3.4 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and voltage regulator circuits, and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} will be very small.

Table 5. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	T_L to T_H (–40 to 85 or 0 to 70)[1]	°C
Maximum junction temperature		T_{JM}	95	°C
Thermal resistance Single-layer board				
	48-pin QFN	θ_{JA}	81	°C/W
	64-pin LQFP		69	
	80-pin LQFP		60	
Thermal resistance Four-layer board				
	48-pin QFN	θ_{JA}	26	°C/W
	64-pin LQFP		50	
	80-pin LQFP		47	

1 Depending on device.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

3.6 DC Characteristics

This section includes information about power supply requirements and I/O pin characteristics.

Table 8. DC Characteristics

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
1	—	Operating Voltage[2]	—	—	1.8[3]	—	3.6	V
2	C	Output high voltage — All I/O pins, low-drive strength	V_{OH}	1.8 V, I_{Load} = –2 mA	V_{DD} – 0.5	—	—	V
	P	Output high voltage — All I/O pins, high-drive strength		2.7 V, I_{Load} = –10 mA	V_{DD} – 0.5	—	—	
	T			2.3 V, I_{Load} = –6 mA	V_{DD} – 0.5	—	—	
	C			1.8V, I_{Load} = –3 mA	V_{DD} – 0.5	—	—	
3	D	Output high current — Max total I_{OH} for all ports	I_{OHT}	—	—	—	100	mA
4	C	Output low voltage — All I/O pins, low-drive strength	V_{OL}	1.8 V, I_{Load} = 2 mA	—	—	0.5	V
	P	Output low voltage — All I/O pins, high-drive strength		2.7 V, I_{Load} = 10 mA	—	—	0.5	
	T			2.3 V, I_{Load} = 6 mA	—	—	0.5	
	C			1.8 V, I_{Load} = 3 mA	—	—	0.5	
5	D	Output low current — Max total I_{OL} for all ports	I_{OLT}	—	—	—	100	mA
6	P	Input high voltage — all digital inputs	V_{IH}	V_{DD} > 2.7 V	0.70 x V_{DD}	—	—	V
	C			V_{DD} > 1.8 V	0.85 x V_{DD}	—	—	
7	P	Input low voltage — all digital inputs	V_{IL}	V_{DD} > 2.7 V	—	—	0.35 x V_{DD}	
	C			V_{DD} >1.8 V	—	—	0.30 x V_{DD}	
8	C	Input hysteresis — all digital inputs	V_{hys}	—	0.06 x V_{DD}	—	—	mV
9	P	Input leakage current — all input only pins (Per pin)	$\lvert I_{In} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
10	P	Hi-Z (off-state) leakage current — all input/output (per pin)	$\lvert I_{OZ} \rvert$	V_{In} = V_{DD} or V_{SS}	—	0.1	1	µA
11	P	Pull resistors — all digital inputs, when enabled	R_P	—	17.5	—	52.5	kΩ
12	D	DC injection current [4, 5, 6] — Single pin limit	I_{IC}	V_{IN} < V_{SS}, V_{IN} > V_{DD}	–0.2	—	0.2	mA
		DC injection current [4, 5, 6] — Total MCU limit, includes sum of all stressed pins			–5	—	5	mA
13	C	Input Capacitance, all pins	C_{In}		—	—	8	pF
14	C	POR re-arm voltage[7]	V_{POR}		0.9	1.4	1.79	V
15	D	POR re-arm time	t_{POR}		10	—	—	µs
16	P	Low-voltage detection threshold — high range[8]	V_{LVDH}[9]	V_{DD} falling V_{DD} rising	2.15 2.24	2.32 2.39	2.45 2.49	V

Table 8. DC Characteristics (continued)

Num	C	Characteristic	Symbol	Condition	Min	Typ[1]	Max	Unit
17	P	Low-voltage detection threshold — low range[8]	V_{LVDL}	V_{DD} falling V_{DD} rising	1.70 1.80	1.83 1.89	1.95 2.00	V
18	P	Low-voltage warning threshold — high range[8]	V_{LVWH}	V_{DD} falling V_{DD} rising	2.50 2.50	2.62 2.62	2.70 2.70	V
19	P	Low-voltage warning threshold — low range[8]	V_{LVWL}	V_{DD} falling V_{DD} rising	2.25 2.29	2.32 2.39	2.45 2.49	V
20	P	Bandgap Voltage Reference[10]	V_{BG}	—	1.15	1.17	1.18	V

1 Typical values are measured at 25 °C. Characterized, not tested

2 As an exception, the Fast Ethernet Controller (FEC) is only operational above the operating voltage of 3 V.

3 As the supply voltage rises, the LVD circuit will hold the MCU in reset until the supply has risen above V_{LVDL}.

4 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

5 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

6 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

7 Maximum is highest voltage that POR is guaranteed.

8 Low voltage detection and warning limits measured at 1 MHz bus frequency.

9 Run at 1 MHz bus frequency

10 Factory trimmed at V_{DD} = 3.3 V, Temp = 25 °C

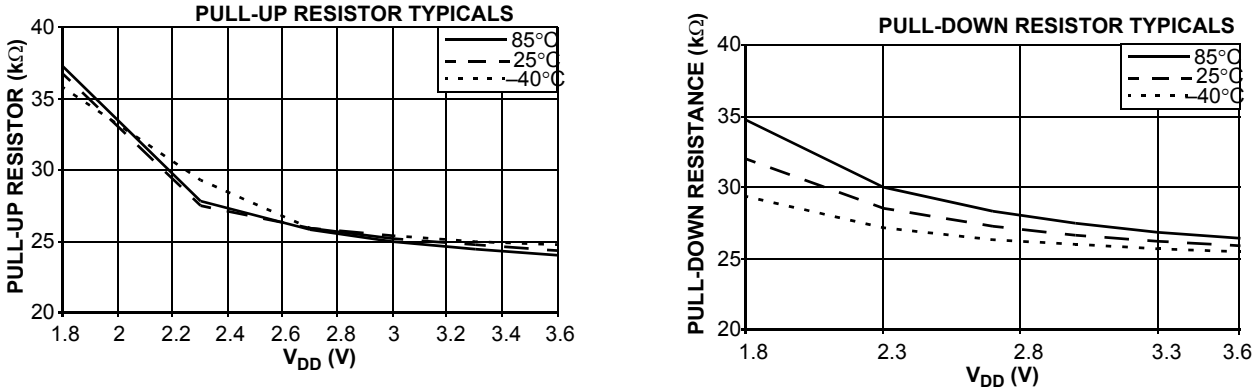


Figure 5. Pull-up and Pull-down Typical Resistor Values

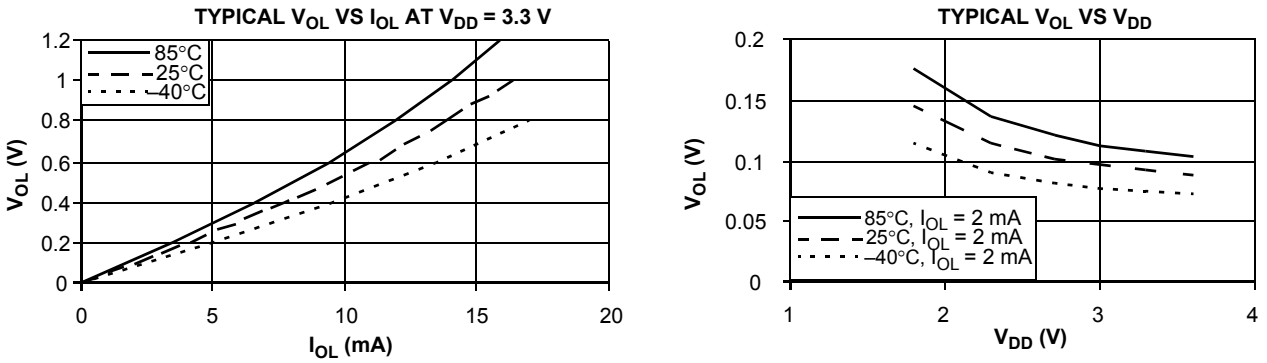


Figure 6. Typical Low-Side Driver (Sink) Characteristics — Low Drive (PTxDSn = 0)

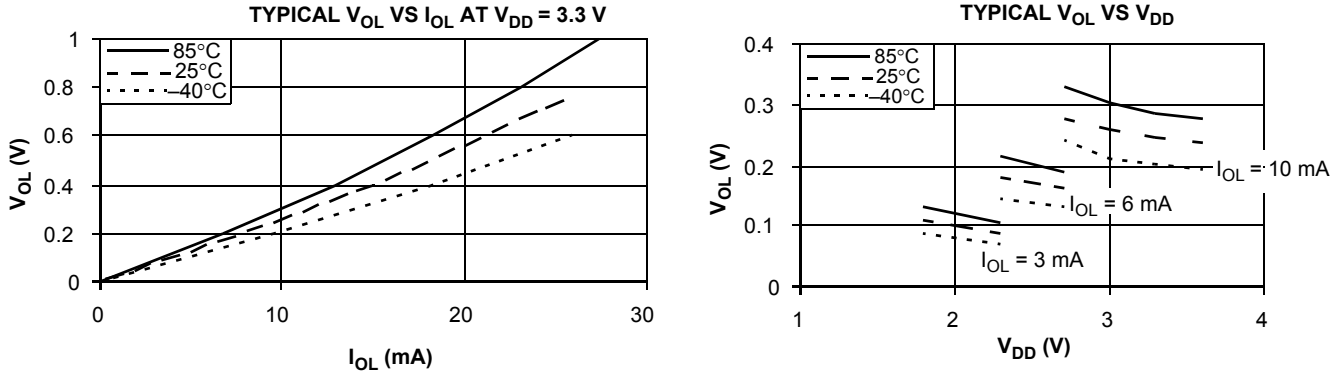


Figure 7. Typical Low-Side Driver (Sink) Characteristics — High Drive (PTxDSn = 1)

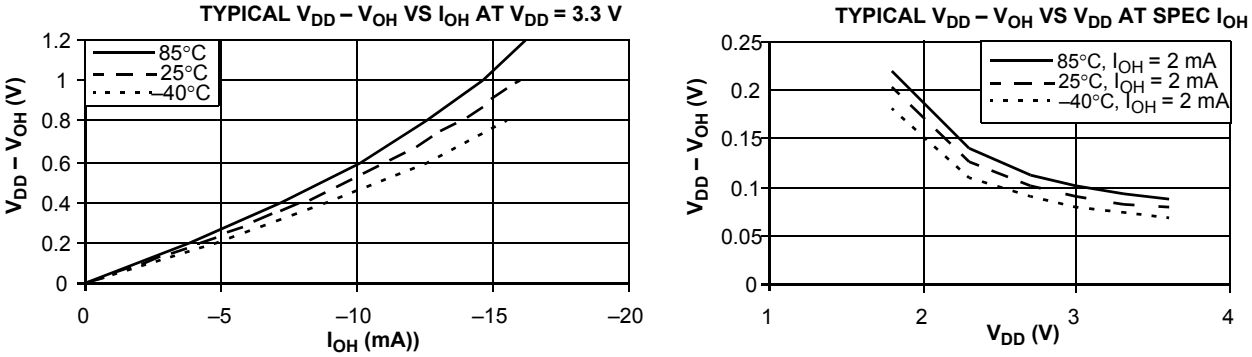


Figure 8. Typical High-Side (Source) Characteristics — Low Drive (PTxDSn = 0)

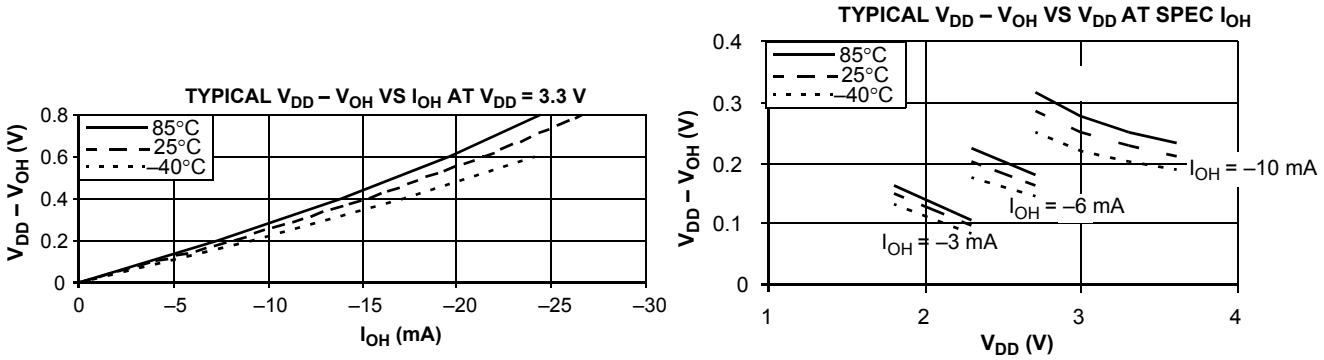


Figure 9. Typical High-Side (Source) Characteristics — High Drive (PTxDSn = 1)

3.7 Supply Current Characteristics

This section includes information about power supply current in various operating modes.

Table 9. Supply Current Characteristics

Num	C	Parameter	Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
1	P	Run supply current FEI mode, all modules on	RI_{DD}	25 MHz	3.3	60	75	mA	–40 to 85 °C
	T			20 MHz		49	—		
	T			8 MHz		21	—		
	T			1 MHz		4.6	—		
2	C	Run supply current FEI mode, all modules off	RI_{DD}	25 MHz	3.3	44	47	mA	–40 to 85 °C
	T			20 MHz		36	—		
	T			8 MHz		15.5	—		
	T			1 MHz		3.9	—		
3	T	Run supply current LPRS=0, all modules off	RI_{DD}	16 kHz FBILP	3.3	203	—	µA	–40 to 85 °C
	T			16 kHz FBELP		154	—		
4	T	Run supply current LPRS=1, all modules off, running from Flash	RI_{DD}	16 kHz FBELP	3.3	50	—	µA	–40 to 85 °C
5	C	Wait mode supply current FEI mode, all modules off	WI_{DD}	25 MHz	3.3	11	13.7	µA	–-40 to 85 °C
	T			20 MHz		4.57	—		
	T			8 MHz		2	—		
	T			1 MHz		0.73	—		
6	C	Stop2 mode supply current	$S2I_{DD}$	n/a	3.3	0.35	11	µA	0 to 70 °C
	P						45		–40 to 85 °C
	C				1.8	0.35	12		0 to 70 °C
	C						16.2		–40 to 85 °C

Table 9. Supply Current Characteristics (continued)

Num	C	Parameter		Symbol	Bus Freq	V_{DD} (V)	Typ[1]	Max	Unit	Temp (°C)
7	C	Stop3 mode supply current No clocks active		$S3I_{DD}$	n/a	3.3	0.52	14	µA	0 to 70 °C
	P							55		–40 to 85 °C
	C					1.8	0.52	15		0 to 70 °C
	C							32.4		–40 to 85 °C
8	T	Low power mode adders:	EREFSTEN=1	—	32 kHz	3.3	500	—	nA	–40 to 85 °C
9	T		IREFSTEN=1		32 kHz		70	—	µA	–40 to 85 °C
10	T		TPM PWM		100 Hz		12	—	µA	–40 to 85 °C
11	T		SCI, SPI, or IIC		300 bps		15	—	µA	–40 to 85 °C
12	T		RTC using LPO		1 kHz		200	—	nA	–40 to 85 °C
13	T		RTC using ICSERCLK		32 kHz		1	—	µA	–40 to 85 °C
14	T		LVD		n/a		100	—	µA	–40 to 85 °C

[1] Data in Typical column was characterized at 3.3 V, 25 °C or is typical recommended value.

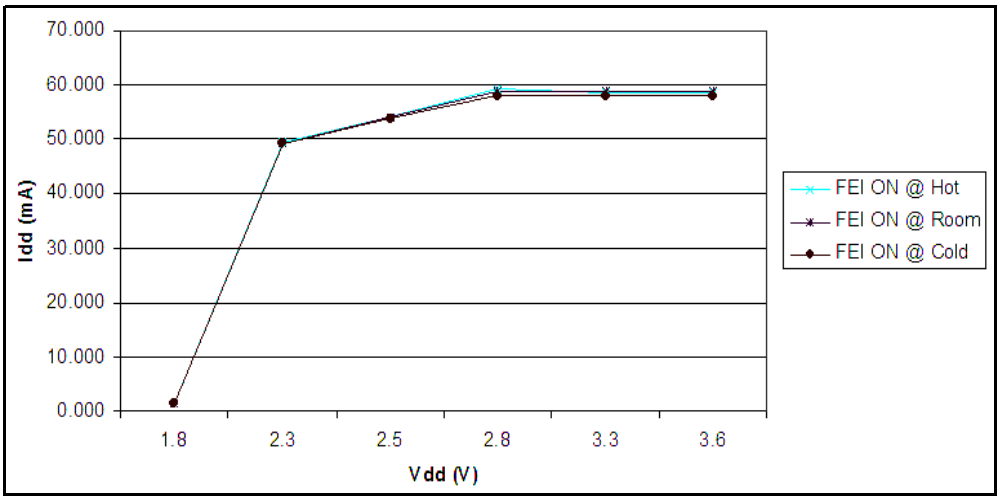


Figure 10. Typical Run I_{DD} for FBE and FEI, I_{DD} vs. V_{DD} (ADC off, All Other Modules Enabled)

3.8 External Oscillator (XOSC) Characteristics

Reference Figure 11 and Figure 12 for crystal or resonator circuits.

Table 10. XOSC and ICS Specifications (Temperature Range = –40 to 85 °C Ambient)

Num	C	Characteristic	Symbol	Min	Typ[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1), high gain (HGO = 1) High range (RANGE = 1), low power (HGO = 0)	 f_{lo} f_{hi} f_{hi}	 32 1 1	 — — —	 38.4 25 8	 kHz MHz MHz
2	D	Load capacitors Low range (RANGE=0), low power (HGO=0) Other oscillator settings	C_1,C_2	See Note[2] See Note[3]			
3	D	Feedback resistor Low range, low power (RANGE=0, HGO=0)[2] Low range, High Gain (RANGE=0, HGO=1) High range (RANGE=1, HGO=X)	R_F	 — — —	 — 10 1	 — — —	MΩ
4	D	Series resistor — Low range, low power (RANGE = 0, HGO = 0)[2] Low range, high gain (RANGE = 0, HGO = 1) High range, low power (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 — 0 100 0 0 0	 — — — 0 10 20	 Ω KΩ
5	C	Crystal start-up time [4] Low range, low power Low range, high power High range, low power High range, high power	 t_{CSTL} t_{CSTH} 	 — — — —	 200 400 5 15	 — — — —	 ms
6	D	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) External with FLL / PLL enabled (FEE / PEE) External with bypass (FBE.FBELP,PBE, PBELP)	f_{extal}	 0.03125 0	 — —	 50.33 50.33	 MHz MHz

1 Data in Typical column was characterized at 3.3 V, 25 °C or is typical recommended value.

2 Load capacitors (C_1,C_2), feedback resistor (R_F) and series resistor (R_S) are incorporated internally when RANGE=HGO=0.

3 See crystal or resonator manufacturer's recommendation.

4 Proper PC board layout procedures must be followed to achieve specifications.

Table 11. MCG Frequency Specifications (continued)(Temperature Range = –40 to 125 °C Ambient)

Num	C	Rating	Symbol	Min	Typical	Max	Unit
8	C	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)	$\Delta f_{dco\_res\_t}$	—	± 0.2	± 0.4	$\%f_{dco}$
9	P	Total deviation of trimmed DCO output frequency over voltage and temperature	Δf_{dco_t}	—	+ 0.5 -1.0	± 2	$\%f_{dco}$
10	C	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 - 70 °C	Δf_{dco_t}	—	± 0.5	± 1	$\%f_{dco}$
11	C	FLL acquisition time [2]	$t_{fll\_acquire}$	—	—	1	ms
12	D	PLL acquisition time [3]	$t_{pll\_acquire}$	—	—	1	ms
13	C	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
14	D	VCO operating frequency	f_{vco}	7.0	—	55.0	MHz
15	D	Lock entry frequency tolerance[5]	D_{lock}	± 1.49	—	± 2.98	%
16	D	Lock exit frequency tolerance[6]	D_{unl}	± 4.47	—	± 5.97	%
17	D	Lock time - FLL	t_{fll_lock}	—	—	$t_{fll\_acquire}$+ 1075(1/f_{int_t})	s
18	D	Lock time - PLL	t_{pll_lock}	—	—	$t_{pll\_acquire}$+ 1075(1/f_{pll_ref})	s
19	D	Loss of external clock minimum frequency - RANGE = 0	f_{loc_low}	(3/5) x f_{int}	—	—	kHz

1 TRIM register at default value (0x80) and FTRIM control bit at default value (0x0).

2 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

3 This specification applies to any time the PLL VCO divider or reference divider is changed, or changing from PLL disabled (BLPE, BLPI) to PLL enabled (PBE, PEE). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry via V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

5 Below D_{lock} minimum, the MCG is guaranteed to enter lock. Above D_{lock} maximum, the MCG does not enter lock. But if the MCG is already in lock, then the MCG may stay in lock.

6 Below D_{unl} minimum, the MCG does not exit lock if already in lock. Above D_{unl} maximum, the MCG is guaranteed to exit lock.

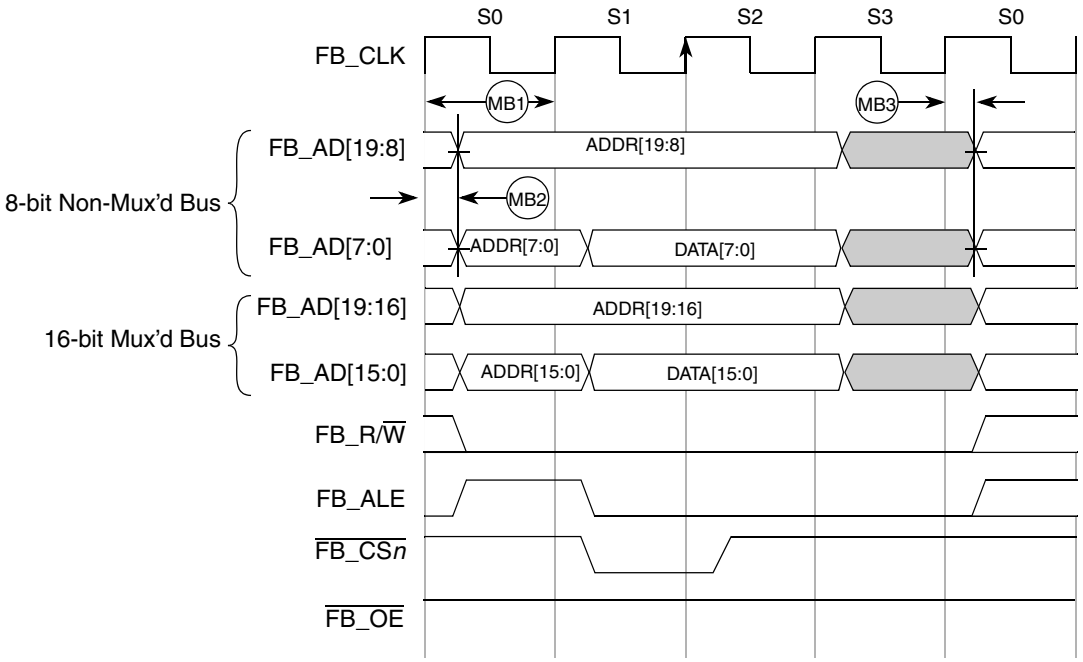


Figure 14. Mini-FlexBus Write Timing

3.11 Fast Ethernet Timing Specifications

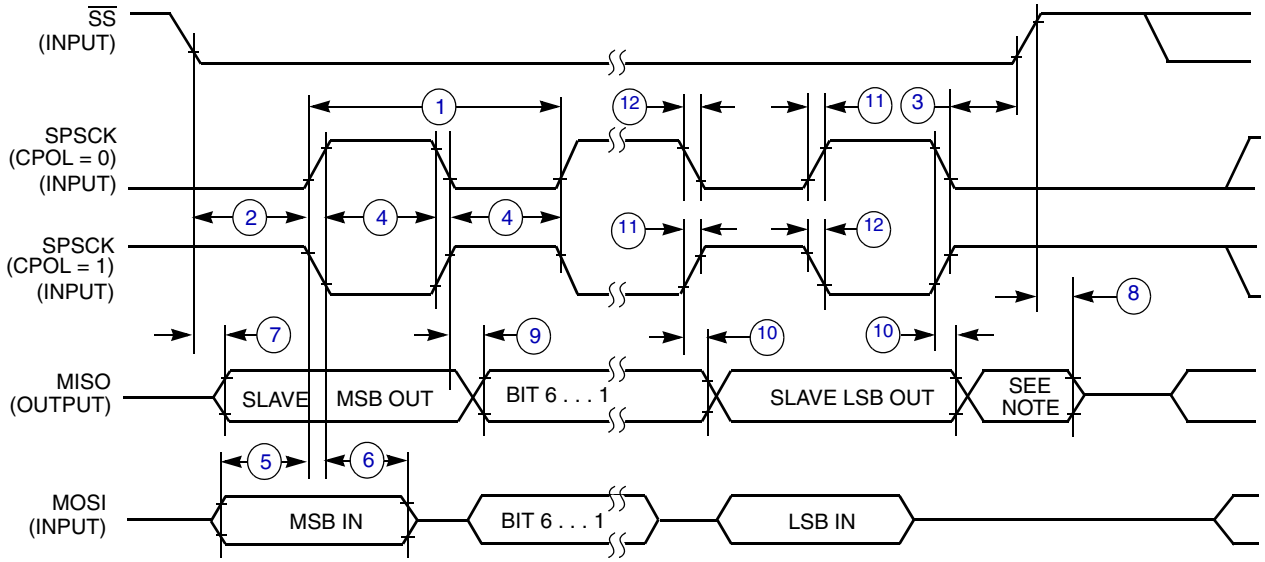
The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

3.11.1 Receive Signal Timing Specifications

The following timing specs meet the requirements for MII and 7-Wire style interfaces for a range of transceiver devices.

Table 13. Receive Signal Timing

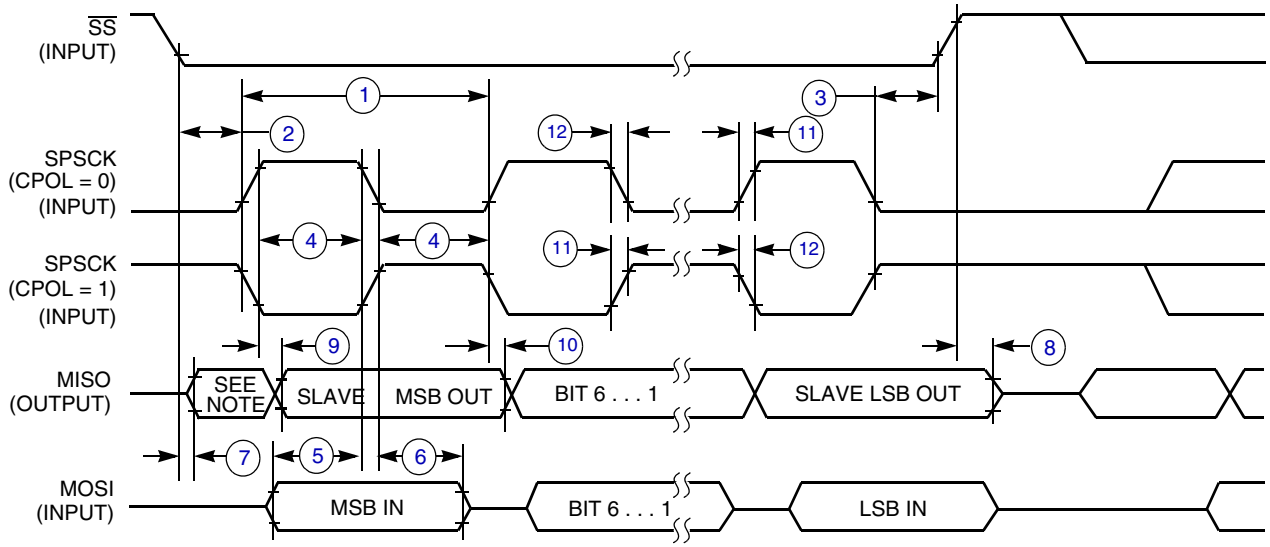
Num	C	Characteristic	MII Mode		Unit
			Min	Max	
—	—	RXCLK frequency	—	25	MHz
E1	P	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
E2	D	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
E3	D	RXCLK pulse width high	35%	65%	RXCLK period
E4	D	RXCLK pulse width low	35%	65%	RXCLK period



NOTE:

1. Not defined but normally MSB of character just received

Figure 25. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 26. SPI Slave Timing (CPHA = 1)

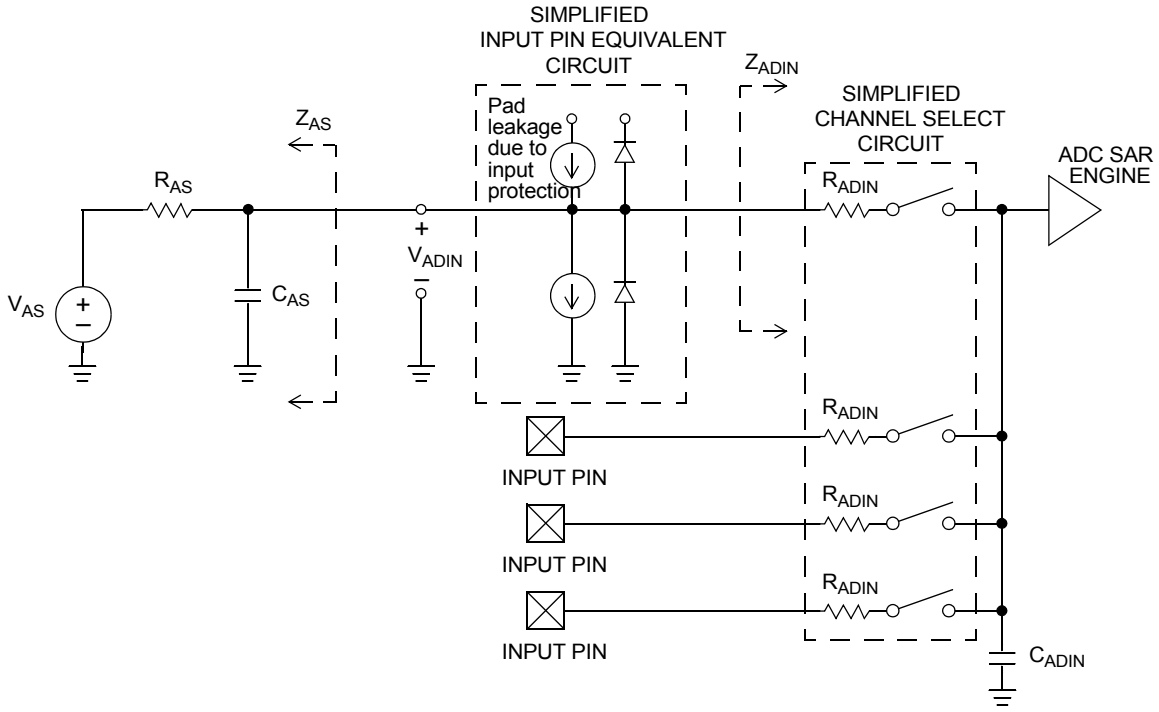


Figure 27. ADC Input Impedance Equivalency Diagram

Table 21. 12-bit ADC Characteristics (V_{REFH} = V_{DDAD}, V_{REFL} = V_{SSAD})

Characteristic	Conditions	C	Symb	Min	Typ[1]	Max	Unit	Comment
Supply Current ADLPC=1 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	120	—	μA	
Supply Current ADLPC=1 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	202	—	μA	
Supply Current ADLPC=0 ADLSMP=1 ADCO=1		T	I_{DDAD}	—	288	—	μA	
Supply Current ADLPC=0 ADLSMP=0 ADCO=1		T	I_{DDAD}	—	0.532	1	mA	
Supply Current	Stop, Reset, Module Off	D	I_{DDAD}	—	0.007	0.8	μA	
ADC Asynchronous Clock Source	High Speed (ADLPC=0)	P	f_{ADACK}	2	3.3	5	MHz	$t_{ADACK} = 1/f_{ADACK}$
	Low Power (ADLPC=1)	C		1.25	2	3.3		

3.12.5 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see the Memory section of the *MCF51CN128 Reference Manual*.

Table 22. Flash Characteristics

C	Characteristic	Symbol	Min	Typical	Max	Unit
D	Supply voltage for program/erase -40 °C to 85 °C	$V_{prog/erase}$	1.8	—	3.6	V
D	Supply voltage for read operation	V_{Read}	1.8	—	3.6	V
D	Internal FCLK frequency[1]	f_{FCLK}	150	—	200	kHz
D	Internal FCLK period (1/FCLK)	t_{Fcyc}	5	—	6.67	µs
P	Longword program time (random location)(2)	t_{prog}	9			t_{Fcyc}
P	Longword program time (burst mode)(2)	t_{Burst}	4			t_{Fcyc}
P	Page erase time[2]	t_{Page}	4000			t_{Fcyc}
P	Mass erase time(2)	t_{Mass}	20,000			t_{Fcyc}
D	Longword program current[3]	R_{IDDBP}	—	9.7	—	mA
D	Page erase current[3]	R_{IDDPE}	—	7.6	—	mA
C	Program/erase endurance[4] T_L to T_H = –40°C to + 85°C T = 25°C		10,000 —	— 100,000	— —	cycles
C	Data retention[5]	t_{D_ret}	15	100	—	years

1 The frequency of this clock is controlled by a software setting.

2 These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

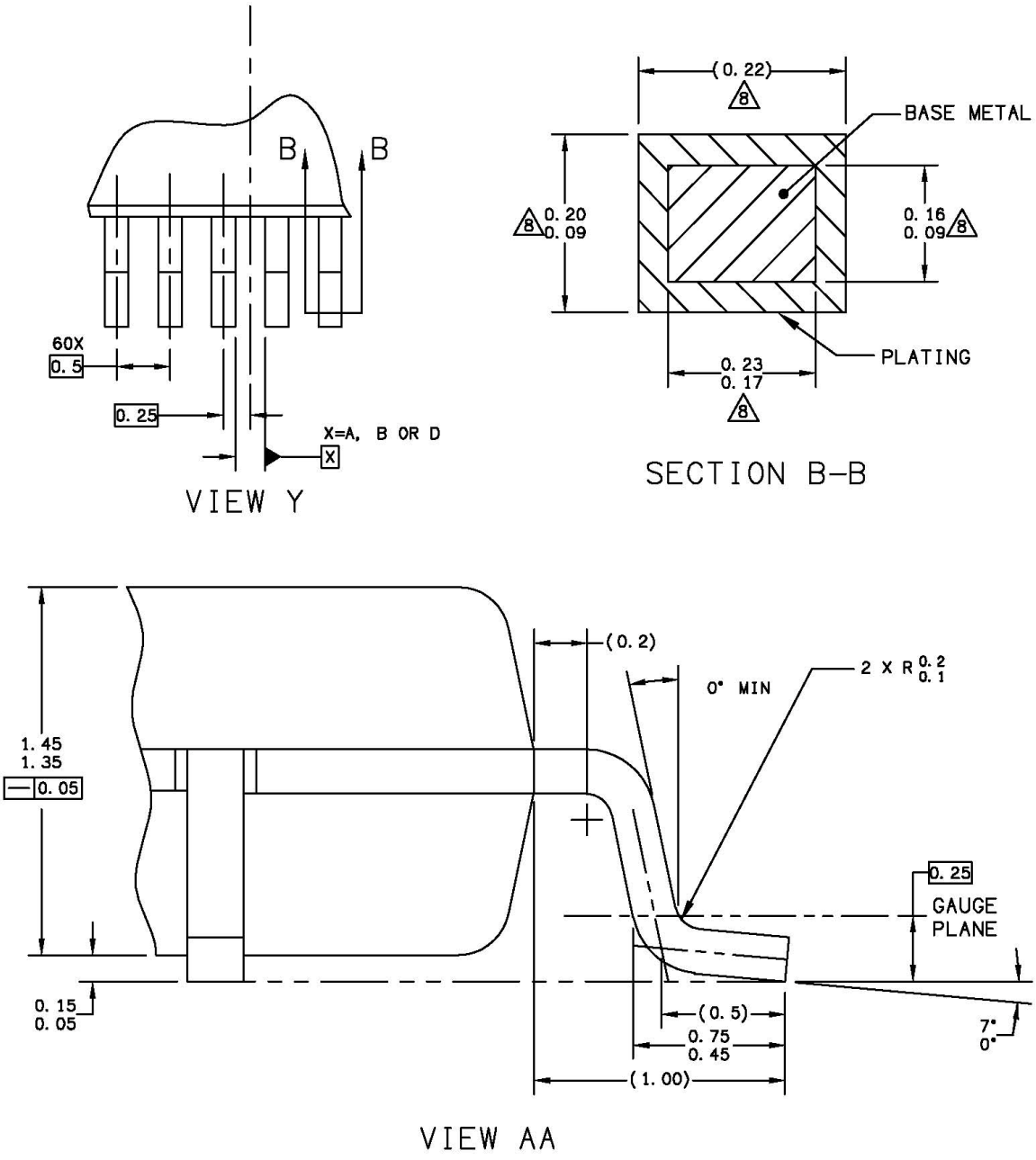
3 The program and erase currents are additional to the standard run I_{DD}. These values are measured at room temperatures with V_{DD} = 3.3 V, bus frequency = 8.0 MHz.

4 **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale defines typical endurance, please refer to Engineering Bulletin EB619, *Typical Endurance for Nonvolatile Memory.*

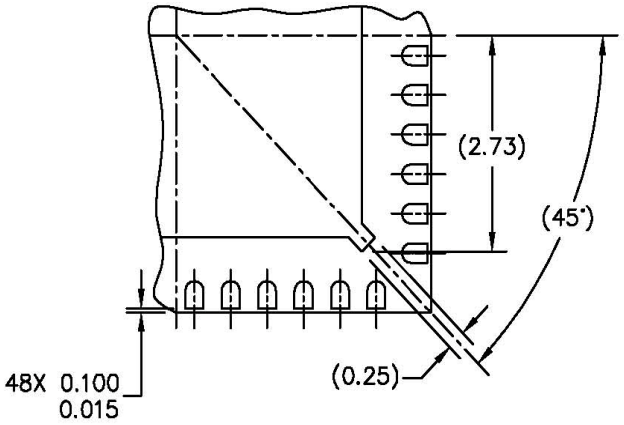
5 **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale defines typical data retention, refer to Engineering Bulletin EB618, *Typical Data Retention for Nonvolatile Memory.*

3.13 EMC Performance

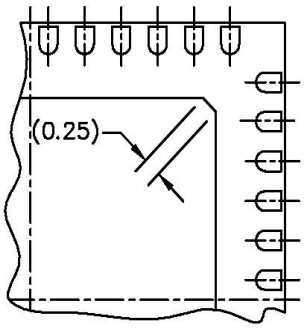
Electromagnetic compatibility (EMC) performance is highly dependent on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.



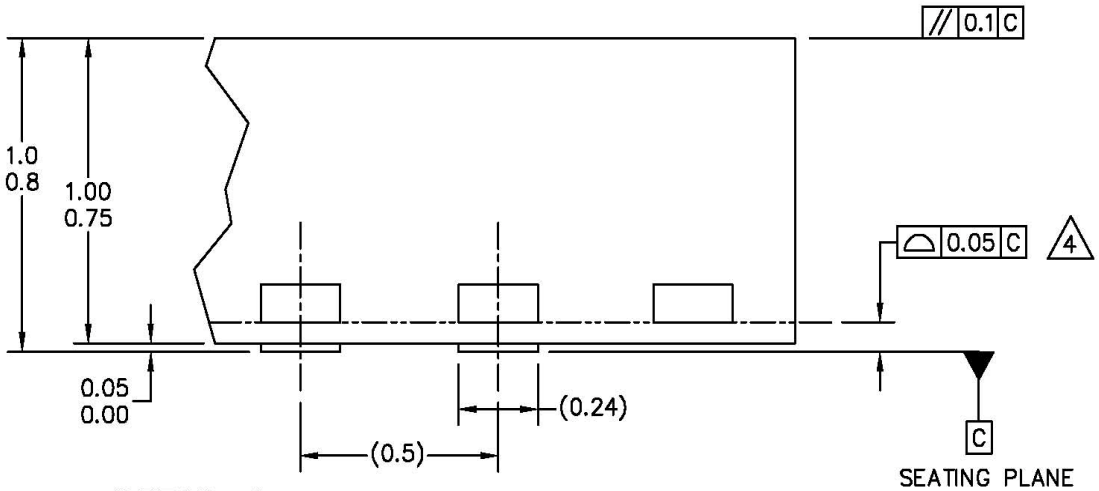
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE
TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	DOCUMENT NO: 98ASS23234W	REV: E
	CASE NUMBER: 840F-02	11 AUG 2006
	STANDARD: JEDEC MS-026 BCD	



DETAIL N
PREFERRED CORNER CONFIGURATION



DETAIL M
PREFERED PIN 1 BACKSIDE IDENTIFIER



DETAIL G
VIEW ROTATED 90° CW

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TITLE: THERMALLY ENHANCED QUAD FLAT NON-LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314-05	05 DEC 2005
	STANDARD: JEDEC-MO-220 VKKD-2	

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.
3. THE COMPLETE JEDEC DESIGNATOR FOR THIS PACKAGE IS: HF–PQFN.
4. COPLANARITY APPLIES TO LEADS, CORNER LEADS, AND DIE ATTACH PAD.
5. MIN METAL GAP SHOULD BE 0.2MM.

	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: THERMALLY ENHANCED QUAD FLAT NON–LEADED PACKAGE (QFN) 48 TERMINAL, 0.5 PITCH (7 X 7 X 1)	DOCUMENT NO: 98ARH99048A	REV: F
	CASE NUMBER: 1314–05	05 DEC 2005
	STANDARD: JEDEC–MO–220 VKKD–2	

7 Revision History

This section lists the changes between versions of MCF51CN128 Data Sheet document.

Table 25. Revision History

Revision Number	Date	Description of Changes
1	August 2008	Alpha Customer Release.
2	January 2009	Pre-Launch Release.
3	January 2009	Launch Release.
4	May 2009	• Changed LVDH trip and recovery values in Table 8. • Fixed Mini-FlexBus maximum frequency to 25.1666 MHz in Section 3.10, “Mini-FlexBus Timing Specifications.” • Updated FEC feature list to describe ethernet operation between 3.0 V to 3.6 V. • In Table 8, added a footnote to the operating voltage. It describes an exception to the Fast Ethernet Controller (FEC), because it is only operational above the operating voltage of 3 V. • Corrected Freescale part numbers in Table 23. • In Table 21, changed I_{DDAD} classification to T.