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#### What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	25MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2321-e-sp

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

### 1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

- PIC18F2221 PIC18LF2221
- PIC18F2321 PIC18LF2321
- PIC18F4221 PIC18LF4221
- PIC18F4321 PIC18LF4321

This family offers the advantages of all PIC18 microcontrollers – namely, high computational performance at an economical price – with the addition of highendurance, Enhanced Flash program memory. On top of these features, the PIC18F2221/2321/4221/4321 family introduces design enhancements that make these microcontrollers a logical choice for many high-performance, power sensitive applications.

#### 1.1 New Core Features

#### 1.1.1 nanoWatt TECHNOLOGY

All of the devices in the PIC18F2221/2321/4221/4321 family incorporate a range of features that can significantly reduce power consumption during operation. Key items include:

- Alternate Run Modes: By clocking the controller from the Timer1 source or the internal oscillator block, power consumption during code execution can be reduced by as much as 90%.
- **Multiple Idle Modes:** The controller can also run with its CPU core disabled but the peripherals still active. In these states, power consumption can be reduced even further, to as little as 4% of normal operation requirements.
- On-the-Fly Mode Switching: The power-managed modes are invoked by user code during operation, allowing the user to incorporate power-saving ideas into their application's software design.
- Low Consumption in Key Modules: The power requirements for both Timer1 and the Watchdog Timer are minimized. See Section 27.0 "Electrical Characteristics" for values.

#### 1.1.2 MULTIPLE OSCILLATOR OPTIONS AND FEATURES

All of the devices in the PIC18F2221/2321/4221/4321 family offer ten different oscillator options, allowing users a wide range of choices in developing application hardware. These include:

- Four Crystal modes, using crystals or ceramic resonators.
- Two External Clock modes, offering the option of using two pins (oscillator input and a divide-by-4 clock output) or one pin (oscillator input, with the second pin reassigned as general I/O).
- Two External RC Oscillator modes with the same pin options as the External Clock modes.
- Two Internal Oscillator modes which provide an 8 MHz clock and an INTRC source (approximately 31 kHz), as well as a range of 6 user-selectable clock frequencies, between 125 kHz to 4 MHz, for a total of 8 clock frequencies. One or both of the oscillator pins can be used for general purpose I/O.
- A Phase Lock Loop (PLL) frequency multiplier, available to both the high-speed crystal and internal oscillator modes, which allows clock speeds of up to 40 MHz. Used with the internal oscillator, the PLL gives users a complete selection of clock speeds, from 31 kHz to 32 MHz – all without using an external crystal or clock circuit.

Besides its availability as a clock source, the internal oscillator block provides a stable reference source that gives the family additional features for robust operation:

- Fail-Safe Clock Monitor: This option constantly monitors the main clock source against a reference signal provided by the internal oscillator. If a clock failure occurs, the controller is switched to the internal oscillator block, allowing for continued low-speed operation or a safe application shutdown.
- **Two-Speed Start-up:** This option allows the internal oscillator to serve as the clock source from Power-on Reset, or wake-up from Sleep mode, until the primary clock source is available.

#### 3.8 Effects of Power-Managed Modes on the Various Clock Sources

When PRI\_IDLE mode is selected, the designated primary oscillator continues to run without interruption. For all other power-managed modes, the oscillator using the OSC1 pin is disabled. The OSC1 pin (and OSC2 pin in Crystal Oscillator modes) will stop oscillating.

In secondary clock modes (SEC\_RUN and SEC\_IDLE), the Timer1 oscillator is operating and providing the device clock. The Timer1 oscillator may also run in all power-managed modes if required to clock Timer1 or Timer3.

In internal oscillator modes (RC\_RUN and RC\_IDLE), the internal oscillator block provides the device clock source. The 31 kHz INTRC output can be used directly to provide the clock and may be enabled to support various special features, regardless of the powermanaged mode (see Section 24.2 "Watchdog Timer (WDT)", Section 24.3 "Two-Speed Start-up" and Section 24.4 "Fail-Safe Clock Monitor" for more information). The INTOSC output at 8 MHz may be used directly to clock the device or may be divided down by the postscaler. The INTOSC output is disabled if the clock is provided directly from the INTRC output. The INTOSC output is also enabled for Two-Speed Start-up at 1 MHz after a Reset.

If the Sleep mode is selected, all clock sources are stopped. Since all the transistor switching currents have been stopped, Sleep mode achieves the lowest current consumption of the device (only leakage currents).

Enabling any on-chip feature that will operate during Sleep will increase the current consumed during Sleep. The INTRC is required to support WDT operation. The Timer1 oscillator may be operating to support a Real-Time Clock. Other features may be operating that do not require a device clock source (i.e., MSSP slave, PSP, INTx pins and others). Peripherals that may add significant current consumption are listed in **Section 27.2 "DC Characteristics".** 

#### 3.9 Power-up Delays

Power-up delays are controlled by two or three timers, so that no external Reset circuitry is required for most applications. The delays ensure that the device is kept in Reset until the device power supply is stable under normal circumstances and the primary clock is operating and stable. For additional information on power-up delays, see **Section 5.5 "Device Reset Timers"**.

The first timer is the Power-up Timer (PWRT) which provides a fixed delay on power-up (parameter 33, Table 27-10). It is enabled by clearing (= 0) the PWRTEN Configuration bit (CONFIG2L<0>).

#### 3.9.1 DELAYS FOR POWER-UP AND RETURN TO PRIMARY CLOCK

The second timer is the Oscillator Start-up Timer (OST), intended to delay execution until the crystal oscillator is stable (LP, XT and HS modes). The OST does this by counting 1024 oscillator cycles before allowing the oscillator to clock the device.

When the HSPLL Oscillator mode is selected, a third timer delays execution for an additional 2 ms following the HS mode OST delay, so the PLL can lock to the incoming clock frequency. At the end of these delays, the OSTS bit (OSCCON<3>) is set.

There is a delay of interval TCSD (parameter 38, Table 27-10), once execution is allowed to start, when the controller becomes ready to execute instructions. This delay runs concurrently with any other delays. This may be the only delay that occurs when any of the EC, RC or INTIO modes are used as the primary clock source.

OSC Mode	OSC1 Pin	OSC2 Pin
RC, INTIO1	Floating, external resistor pulls high	At logic low (clock/4 output)
RCIO	Floating, external resistor pulls high	Configured as PORTA, bit 6
INTIO2	Configured as PORTA, bit 7	Configured as PORTA, bit 6
ECIO	Floating, driven by external clock	Configured as PORTA, bit 6
EC	Floating, driven by external clock	At logic low (clock/4 output)
LP, XT and HS	Feedback inverter disabled at quiescent voltage level	Feedback inverter disabled at quiescent voltage level

TABLE 3-3:OSC1 AND OSC2 PIN STATES IN SLEEP MODE

**Note:** See Table 5-2 in **Section 5.0 "Reset"** for time-outs due to Sleep and MCLR Reset.

DSCFIF     CMIF		R/W-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
<ul> <li>bit 0</li> <li>SCFIF: Oscillator Fail Interrupt Flag bit</li> <li>Device oscillator failed, clock input has changed to INTOSC (must be cleared in software)</li> <li>Device clock operating</li> <li>MIF: Comparator Interrupt Flag bit</li> <li>Comparator input has changed (must be cleared in software)</li> <li>Comparator input has not changed</li> <li>nimplemented: Read as '0'</li> <li>EIF: Data EEPROM/Flash Write Operation Interrupt Flag bit</li> <li>The write operation is not complete or has not been started</li> <li>CLIF: Bus Collision Interrupt Flag bit</li> <li>A bus collision occurred (must be cleared in software)</li> <li>No bus collision occurred (must be cleared in software)</li> <li>No bus collision occurred (must be cleared in software)</li> <li>No bus collision occurred (must be cleared in software)</li> <li>A high/low-voltage Detect Interrupt Flag bit</li> <li>A high/low-voltage condition occurred; direction determined by VDIRMAG bit (HLVDCON&lt;7&gt;)</li> <li>A high/low-voltage condition has not occurred</li> <li>MR3IF: TMR3 Overflow Interrupt Flag bit</li> <li>TMR3 register overflowed (must be cleared in software)</li> <li>TMR3 register capture occurred (must be cleared in software)</li> <li>TMR3 register capture occurred (must be cleared in software)</li> <li>TMR1 register capture occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred (must be cleared in software)</li> </ul>	I	OSCFIF	CMIF	_	EEIF	BCLIF	HLVDIF	TMR3IF	CCP2IF
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<pre>MR3IF: TMR3 Overflow Interrupt Flag bit = TMR3 register overflowed (must be cleared in software) = TMR3 register did not overflow CP2IF: CCP2 Interrupt Flag bit apture mode: = A TMR1 register capture occurred (must be cleared in software) = No TMR1 register capture occurred ompare mode: = A TMR1 register compare match occurred (must be cleared in software) = No TMR1 register compare match occurred WM mode: nused in this mode. egend:</pre>		0 = A high/	low-voltage	condition ha	as not occur	red			
<ul> <li>TMR3 register overflowed (must be cleared in software)</li> <li>TMR3 register did not overflow</li> <li>CP2IF: CCP2 Interrupt Flag bit <ul> <li>apture mode:</li> <li>A TMR1 register capture occurred (must be cleared in software)</li> <li>No TMR1 register capture occurred</li> <li>ompare mode:</li> <li>A TMR1 register compare match occurred (must be cleared in software)</li> <li>No TMR1 register compare match occurred</li> <li>WM mode:</li> <li>nused in this mode.</li> </ul> </li> </ul>		TMR3IF: T	MR3 Overflo	w Interrupt	Flag bit				
<pre>CP2IF: CCP2 Interrupt Flag bit apture mode: = A TMR1 register capture occurred (must be cleared in software) = No TMR1 register capture occurred ompare mode: = A TMR1 register compare match occurred (must be cleared in software) = No TMR1 register compare match occurred WM mode: nused in this mode. egend:</pre>		<ul><li>1 = TMR3 register overflowed (must be cleared in software)</li><li>0 = TMR3 register did not overflow</li></ul>							
<ul> <li>apture mode:</li> <li>apture mode:</li> <li>A TMR1 register capture occurred (must be cleared in software)</li> <li>No TMR1 register capture occurred</li> <li>a TMR1 register compare match occurred (must be cleared in software)</li> <li>A TMR1 register compare match occurred</li> <li>WM mode:</li> <li>nused in this mode.</li> </ul>		CCP2IF: C	CP2 Interrup	ot Flag bit					
ompare mode:         = A TMR1 register compare match occurred (must be cleared in software)         = No TMR1 register compare match occurred <u>WM mode:</u> nused in this mode.		<u>Capture mode:</u> 1 = A TMR1 register capture occurred (must be cleared in software) 0 = No TMR1 register capture occurred							
WM mode: nused in this mode. egend:	<u>Compare mode:</u> 1 = A TMR1 register compare match occurred (must be cleared in software) 0 = No TMR1 register compare match occurred								
egend:		<u>PWM mode</u> Unused in t	<u>:</u> his mode.						
= Decade b = bit $N = N/mitchele bit = L = Unimensional concentration bit = (0)$	]	Legend:		\A( _ \A(	itabla bit	11 11e <sup>-</sup>		ait mode at (	0,

'1' = Bit is set

'0' = Bit is cleared

# REGISTER 10-5: PIR2: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2

-n = Value at POR

x = Bit is unknown

#### 10.5 RCON Register

The RCON register contains flag bits which are used to determine the cause of the last Reset or wake-up from Idle or Sleep modes. RCON also contains the IPEN bit which enables interrupt priorities.

The operation of the SBOREN bit and the Reset flag bits is discussed in more detail in **Section 5.1 "RCON Register**".

#### REGISTER 10-10: RCON: RESET CONTROL REGISTER

-	R/W-0	R/W-1 <sup>(1)</sup>	U-0	R/W-1	R-1	R-1	R/W-0 <sup>(2)</sup>	R/W-0	_
	IPEN	SBOREN		RI	TO	PD	POR	BOR	
	bit 7							bit 0	-

- bit 7 IPEN: Interrupt Priority Enable bit
  - 1 = Enable priority levels on interrupts
  - 0 = Disable priority levels on interrupts (PIC16XXX Compatibility mode)
- bit 6 **SBOREN:** Software BOR Enable bit<sup>(1)</sup> For details of bit operation, see Register 5-1.
- bit 5 Unimplemented: Read as '0'
- bit 4 **RI:** RESET Instruction Flag bit For details of bit operation, see Register 5-1.
- bit 3 **TO:** Watchdog Time-out Flag bit For details of bit operation, see Register 5-1.
- bit 2 **PD:** Power-down Detection Flag bit For details of bit operation, see Register 5-1.
- bit 1 **POR:** Power-on Reset Status bit<sup>(2)</sup> For details of bit operation, see Register 5-1.
- bit 0 **BOR:** Brown-out Reset Status bit For details of bit operation, see Register 5-1.
  - Note 1: If SBOREN is enabled, its Reset state is '1'; otherwise, it is '0'.
    - **2:** Actual Reset values are determined by device configuration and the nature of the device Reset. See Register 5-1 for additional information.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit,	read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

#### 11.2 PORTB, TRISB and LATB Registers

PORTB is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISB. Setting a TRISB bit (= 1) will make the corresponding PORTB pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISB bit (= 0) will make the corresponding PORTB pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register read and write the latched output value for PORTB.

CLRF	PORTB	; Initialize PORTB by ; clearing output ; data latches
CLRF	LATB	<pre>; Alternate method ; to clear output ; data latches</pre>
MOVLW	OFh	; Set RB<4:0> as
MOVWF	ADCON1	; digital I/O pins
		; (required if config bit ; PBADEN is set)
MOVLW	OCFh	; Value used to
		; initialize data
		; direction
MOVWF	TRISB	; Set RB<3:0> as inputs ; RB<5:4> as outputs ; RB<7:6> as inputs

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn <u>on all</u> the pull-ups. This is performed by clearing bit, RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Note:	On a Power-on Reset, RB<4:0> are configured as analog inputs by default and read as '0'; RB<7:5> are configured as digital inputs.
	By clearing the Configuration bit, PBADEN, RB<4:0> will alternatively be configured as digital inputs on POR.

Four of the PORTB pins (RB<7:4>) have an interrupton-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB<7:4> pin configured as an output is excluded from the interrupton-change comparison). The input pins (of RB<7:4>) are compared with the old value latched on the last read of PORTB. The "mismatch" outputs of RB<7:4> are ORed together to generate the RB Port Change Interrupt with Flag bit, RBIF (INTCON<0>).

This interrupt can wake the device from Sleep mode or any of the Idle modes. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB (except with the MOVFF (ANY), PORTB instruction).
- b) 1 Tcy.
- c) Clear flag bit, RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB and waiting 1 Tcy will end the mismatch condition and allow flag bit, RBIF, to be cleared. Also, if the port pin returns to its original state, the mismatch condition will be cleared.

The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

RB3 can be configured by the Configuration bit, CCP2MX, as the alternate peripheral pin for the CCP2 module (CCP2MX = 0).

#### 14.2 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (TMR2 to PR2 match) provides the input for the 4-bit output counter/postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF (PIR1<1>). The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE (PIE1<1>).

A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscaler control bits, T2OUTPS<3:0> (T2CON<6:3>).

#### 14.3 Timer2 Output

The unscaled output of TMR2 is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSP module operating in SPI mode. Additional information is provided in Section 18.0 "Master Synchronous Serial Port (MSSP) Module".



### FIGURE 14-1: TIMER2 BLOCK DIAGRAM

#### TABLE 14-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	58
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	58
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	58
TMR2	Timer2 Register						56		
T2CON	- T2OUTPS3 T2OUTPS2 T2OUTPS1 T2OUTPS0 TMR2ON T2CKPS1 T2CKPS0						56		
PR2	Timer2 Period Register								56

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

Note 1: These bits are unimplemented on 28-pin devices and read as '0'.

#### 16.4 PWM Mode

In Pulse-Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP2 pin is multiplexed with a PORTB or PORTC data latch, the appropriate TRIS bit must be cleared to make the CCP2 pin an output.

Note:	Clearing the CCP2CON register will force
	the RB3 or RC1 output latch (depending on
	device configuration) to the default low
	level. This is not the PORTB or PORTC I/O
	data latch.

Figure 16-3 shows a simplified block diagram of the CCP module in PWM mode.

For a step-by-step procedure on how to set up the CCP module for PWM operation, see **Section 16.4.4** "Setup for PWM Operation".





A PWM output (Figure 16-4) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).





#### 16.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

#### EQUATION 16-1:

 $PWM Period = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (TMR2 Prescale Value)$ 

PWM frequency is defined as 1/[PWM period].

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set (exception: if PWM duty cycle = 0%, the CCPx pin will not be set)
- The PWM duty cycle is latched from CCPRxL into CCPRxH



#### 16.4.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPRxL register and to the CCPxCON<5:4> bits. Up to 10-bit resolution is available. The CCPRxL contains the eight MSbs and the CCPxCON<5:4> contains the two LSbs. This 10-bit value is represented by CCPRxL:CCPxCON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

#### **EQUATION 16-2:**

```
PWM Duty Cycle = (CCPRxL:CCPxCON<5:4>) •
Tosc • (TMR2 Prescale Value)
```

CCPRxL and CCPxCON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPRxH until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPRxH is a read-only register.



#### 19.4.2 EUSART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of Sleep, or any Idle mode and bit SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting the CREN bit prior to entering Sleep or any Idle mode, then a word may be received while in this low-power mode. Once the word is received, the RSR register will transfer the data to the RCREG register; if the RCIE enable bit is set, the interrupt generated will wake the chip from the lowpower mode. If the global interrupt is enabled, the program will branch to the interrupt vector. To set up a Synchronous Slave Reception:

- Enable the synchronous master serial port by setting bits, SYNC and SPEN, and clearing bit, CSRC.
- 2. If interrupts are desired, set enable bit RCIE.
- 3. If the signal from the CK pin is to be inverted, set the TXCKP bit.
- 4. If 9-bit reception is desired, set bit, RX9.
- 5. To enable reception, set enable bit, CREN.
- Flag bit, RCIF, will be set when reception is complete. An interrupt will be generated if enable bit, RCIE, was set.
- 7. Read the RCSTA register to get the 9th bit (if enabled) and determine if any error occurred during reception.
- 8. Read the 8-bit received data by reading the RCREG register.
- 9. If any error occurred, clear the error by clearing bit, CREN.
- 10. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	58
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	58
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	58
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	57
RCREG	EUSART F	Receive Regi	ster						57
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	57
BAUDCON	ABDOVF	RCIDL	RXDTP	TXCKP	BRG16	—	WUE	ABDEN	57
SPBRGH	EUSART Baud Rate Generator Register High Byte							57	
SPBRG	EUSART E	Baud Rate G	enerator Re	gister Low I	Byte				57

#### TABLE 19-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Legend: — = unimplemented, read as '0'. Shaded cells are not used for synchronous slave reception.

Note 1: These bits are unimplemented on 28-pin devices and read as '0'.

#### 20.4 Operation in Power-Managed Modes

The selection of the automatic acquisition time and A/D conversion clock is determined in part by the clock source and frequency while in a power-managed mode.

If the A/D is expected to operate while the device is in a power-managed mode, the ACQT<2:0> and ADCS<2:0> bits in ADCON2 should be updated in accordance with the clock source to be used in that mode. After entering the mode, an A/D acquisition or conversion may be started. Once started, the device should continue to be clocked by the same clock source until the conversion has been completed.

If desired, the device may be placed into the corresponding Idle mode during the conversion. If the device clock frequency is less than 1 MHz, the A/D RC clock source should be selected.

Operation in Sleep mode requires the A/D FRC clock to be selected. If bits ACQT<2:0> are set to '000' and a conversion is started, the conversion will be delayed one instruction cycle to allow execution of the SLEEP instruction and entry to Sleep mode. The IDLEN bit (OSCCON<7>) must have already been cleared prior to starting the conversion.

### 20.5 Configuring Analog Port Pins

The ADCON1, TRISA, TRISB and TRISE registers all configure the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS<3:0> bits and the TRIS bits.

- Note 1: When reading the Port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert as analog inputs. Analog levels on a digitally configured input will be accurately converted.
  - 2: Analog levels on any pin defined as a digital input may cause the digital input buffer to consume current out of the device's specification limits.
  - 3: The PBADEN bit in Configuration Register 3H configures PORTB pins to reset as analog or digital pins by controlling how the PCFG<3:0> bits in ADCON1 are reset.

### 23.1 Operation

When the HLVD module is enabled, a comparator uses an internally generated reference voltage as the set point. The set point is compared with the trip point, where each node in the resistor divider represents a trip point voltage. The "trip point" voltage is the voltage level at which the device detects a high or low-voltage event, depending on the configuration of the module. When the supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal by setting the HLVDIF bit. The trip point voltage is software programmable to any one of 16 values. The trip point is selected by programming the HLVDL<3:0> bits (HLVDCON<3:0>).

The HLVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits HLVDL<3:0> are set to '1111'. In this state, the comparator input is multiplexed from the external input pin, HLVDIN. This gives users flexibility because it allows them to configure the High/Low-Voltage Detect interrupt to occur at any voltage in the valid operating range.





#### REGISTER 24-3: CONFIG2H: CONFIGURATION REGISTER 2 HIGH (BYTE ADDRESS 300003h) R/P-1 R/P-1 U-0 U-0 U-0 R/P-1 R/P-1 R/P-1 WDTPS0 WDTEN WDTPS3 WDTPS2 WDTPS1 bit 7 bit 0

- bit 7-5 Unimplemented: Read as '0'
- bit 4-1 WDTPS<3:0>: Watchdog Timer Postscale Select bits

1111	=	1:32,768
1110	=	1:16,384
1101	=	1:8,192
1100	=	1:4,096
1011	=	1:2,048
1010	=	1:1,024
1001	=	1:512
1000	=	1:256
0111	=	1:128
0110	=	1:64
0101	=	1:32
0100	=	1:16
0011	=	1:8
0010	=	1:4
0001	=	1:2
0000	=	1:1
		I. Wotobd

- bit 0 WDTEN: Watchdog Timer Enable bit
  - 1 = WDT enabled
  - 0 = WDT disabled (control is placed on the SWDTEN bit)

Legend:		
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed		u = Unchanged from programmed state



#### 24.4.3 FSCM INTERRUPTS IN POWER-MANAGED MODES

By entering a power-managed mode, the clock multiplexer selects the clock source selected by the OSCCON register. Fail-Safe Monitoring of the powermanaged clock source resumes in the power-managed mode.

If an oscillator failure occurs during power-managed operation, the subsequent events depend on whether or not the oscillator failure interrupt is enabled. If enabled (OSCFIF = 1), code execution will be clocked by the INTOSC multiplexer. An automatic transition back to the failed clock source will not occur.

If the interrupt is disabled, subsequent interrupts while in Idle mode will cause the CPU to begin executing instructions while being clocked by the INTOSC source.

#### 24.4.4 POR OR WAKE FROM SLEEP

The FSCM is designed to detect oscillator failure at any point after the device has exited Power-on Reset (POR) or low-power Sleep mode. When the primary device clock is EC, RC or INTRC modes, monitoring can begin immediately following these events.

For oscillator modes involving a crystal or resonator (HS, HSPLL, LP or XT), the situation is somewhat different. Since the oscillator may require a start-up time considerably longer than the FCSM sample clock time, a false clock failure may be detected. To prevent this, the internal oscillator block is automatically configured as the device clock and functions until the primary clock is stable (the OST and PLL timers have timed out). This is identical to Two-Speed Start-up mode. Once the primary clock is stable, the INTRC returns to its role as the FSCM source.

Note:	The same logic that prevents false oscilla- tor failure interrupts on POR or wake from	
	Sloop will also provent the detection of	
	Sleep, will also prevent the detection of	
	the oscillator's failure to start at all follow-	
	ing these events. This can be avoided by	
	monitoring the OSTS bit and using a	
	timing routine to determine if the oscillator	
	is taking too long to start. Even so, no	
	oscillator failure interrupt will be flagged.	

As noted in Section 24.3.1 "Special Considerations for Using Two-Speed Start-up", it is also possible to select another clock configuration and enter an alternate power-managed mode while waiting for the primary clock to become stable. When the new powermanaged mode is selected, the primary clock is disabled.

#### 24.5.2 DATA EEPROM CODE PROTECTION

The entire data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of data EEPROM. WRTD inhibits internal and external writes to data EEPROM. The CPU can always read data EEPROM under normal operation, regardless of the protection bit settings.

#### 24.5.3 CONFIGURATION REGISTER PROTECTION

The Configuration registers can be write-protected. The WRTC bit controls protection of the Configuration registers. In normal execution mode, the WRTC bit is readable only. WRTC can only be written via ICSP operation or an external programmer.

### 24.6 ID Locations

Eight memory locations (20000h-200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are both readable and writable during normal execution through the TBLRD and TBLWT instructions or during program/verify. The ID locations can be read when the device is code-protected.

# 24.7 In-Circuit Serial Programming

PIC18F2221/2321/4221/4321 family microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

# 24.8 In-Circuit Debugger

When the DEBUG Configuration bit is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB<sup>®</sup> IDE. When the microcontroller has this feature enabled, some resources are not available for general use. Table 24-4 shows which resources are required by the background debugger.

TABI F 24-4·	DEBUGGER RESOURCES

I/O Pins:	RB6, RB7
Stack:	2 levels
Program Memory:	512 bytes
Data Memory:	10 bytes

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP/RE3, VDD, Vss, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

### 24.9 Single-Supply ICSP Programming

The LVP Configuration bit enables Single-Supply ICSP Programming (formerly known as *Low-Voltage ICSP Programming* or *LVP*). When Single-Supply Programming is enabled, the microcontroller can be programmed <u>without</u> requiring high voltage being applied to the MCLR/VPP/RE3 pin, but the RB5/KBI1/PGM pin is then dedicated to controlling Program mode entry and is not available as a general purpose I/O pin.

While programming, using <u>Single-Supply Programming</u>, VDD is applied to the MCLR/VPP/RE3 pin as in normal execution mode. To enter Programming mode, VDD is applied to the PGM pin.

- Note 1: High-voltage programming is always available, regardless of the state of the LVP bit or the PGM pin, by applying VIнн to the MCLR pin.
  - 2: By default, Single-Supply ICSP Programming is enabled in unprogrammed devices (as supplied from Microchip) and erased devices.
  - When Single-Supply ICSP Programming is enabled, the RB5 pin can no longer be used as a general purpose I/O pin.
  - 4: When LVP is enabled, externally pull the PGM pin to Vss to allow normal program execution.

If Single-Supply ICSP Programming mode will not be used, the LVP bit can be cleared. RB5/KBI1/PGM then becomes available as the digital I/O pin, RB5. The LVP bit may be set or cleared only when using standard high-voltage programming (VIHH applied to the MCLR/ VPP/RE3 pin). Once LVP has been disabled, only the standard high-voltage programming is available and must be used to program the device.

Memory that is not code-protected can be erased using either a block erase, or erased row by row, then written at any specified VDD. If code-protected memory is to be erased, a block erase is required. If a block erase is to be performed when using Low-Voltage ICSP Programming, the device must be supplied with VDD of 4.5V to 5.5V.

RETURN Return from			om Sub	routine		
Synta	Syntax: RETURN {s}					
Oper	ands:	<b>S</b> ∈ [0,1]				
Oper	ation:	$(TOS) \rightarrow PC;$ if s = 1, $(WS) \rightarrow W,$ $(STATUSS) \rightarrow STATUS,$ $(BSRS) \rightarrow BSR,$ PCLATU, PCLATH are unchanged				
Statu	s Affected:	None				
Enco	oding:	0000	0000	0001	001s	
Description: Return from subroutine. The stack popped and the top of the stack (' is loaded into the program counte 's'= 1, the contents of the shadow registers, WS, STATUSS and BSI are loaded into their correspondin registers, W, STATUS and BSR. I 's' = 0, no update of these registe occurs (default)			stack is ack (TOS) punter. If adow I BSRS, onding SR. If gisters			
Words:		1	1			
Cycles:		2	2			
Q Cvcle Activity:						
	Q1	Q2	Q	3	Q4	
	Decode	No	Proce	ess	POP PC	
		operation	Dat	a fi	rom stack	
	No	No	No	)	No	
	operation	operation	opera	tion o	operation	
Example:		RETURN				

Examp	ole:

After Instruction: PC = TOS

RLCF	Rotate Left f through Carry		
Syntax:	RLCF f	{,d {,a}}	
Operands:	0≤f≤255 d∈[0,1] a∈[0,1]		
Operation:	$(f < n >) \rightarrow dr$ $(f < 7 >) \rightarrow C$ $(C) \rightarrow dest$	est <n +="" 1="">, ; &lt;0&gt;</n>	
Status Affected:	C, N, Z		
Encoding:	0011	01da fff	f ffff
Description:	The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details.		f' are rotated the Carry is placed in a stored back nk is SR is used to ault). ed instruction ction al Offset ver 25.2.3 Driented _iteral Offset
Words:	1		
Cycles:	1		
O Cuelo Activitur	I		
	02	03	04
Decode	Read	Process	Write to
	register 'f'	Data	destination
Example: Before Instruc REG C After Instructic	RLCF tion = 1110 0 = 0	REG, 0,	0
REG W	= 1110 0 = 1100 1	110	

### 27.4 AC (Timing) Characteristics

#### 27.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS		3. Tcc:st	(I <sup>2</sup> C specifications only)
2. TppS		4. Ts	(I <sup>2</sup> C specifications only)
Т			
F	Frequency	Т	Time
Lowercase le	tters (pp) and their meanings:		
рр			
сс	CCP1	osc	OSC1
ck	CLKO	rd	RD
cs	CS	rw	RD or WR
di	SDI	sc	SCK
do	SDO	SS	SS
dt	Data in	tO	TOCKI
io	I/O port	t1	T13CKI
mc	MCLR	wr	WR
Uppercase le	tters and their meanings:		
S			
F	Fall	Р	Period
н	High	R	Rise
1	Invalid (High-impedance)	V	Valid
L	Low	Z	High-impedance
I <sup>2</sup> C only			
AA	output access	High	High
BUF	Bus free	Low	Low
TCC:ST (I <sup>2</sup> C s	pecifications only)		
CC			
HD	Hold	SU	Setup
ST			
DAT	DATA input hold	STO	Stop condition
STA	Start condition		

NOTES:

### 44-Lead Plastic Quad Flat, No Lead Package (ML) – 8x8 mm Body [QFN]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging







Units		MILLIMETERS		
Dimension	n Limits	MIN	NOM	MAX
Number of Pins	Ν		44	
Pitch	е	0.65 BSC		
Overall Height	Α	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3	0.20 REF		
Overall Width	Е		8.00 BSC	
Exposed Pad Width	E2	6.30	6.45	6.80
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.30	6.45	6.80
Contact Width	b	0.25	0.30	0.38
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	_	_

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103B

### 44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



**RECOMMENDED LAND PATTERN** 

Units		MILLIM	ETERS	-
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.80 BSC	
Contact Pad Spacing	C1		11.40	
Contact Pad Spacing	C2		11.40	
Contact Pad Width (X44)	X1			0.55
Contact Pad Length (X44)	Y1			1.50
Distance Between Pads	G	0.25		

#### Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2076A

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