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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2321-i-ml



MICROCHIP PIC18F2221/2321/4221/4321 FAMILY

28/40/44-Pin Enhanced Flash Microcontrollers with 10-Bit A/D and nanoWatt Technology

Power-Managed Modes:

- Run: CPU On, Peripherals On
- Idle: CPU Off, Peripherals On
- Sleep: CPU Off, Peripherals Off
- Idle mode Currents Down to 2.5 μ A Typical
- Sleep mode Currents Down to 500 nA Typical
- Timer1 Oscillator: 1.8 μ A, 32 kHz, 2V Typical
- Watchdog Timer: 1.6 μ A, 2V Typical
- Two-Speed Oscillator Start-up

Flexible Oscillator Structure:

- Four Crystal modes, up to 40 MHz
- 4x Phase Lock Loop (PLL) – Available for Crystal and Internal Oscillators
- Two External RC modes, up to 4 MHz
- Two External Clock modes, up to 40 MHz
- Internal Oscillator Block:
 - 8 user-selectable frequencies, from 31 kHz to 8 MHz
 - Provides a complete range of clock speeds from 31 kHz to 32 MHz when used with PLL
 - User-tunable to compensate for frequency drift
- Secondary Oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor
 - Allows for safe shutdown if peripheral clock stops

Peripheral Highlights:

- High-Current Sink/Source 25 mA/25 mA
- Three Programmable External Interrupts
- Four Input Change Interrupts
- Up to 2 Capture/Compare/PWM (CCP) modules, one with Auto-Shutdown (28-pin devices)
- Enhanced Capture/Compare/PWM (ECCP) module (40/44-pin devices only):
 - One, two or four PWM outputs
 - Selectable polarity
 - Programmable dead time
 - Auto-shutdown and auto-restart

Peripheral Highlights (Continued):

- Master Synchronous Serial Port (MSSP) module Supporting 3-Wire SPI (all 4 modes) and I²C™ Master and Slave modes
- Enhanced Addressable USART module:
 - Supports RS-485, RS-232 and LIN/J2602
 - Auto-wake-up on Start bit
 - Auto-Baud Detect
- 10-Bit, up to 13-Channel Analog-to-Digital Converter module (A/D):
 - Auto-acquisition capability
 - Conversion available during Sleep
- Dual Analog Comparators with Input Multiplexing
- Programmable 16-Level High/Low-Voltage Detection (HLVD) module:
 - Supports interrupt on High/Low-Voltage Detection

Special Microcontroller Features:

- C Compiler Optimized Architecture:
 - Optional extended instruction set designed to optimize re-entrant code
- 100,000 Erase/Write Cycle Enhanced Flash Program Memory Typical
- 1,000,000 Erase/Write Cycle Data EEPROM Memory Typical
- Flash/Data EEPROM Retention: 100 Years Typical
- Self-Programmable under Software Control
- Priority Levels for Interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
 - Programmable period from 4 ms to 131s
- Single-Supply 5V In-Circuit Serial Programming™ (ICSP™) via Two Pins
- In-Circuit Debug (ICD) via Two Pins
- Wide Operating Voltage Range: 2.0V to 5.5V
- Programmable Brown-out Reset (BOR) with Software Enable Option)

Device	Program Memory		Data Memory		I/O	10-Bit A/D (ch)	CCP/ ECCP (PWM)	MSSP		EUSART	Comp.	Timers 8/16-Bit
	Flash (bytes)	# Single-Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I ² C™			
PIC18F2221	4K	2048	512	256	25	10	2/0	Y	Y	1	2	1/3
PIC18F2321	8K	4096	512	256	25	10	2/0	Y	Y	1	2	1/3
PIC18F4221	4K	2048	512	256	36	13	1/1	Y	Y	1	2	1/3
PIC18F4321	8K	4096	512	256	36	13	1/1	Y	Y	1	2	1/3

PIC18F2221/2321/4221/4321 FAMILY

2.4 ICSP Pins

The PGC and PGD pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGC and PGD pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high (V_{IH}) and input low (V_{IL}) requirements.

For device emulation, ensure that the “Communication Channel Select” (i.e., PGC/PGD pins) programmed into the device matches the physical connections for the ICSP to the MPLAB® ICD 2, MPLAB ICD 3 or REAL ICE™ emulator.

For more information on the ICD 2, ICD 3 and REAL ICE emulator connection requirements, refer to the following documents that are available on the Microchip web site.

- “MPLAB® ICD 2 In-Circuit Debugger User’s Guide” (DS51331)
- “Using MPLAB® ICD 2” (poster) (DS51265)
- “MPLAB® ICD 2 Design Advisory” (DS51566)
- “Using MPLAB® ICD 3” (poster) (DS51765)
- “MPLAB® ICD 3 Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™ In-Circuit Emulator” (poster) (DS51749)

2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 3.0 “Oscillator Configurations”** for details).

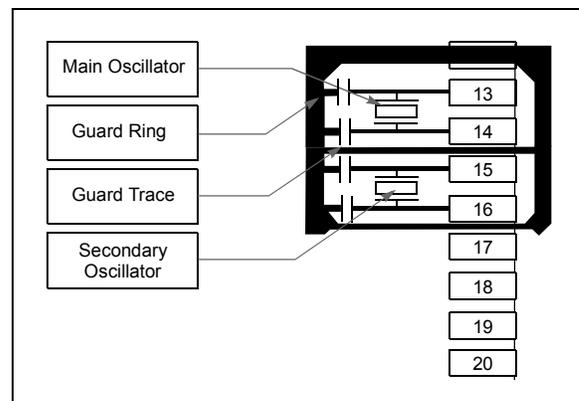
The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site (www.microchip.com):

- AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices”
- AN849, “Basic PICmicro® Oscillator Design”
- AN943, “Practical PICmicro® Oscillator Analysis and Design”
- AN949, “Making Your Oscillator Work”

FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT



2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

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TABLE 5-4: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices				Power-on Reset, Brown-out Reset	MCLR Resets, WDT Reset, RESET Instruction, Stack Resets	Wake-up via WDT or Interrupt
FSR1H	2221	2321	4221	4321	---- 0000	---- 0000	---- uuuu
FSR1L	2221	2321	4221	4321	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	2221	2321	4221	4321	---- 0000	---- 0000	---- uuuu
INDF2	2221	2321	4221	4321	N/A	N/A	N/A
POSTINC2	2221	2321	4221	4321	N/A	N/A	N/A
POSTDEC2	2221	2321	4221	4321	N/A	N/A	N/A
PREINC2	2221	2321	4221	4321	N/A	N/A	N/A
PLUSW2	2221	2321	4221	4321	N/A	N/A	N/A
FSR2H	2221	2321	4221	4321	---- 0000	---- 0000	---- uuuu
FSR2L	2221	2321	4221	4321	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	2221	2321	4221	4321	---x xxxx	---u uuuu	---u uuuu
TMR0H	2221	2321	4221	4321	0000 0000	0000 0000	uuuu uuuu
TMR0L	2221	2321	4221	4321	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	2221	2321	4221	4321	1111 1111	1111 1111	uuuu uuuu
OSCCON	2221	2321	4221	4321	0100 q000	0100 q000	uuuu uuqu
HLVDCON	2221	2321	4221	4321	0-00 0101	0-00 0101	u-uu uuuu
WDTCON	2221	2321	4221	4321	---- ---0	---- ---0	---- ---u
RCON ⁽⁴⁾	2221	2321	4221	4321	0q-1 11q0	0q-q qquu	uq-u qquu
TMR1H	2221	2321	4221	4321	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	2221	2321	4221	4321	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	2221	2321	4221	4321	0000 0000	u0uu uuuu	uuuu uuuu
TMR2	2221	2321	4221	4321	0000 0000	0000 0000	uuuu uuuu
PR2	2221	2321	4221	4321	1111 1111	1111 1111	1111 1111
T2CON	2221	2321	4221	4321	-000 0000	-000 0000	-uuu uuuu
SSPBUF	2221	2321	4221	4321	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	2221	2321	4221	4321	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	2221	2321	4221	4321	0000 0000	0000 0000	uuuu uuuu
SSPCON1	2221	2321	4221	4321	0000 0000	0000 0000	uuuu uuuu
SSPCON2	2221	2321	4221	4321	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.
Shaded cells indicate conditions do not apply for the designated device.

- Note 1:** One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
- 2:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
- 3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
- 4:** See Table 5-3 for Reset value for specific condition.
- 5:** Bits 6 and 7 of PORTA, LATA and TRISA are enabled, depending on the oscillator mode selected. When not enabled as PORTA pins, they are disabled and read '0'.

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6.0 MEMORY ORGANIZATION

There are three types of memory in PIC18 Enhanced microcontroller devices:

- Program Memory
- Data RAM
- Data EEPROM

As Harvard architecture devices, the data and program memories use separate busses; this allows for concurrent access of the two memory spaces. The data EEPROM, for practical purposes, can be regarded as a peripheral device, since it is addressed and accessed through a set of control registers.

Additional detailed information on the operation of the Flash program memory is provided in **Section 7.0 “Flash Program Memory”**. Data EEPROM is discussed separately in **Section 8.0 “Data EEPROM Memory”**.

6.1 Program Memory Organization

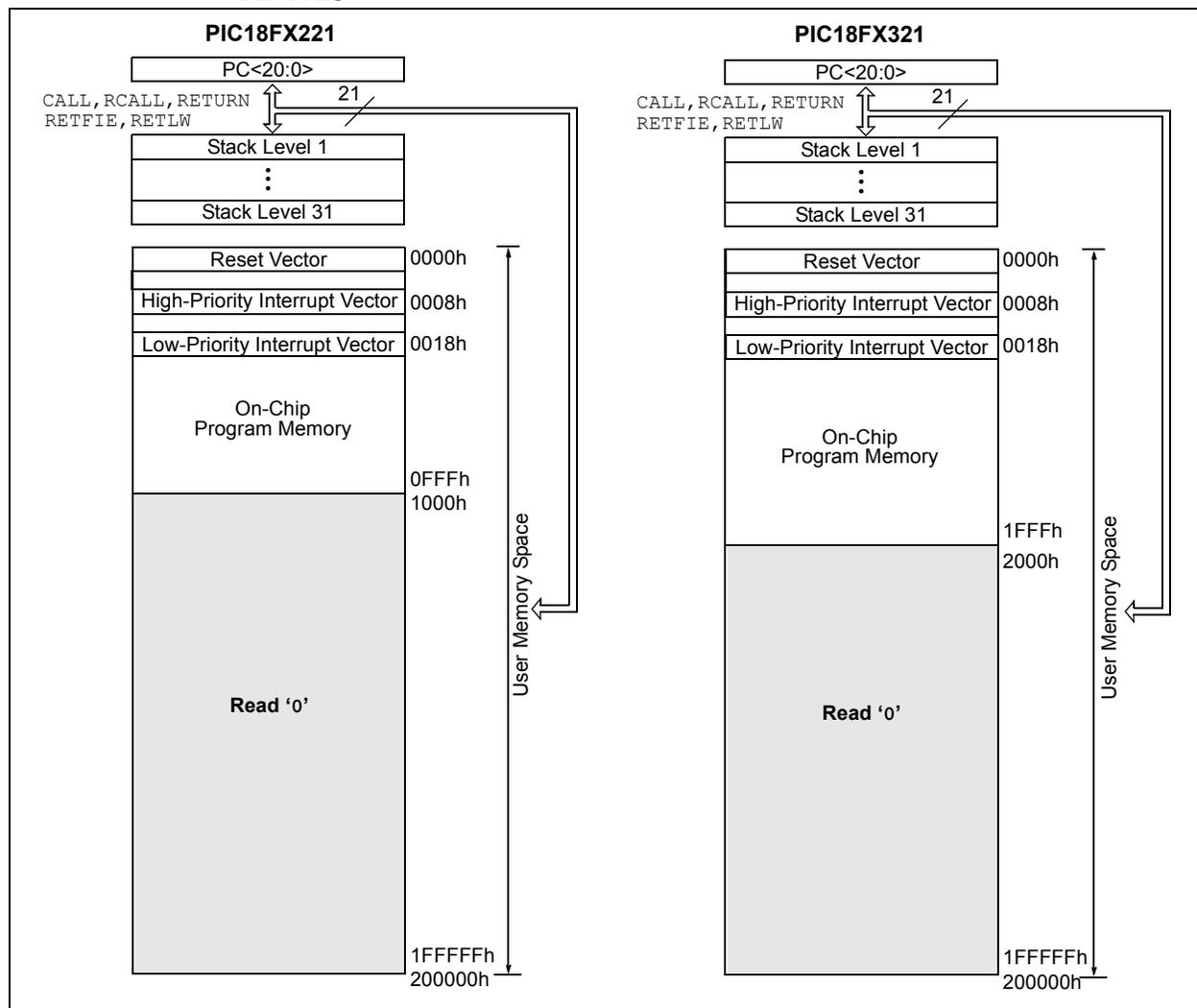
PIC18 microcontrollers implement a 21-bit program counter, which is capable of addressing a 2-Mbyte program memory space. Accessing a location between the upper boundary of the physically implemented memory and the 2-Mbyte address will return all ‘0’s (a NOP instruction).

The PIC18F2221 and PIC18F4221 each have 4 Kbytes of Flash memory and can store up to 2048 single-word instructions. The PIC18F2321 and PIC18F4321 each have 8 Kbytes of Flash memory and can store up to 4096 single-word instructions.

PIC18 devices have two interrupt vectors. The Reset vector address is at 0000h and the interrupt vector addresses are at 0008h and 0018h.

The program memory maps for PIC18F2221/4221 and PIC18F2321/4321 devices are shown in Figure 6-1.

FIGURE 6-1: PROGRAM MEMORY MAP AND STACK FOR PIC18F2221/2321/4221/4321 FAMILY DEVICES



PIC18F2221/2321/4221/4321 FAMILY

REGISTER 7-1: EECON1: DATA EEPROM CONTROL REGISTER 1

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD
bit 7						bit 0	

- bit 7 **EEPGD:** Flash Program or Data EEPROM Memory Select bit
 1 = Access Flash program memory
 0 = Access data EEPROM memory
- bit 6 **CFGS:** Flash Program/Data EEPROM or Configuration Select bit
 1 = Access Configuration registers
 0 = Access Flash program or data EEPROM memory
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **FREE:** Flash Row Erase Enable bit
 1 = Erase the program memory row addressed by TBLPTR on the next WR command
 (cleared by completion of erase operation)
 0 = Perform write-only
- bit 3 **WRERR:** Flash Program/Data EEPROM Error Flag bit
 1 = A write operation is prematurely terminated (any Reset during self-timed programming in normal operation, or an improper write attempt)
 0 = The write operation completed
Note: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.
- bit 2 **WREN:** Flash Program/Data EEPROM Write Enable bit
 1 = Allows write cycles to Flash program/data EEPROM
 0 = Inhibits write cycles to Flash program/data EEPROM
- bit 1 **WR:** Write Control bit
 1 = Initiates a data EEPROM erase/write cycle or a program memory erase/write cycle.
 (The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
 0 = Write cycle to the EEPROM is complete
- bit 0 **RD:** Read Control bit
 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)
 0 = Does not initiate an EEPROM read

Legend:

R = Readable bit	W = Writable bit
S = Bit can be set by software, but not cleared	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set '0' = Bit is cleared x = Bit is unknown

PIC18F2221/2321/4221/4321 FAMILY

10.6 INTx Pin Interrupts

External interrupts on the RB0/INT0, RB1/INT1 and RB2/INT2 pins are edge-triggered. If the corresponding INTEDGx bit in the INTCON2 register is set (= 1), the interrupt is triggered by a rising edge; if the bit is clear, the trigger is on the falling edge. When a valid edge appears on the RBx/INTx pin, the corresponding flag bit, INTxF, is set. This interrupt can be disabled by clearing the corresponding enable bit, INTxE. Flag bit, INTxF, must be cleared in software in the Interrupt Service Routine before re-enabling the interrupt.

All external interrupts (INT0, INT1 and INT2) can wake-up the processor from Idle or Sleep modes if bit INTxE was set prior to going into those modes. If the Global Interrupt Enable bit, GIE, is set, the processor will branch to the interrupt vector following wake-up.

Interrupt priority for INT1 and INT2 is determined by the value contained in the interrupt priority bits, INT1IP (INTCON3<6>) and INT2IP (INTCON3<7>). There is no priority bit associated with INT0. It is always a high-priority interrupt source.

10.7 TMR0 Interrupt

In 8-bit mode (which is the default), an overflow in the TMR0 register (FFh → 00h) will set flag bit, TMR0IF. In 16-bit mode, an overflow in the TMR0H:TMR0L register pair (FFFFh → 0000h) will set TMR0IF. The interrupt can be enabled/disabled by setting/clearing enable bit, TMR0IE (INTCON<5>). Interrupt priority for Timer0 is determined by the value contained in the interrupt priority bit, TMR0IP (INTCON2<2>). See **Section 12.0 “Timer0 Module”** for further details on the Timer0 module.

10.8 PORTB Interrupt-on-Change

An input change on PORTB<7:4> sets flag bit, RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit, RBIE (INTCON<3>). Interrupt priority for PORTB interrupt-on-change is determined by the value contained in the interrupt priority bit, RBIP (INTCON2<0>).

10.9 Context Saving During Interrupts

During interrupts, the return PC address is saved on the stack. Additionally, the WREG, STATUS and BSR registers are saved on the fast return stack. If a fast return from interrupt is not used (see **Section 6.3 “Data Memory Organization”**), the user may need to save the WREG, STATUS and BSR registers on entry to the Interrupt Service Routine. Depending on the user’s application, other registers may also need to be saved. Example 10-1 saves and restores the WREG, STATUS and BSR registers during an Interrupt Service Routine.

EXAMPLE 10-1: SAVING STATUS, WREG AND BSR REGISTERS IN RAM

```
MOVWF    W_TEMP                ; W_TEMP is in virtual bank
MOVFF    STATUS, STATUS_TEMP    ; STATUS_TEMP located anywhere
MOVFF    BSR, BSR_TEMP          ; BSR_TEMP located anywhere
;
; USER ISR CODE
;
MOVFF    BSR_TEMP, BSR          ; Restore BSR
MOVF     W_TEMP, W              ; Restore WREG
MOVFF    STATUS_TEMP, STATUS    ; Restore STATUS
```

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11.0 I/O PORTS

Depending on the device selected and features enabled, there are up to five ports available. Some pins of the I/O ports are multiplexed with an alternate function from the peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

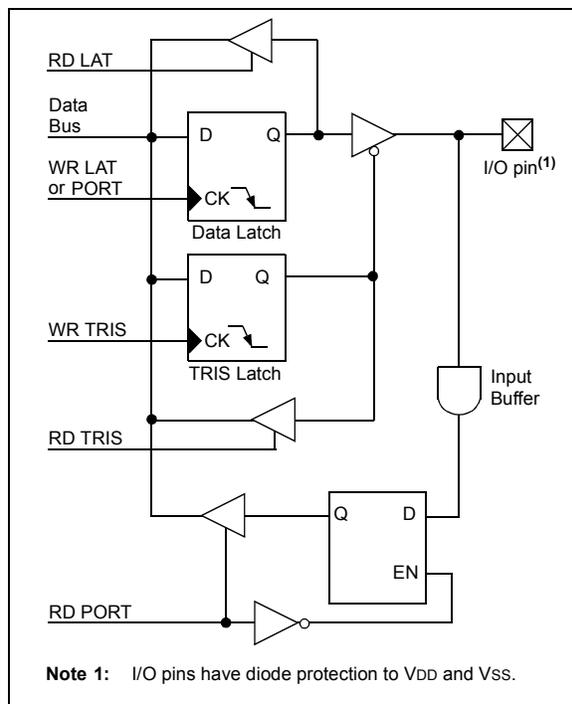
Each port has three registers for its operation. These registers are:

- TRIS register (Data Direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (Data Latch register)

The Data Latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 11-1.

FIGURE 11-1: GENERIC I/O PORT OPERATION



11.1 PORTA, TRISA and LATA Registers

PORTA is an 8-bit wide, bidirectional port. The corresponding Data Direction register is TRISA. Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a High-Impedance mode). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it, will write to the port latch.

The Data Latch (LATA) register is also memory mapped. Read-modify-write operations on the LATA register read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input and one of the comparator outputs to become the RA4/T0CKI/C1OUT pin. Pins RA6 and RA7 are multiplexed with the main oscillator pins. They are enabled as oscillator or I/O pins by the selection of the main oscillator in the Configuration register (see Section 24.1 "Configuration Bits" for details). When they are not used as port pins, RA6 and RA7 and their associated TRIS and LAT bits are read as '0'.

The other PORTA pins are multiplexed with analog inputs, the analog VREF+ and VREF- inputs and the comparator voltage reference output. The operation of pins RA<3:0> and RA5 as A/D converter inputs is selected by clearing or setting the control bits in the ADCON1 register (A/D Control Register 1).

Pins RA0 through RA5 may also be used as comparator inputs or outputs by setting the appropriate bits in the CMCON register. To use RA<3:0> as digital inputs, it is also necessary to turn off the comparators.

Note: On a Power-on Reset, RA5 and RA<3:0> are configured as analog inputs and read as '0'. RA4 is configured as a digital input.

The RA4/T0CKI/C1OUT pin is a Schmitt Trigger input. All other PORTA pins have TTL input levels and full CMOS output drivers.

The TRISA register controls the direction of the PORTA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 11-1: INITIALIZING PORTA

```
CLRF   PORTA   ; Initialize PORTA by
              ; clearing output
              ; data latches
CLRF   LATA    ; Alternate method
              ; to clear output
              ; data latches
MOVLW  0Fh    ; Configure all A/D
MOVWF  ADCON1 ; for digital inputs
MOVWF  07h    ; Configure comparators
MOVWF  CMCON  ; for digital input
MOVLW  0CFh   ; Value used to
              ; initialize data
              ; direction
MOVWF  TRISA  ; Set RA<7:6,3:0> as inputs
              ; RA<5:4> as outputs
```

PIC18F2221/2321/4221/4321 FAMILY

FIGURE 11-3: PARALLEL SLAVE PORT WRITE WAVEFORMS

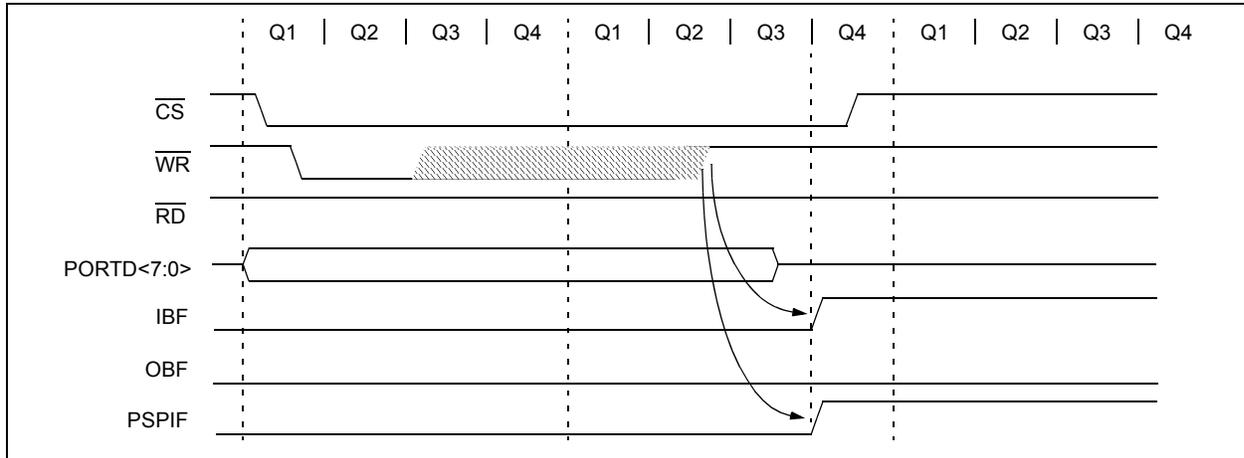


FIGURE 11-4: PARALLEL SLAVE PORT READ WAVEFORMS

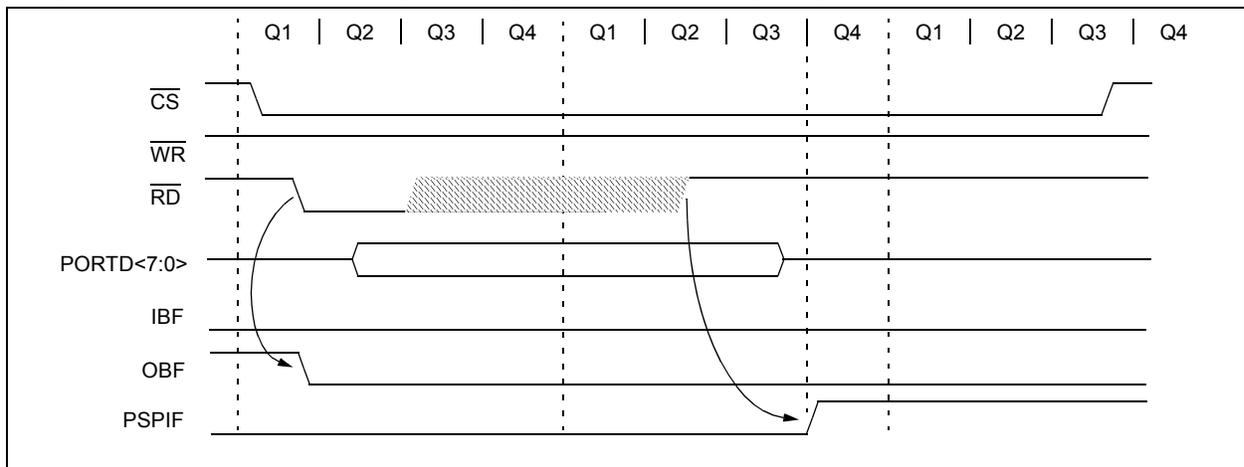


TABLE 11-11: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	58
LATD	PORTD Data Latch Register (Read and Write to Data Latch)								58
TRISD	PORTD Data Direction Register								58
PORTE	—	—	—	—	RE3	RE2	RE1	RE0	58
LATE	—	—	—	—	—	PORTE Data Latch Register (Read and Write to Data Latch)			58
TRISE	IBF	OBF	IBOV	PSPMODE	—	TRISE2	TRISE1	TRISE0	58
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IF	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	58
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	58
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	58
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	57

Legend: — = unimplemented, read as '0'. Shaded cells are not used by the Parallel Slave Port.

Note 1: These bits are unimplemented on 28-pin devices and read as '0'.

PIC18F2221/2321/4221/4321 FAMILY

NOTES:

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17.0 ENHANCED CAPTURE/ COMPARE/PWM (ECCP) MODULE

Note: The ECCP module is implemented only in 40/44-pin devices.

In PIC18F4221/4321 devices, CCP1 is implemented as a standard CCP module with Enhanced PWM capabilities. These include the provision for 2 or 4 output channels, user-selectable polarity, dead-band control and automatic shutdown and restart. The

Enhanced features are discussed in detail in **Section 17.4 “Enhanced PWM Mode”**. Capture, Compare and single-output PWM functions of the ECCP module are the same as described for the standard CCP module.

The control register for the Enhanced CCP module is shown in Register 17-1. It differs from the CCPxCON registers in PIC18F2221/2321 devices in that the two Most Significant bits are implemented to control PWM functionality.

REGISTER 17-1: CCP1CON REGISTER (ECCP1 MODULE, 40/44-PIN DEVICES)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

bit 7-6 **P1M<1:0>**: Enhanced PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A assigned as Capture/Compare input/output; P1B, P1C, P1D assigned as port pins

If CCP1M<3:2> = 11:

00 = Single output: P1A modulated; P1B, P1C, P1D assigned as port pins

01 = Full-bridge output forward: P1D modulated; P1A active; P1B, P1C inactive

10 = Half-bridge output: P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins

11 = Full-bridge output reverse: P1B modulated; P1C active; P1A, P1D inactive

bit 5-4 **DC1B<1:0>**: PWM Duty Cycle bit 1 and bit 0

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPR1L.

bit 3-0 **CCP1M<3:0>**: Enhanced CCP Mode Select bits

0000 = Capture/Compare/PWM off (resets ECCP module)

0001 = Reserved

0010 = Compare mode, toggle output on match

0011 = Capture mode

0100 = Capture mode, every falling edge

0101 = Capture mode, every rising edge

0110 = Capture mode, every 4th rising edge

0111 = Capture mode, every 16th rising edge

1000 = Compare mode, initialize CCP1 pin low, set output on compare match (set CCP1IF)

1001 = Compare mode, initialize CCP1 pin high, clear output on compare match (set CCP1IF)

1010 = Compare mode, generate software interrupt only, CCP1 pin reverts to I/O state

1011 = Compare mode, trigger special event (ECCP resets TMR1 or TMR3, sets CC1IF bit)

1100 = PWM mode; P1A, P1C active-high; P1B, P1D active-high

1101 = PWM mode; P1A, P1C active-high; P1B, P1D active-low

1110 = PWM mode; P1A, P1C active-low; P1B, P1D active-high

1111 = PWM mode; P1A, P1C active-low; P1B, P1D active-low

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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REGISTER 18-5: SSPCON2: MSSP CONTROL REGISTER 2 (I²C™ MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT/ ADMSK5	ACKEN ⁽¹⁾ / ADMSK4	RCEN ⁽¹⁾ / ADMSK3	PEN ⁽¹⁾ / ADMSK2	RSEN ⁽¹⁾ / ADMSK1	SEN ⁽¹⁾

bit 7

bit 0

- bit 7 **GCEN:** General Call Enable bit (Slave mode only)
 1 = Enable interrupt when a general call address (0000h) is received in the SSPSR
 0 = General call address disabled
- bit 6 **ACKSTAT:** Acknowledge Status bit (Master Transmit mode only)
 1 = Acknowledge was not received from slave
 0 = Acknowledge was received from slave
- bit 5 **ACKDT/ADMSK5:** Acknowledge Data bit
In Master Receive mode:
 1 = Not Acknowledge
 0 = Acknowledge
Note: Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
In Slave mode:
 1 = Address masking of ADD5 enabled
 0 = Address masking of ADD5 disabled
- bit 4 **ACKEN/ADMSK4:** Acknowledge Sequence Enable bit
In Master Receive mode:⁽¹⁾
 1 = Initiate Acknowledge sequence on SDA and SCL pins and transmit ACKDT data bit. Automatically cleared by hardware.
 0 = Acknowledge sequence Idle
In Slave mode:
 1 = Address masking of ADD4 enabled
 0 = Address masking of ADD4 disabled
- bit 3 **RCEN/ADMSK3:** Receive Enable bit
In Master Receive mode:⁽¹⁾
 1 = Enables Receive mode for I²C
 0 = Receive Idle
In Slave mode:
 1 = Address masking of ADD3 enabled
 0 = Address masking of ADD3 disabled
- bit 2 **PEN/ADMSK2:** Stop Condition Enable bit
In Master mode:⁽¹⁾
 1 = Initiate Stop condition on SDA and SCL pins. Automatically cleared by hardware.
 0 = Stop condition Idle
In Slave mode:
 1 = Address masking of ADD2 enabled
 0 = Address masking of ADD2 disabled
- bit 1 **RSEN/ADMSK1:** Repeated Start Condition Enable bit
In Master mode:⁽¹⁾
 1 = Initiate Repeated Start condition on SDA and SCL pins. Automatically cleared by hardware.
 0 = Repeated Start condition Idle
In Slave mode (7-Bit Addressing mode):
 1 = Address masking of ADD1 enabled
 0 = Address masking of ADD1 disabled
In Slave mode (10-Bit Addressing mode):
 1 = Address masking of ADD1 and ADD0 enabled
 0 = Address masking of ADD1 and ADD0 disabled

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18.4.4 CLOCK STRETCHING

Both 7-Bit and 10-Bit Slave modes implement automatic clock stretching during a transmit sequence.

The SEN bit (SSPCON2<0>) allows clock stretching to be enabled during receives. Setting SEN will cause the SCL pin to be held low at the end of each data receive sequence.

18.4.4.1 Clock Stretching for 7-Bit Slave Receive Mode (SEN = 1)

In 7-Bit Slave Receive mode, on the falling edge of the ninth clock at the end of the ACK sequence if the BF bit is set, the CKP bit in the SSPCON1 register is automatically cleared, forcing the SCL output to be held low. The CKP bit being cleared to '0' will assert the SCL line low. The CKP bit must be set in the user's ISR before reception is allowed to continue. By holding the SCL line low, the user has time to service the ISR and read the contents of the SSPBUF before the master device can initiate another receive sequence. This will prevent buffer overruns from occurring (see Figure 18-15).

Note 1: If the user reads the contents of the SSPBUF before the falling edge of the ninth clock, thus clearing the BF bit, the CKP bit will not be cleared and clock stretching will not occur.

2: The CKP bit can be set in software regardless of the state of the BF bit. The user should be careful to clear the BF bit in the ISR before the next receive sequence in order to prevent an overflow condition.

18.4.4.2 Clock Stretching for 10-Bit Slave Receive Mode (SEN = 1)

In 10-Bit Slave Receive mode during the address sequence, clock stretching automatically takes place but CKP is not cleared. During this time, if the UA bit is set after the ninth clock, clock stretching is initiated. The UA bit is set after receiving the upper byte of the 10-bit address and following the receive of the second byte of the 10-bit address with the R/W bit cleared to '0'. The release of the clock line occurs upon updating SSPADD. Clock stretching will occur on each data receive sequence as described in 7-bit mode.

Note: If the user polls the UA bit and clears it by updating the SSPADD register before the falling edge of the ninth clock occurs and if the user hasn't cleared the BF bit by reading the SSPBUF register before that time, then the CKP bit will still NOT be asserted low. Clock stretching on the basis of the state of the BF bit only occurs during a data sequence, not an address sequence.

18.4.4.3 Clock Stretching for 7-Bit Slave Transmit Mode

7-Bit Slave Transmit mode implements clock stretching by clearing the CKP bit after the falling edge of the ninth clock if the BF bit is clear. This occurs regardless of the state of the SEN bit.

The user's ISR must set the CKP bit before transmission is allowed to continue. By holding the SCL line low, the user has time to service the ISR and load the contents of the SSPBUF before the master device can initiate another transmit sequence (see Figure 18-10).

Note 1: If the user loads the contents of SSPBUF, setting the BF bit before the falling edge of the ninth clock, the CKP bit will not be cleared and clock stretching will not occur.

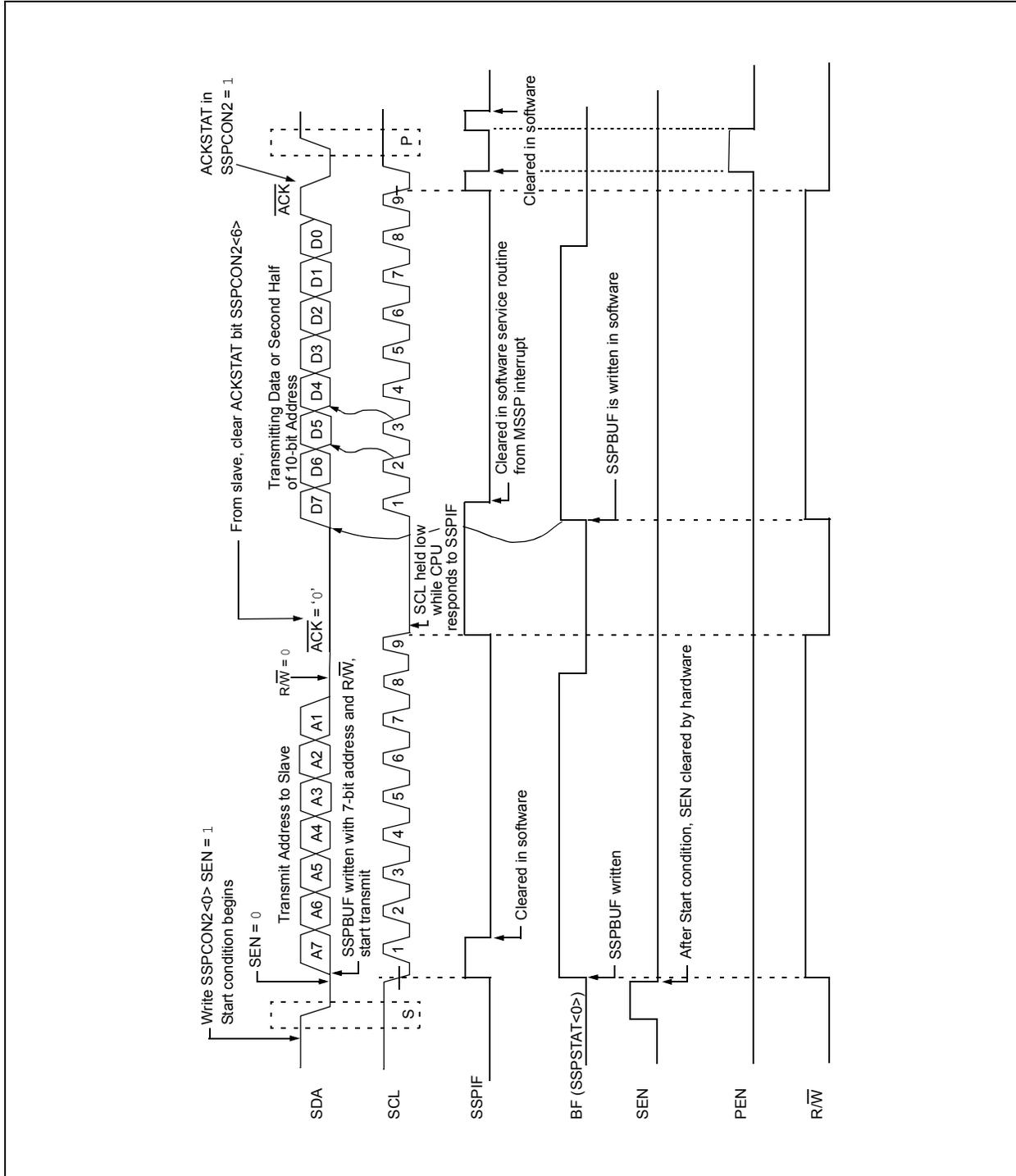
2: The CKP bit can be set in software regardless of the state of the BF bit.

18.4.4.4 Clock Stretching for 10-Bit Slave Transmit Mode

In 10-Bit Slave Transmit mode, clock stretching is controlled during the first two address sequences by the state of the UA bit, just as it is in 10-Bit Slave Receive mode. The first two addresses are followed by a third address sequence which contains the high-order bits of the 10-bit address and the R/W bit set to '1'. After the third address sequence is performed, the UA bit is not set, the module is now configured in Transmit mode and clock stretching is controlled by the BF flag as in 7-Bit Slave Transmit mode (see Figure 18-13).

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FIGURE 18-23: I²C™ MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESSING)



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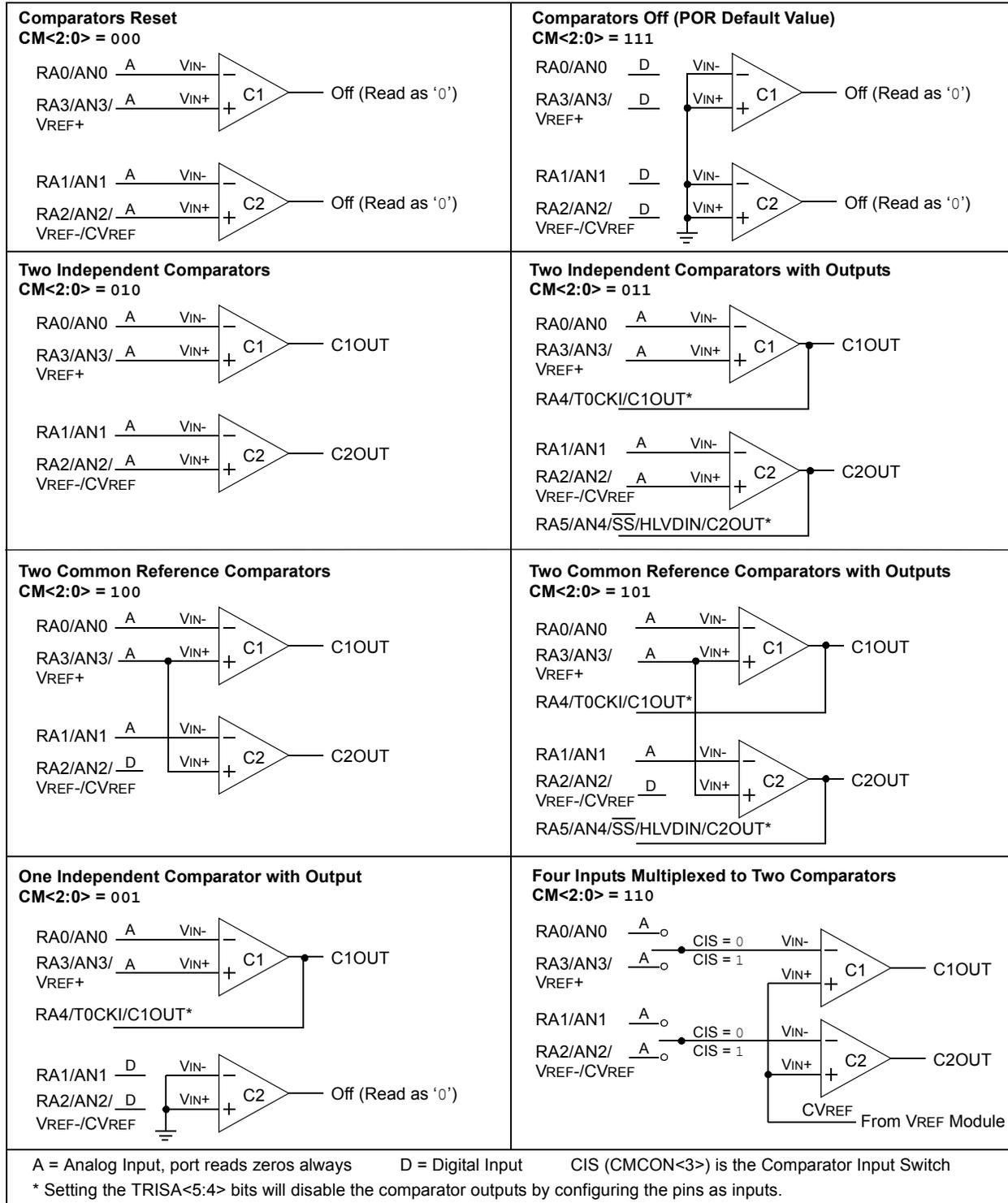
21.1 Comparator Configuration

There are eight modes of operation for the comparators, shown in Figure 21-1. Bits CM<2:0> of the CMCON register are used to select these modes. The TRISA register controls the data direction of the comparator pins for each mode. If the Comparator mode is changed, the

comparator output level may not be valid for the specified mode change delay shown in Section 27.0 “Electrical Characteristics”.

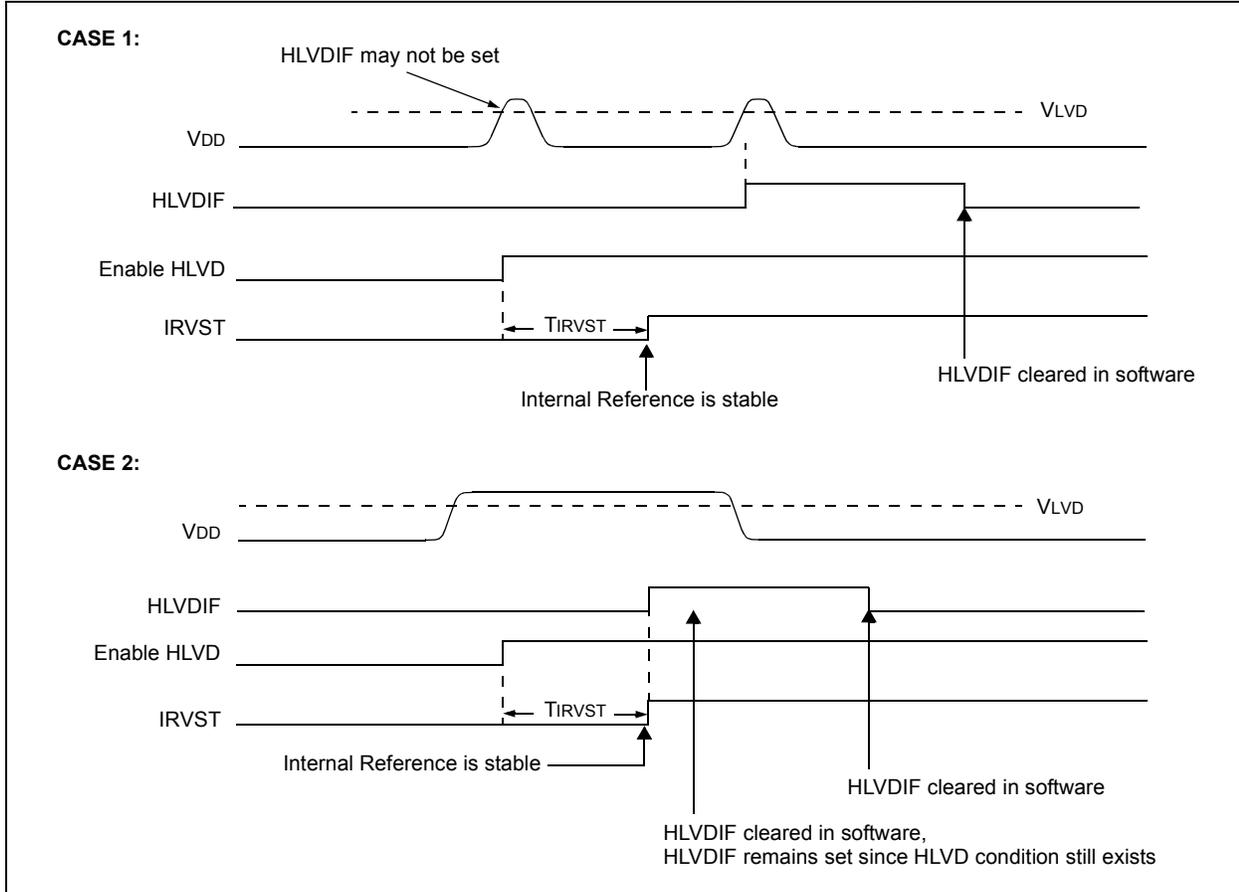
Note: Comparator interrupts should be disabled during a Comparator mode change; otherwise, a false interrupt may occur.

FIGURE 21-1: COMPARATOR I/O OPERATING MODES



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FIGURE 23-3: HIGH-VOLTAGE DETECT OPERATION (VDIRMAG = 1)

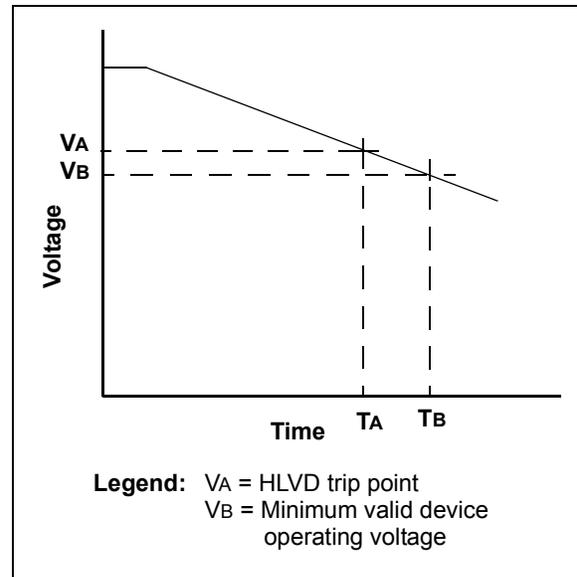


23.5 Applications

In many applications, the ability to detect a drop below or rise above a particular threshold is desirable. For example, the HLVD module could be periodically enabled to detect a Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a high-voltage detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 23-4 shows a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage V_A, the HLVD logic generates an interrupt at time T_A. The interrupt could cause the execution of an ISR, which would allow the application to perform "house-keeping tasks" and perform a controlled shutdown before the device voltage exits the valid operating range at T_B. The HLVD, thus, would give the application a time window, represented by the difference between T_A and T_B, to safely exit.

FIGURE 23-4: TYPICAL LOW-VOLTAGE DETECT APPLICATION



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MULLW Multiply Literal with W

Syntax: MULLW k

Operands: $0 \leq k \leq 255$

Operation: $(W) \times k \rightarrow \text{PRODH:PRODL}$

Status Affected: None

Encoding:

0000	1101	kkkk	kkkk
------	------	------	------

Description: An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in the PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged.
None of the Status flags are affected. Note that neither Overflow nor Carry is possible in this operation. A Zero result is possible but not detected.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write registers PRODH:PRODL

Example: MULLW 0C4h

Before Instruction

W = E2h
PRODH = ?
PRODL = ?

After Instruction

W = E2h
PRODH = ADh
PRODL = 08h

MULWF Multiply W with f

Syntax: MULWF f{,a}

Operands: $0 \leq f \leq 255$
 $a \in [0, 1]$

Operation: $(W) \times (f) \rightarrow \text{PRODH:PRODL}$

Status Affected: None

Encoding:

0000	001a	ffff	ffff
------	------	------	------

Description: An unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged.
None of the Status flags are affected. Note that neither Overflow nor Carry is possible in this operation. A Zero result is possible but not detected. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write registers PRODH:PRODL

Example: MULWF REG, 1

Before Instruction

W = C4h
REG = B5h
PRODH = ?
PRODL = ?

After Instruction

W = C4h
REG = B5h
PRODH = 8Ah
PRODL = 94h

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SUBWFB Subtract W from f with Borrow

Syntax: SUBWFB f {,d {,a}}

Operands: $0 \leq f \leq 255$
 $d \in [0, 1]$
 $a \in [0, 1]$

Operation: $(f) - (W) - (\overline{C}) \rightarrow \text{dest}$

Status Affected: N, OV, C, DC, Z

Encoding:

0101	10da	ffff	ffff
------	------	------	------

Description: Subtract W and the Carry flag (borrow) from register 'f' (2's complement method). If 'd' is '0', the result is stored in W. If 'd' is '1', the result is stored back in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example 1: SUBWFB REG, 1, 0

Before Instruction
REG = 19h (0001 1001)
W = 0Dh (0000 1101)
C = 1

After Instruction
REG = 0Ch (0000 1011)
W = 0Dh (0000 1101)
C = 1
Z = 0
N = 0 ; result is positive

Example 2: SUBWFB REG, 0, 0

Before Instruction
REG = 1Bh (0001 1011)
W = 1Ah (0001 1010)
C = 0

After Instruction
REG = 1Bh (0001 1011)
W = 00h
C = 1
Z = 1 ; result is zero
N = 0

Example 3: SUBWFB REG, 1, 0

Before Instruction
REG = 03h (0000 0011)
W = 0Eh (0000 1101)
C = 1

After Instruction
REG = F5h (1111 0100)
; [2's comp]
W = 0Eh (0000 1101)
C = 0
Z = 0
N = 1 ; result is negative

SWAPF Swap f

Syntax: SWAPF f {,d {,a}}

Operands: $0 \leq f \leq 255$
 $d \in [0, 1]$
 $a \in [0, 1]$

Operation: $(f<3:0>) \rightarrow \text{dest}<7:4>$,
 $(f<7:4>) \rightarrow \text{dest}<3:0>$

Status Affected: None

Encoding:

0011	10da	ffff	ffff
------	------	------	------

Description: The upper and lower nibbles of register 'f' are exchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in register 'f' (default). If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \leq 95$ (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

Example: SWAPF REG, 1, 0

Before Instruction
REG = 53h

After Instruction
REG = 35h

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27.4 AC (Timing) Characteristics

27.4.1 TIMING PARAMETER SYMBOLOGY

The timing parameter symbols have been created using one of the following formats:

1. TppS2ppS
2. TppS
3. Tcc:ST (I²C specifications only)
4. Ts (I²C specifications only)

<p>T</p> <p>F Frequency</p>	<p>T</p> <p>Time</p>
----------------------------------	----------------------

Lowercase letters (pp) and their meanings:

<p>pp</p> <p>cc CCP1</p> <p>ck CLKO</p> <p>cs \overline{CS}</p> <p>di SDI</p> <p>do SDO</p> <p>dt Data in</p> <p>io I/O port</p> <p>mc \overline{MCLR}</p>	<p>osc OSC1</p> <p>rd \overline{RD}</p> <p>rw \overline{RD} or \overline{WR}</p> <p>sc SCK</p> <p>ss \overline{SS}</p> <p>t0 T0CKI</p> <p>t1 T13CKI</p> <p>wr \overline{WR}</p>
--	--

Uppercase letters and their meanings:

<p>S</p> <p>F Fall</p> <p>H High</p> <p>I Invalid (High-impedance)</p> <p>L Low</p> <p>I²C only</p> <p>AA output access</p> <p>BUF Bus free</p>	<p>P Period</p> <p>R Rise</p> <p>V Valid</p> <p>Z High-impedance</p> <p>High High</p> <p>Low Low</p>
--	--

Tcc:ST (I²C specifications only)

<p>CC</p> <p>HD Hold</p> <p>ST</p> <p>DAT DATA input hold</p> <p>STA Start condition</p>	<p>SU Setup</p> <p>STO Stop condition</p>
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FIGURE 27-21: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

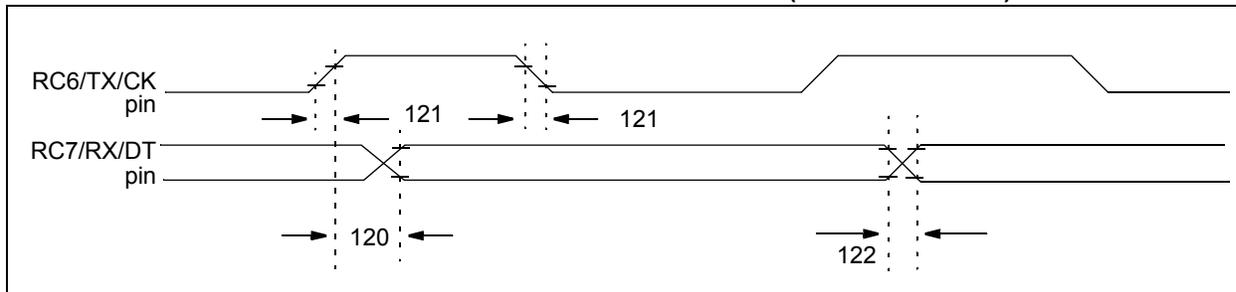


TABLE 27-22: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions	
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock High to Data Out Valid	PIC18FXXXX	—	40	ns	
			PIC18LFXXXX	—	100	ns	VDD = 2.0V
121	Tckrf	Clock Out Rise Time and Fall Time (Master mode)	PIC18FXXXX	—	20	ns	
			PIC18LFXXXX	—	50	ns	VDD = 2.0V
122	Tdtrf	Data Out Rise Time and Fall Time	PIC18FXXXX	—	20	ns	
			PIC18LFXXXX	—	50	ns	VDD = 2.0V

FIGURE 27-22: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

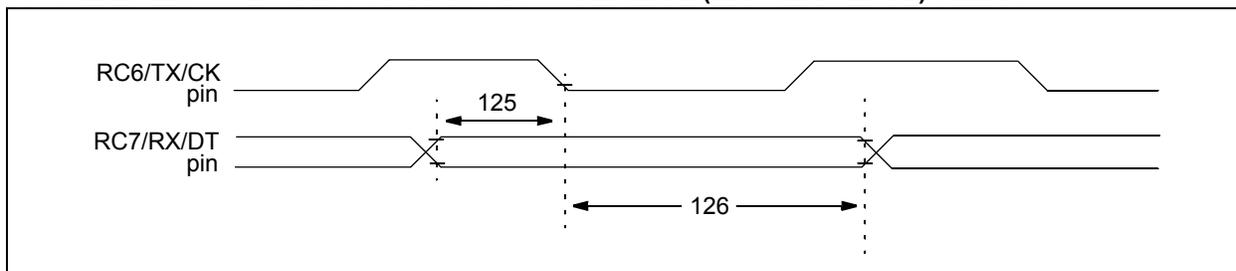


TABLE 27-23: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
125	TdtV2ckl	SYNC RCV (MASTER & SLAVE)				
		Data Hold before CK ↓ (DT hold time)	10	—	ns	
126	TckL2dtl	Data Hold after CK ↓ (DT hold time)	15	—	ns	

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PIC18F2221/2321/4221/4321 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

<u>PART NO.</u>	<u>X</u>	<u>/XX</u>	<u>XXX</u>
Device	Temperature Range	Package	Pattern
Device	PIC18F2221/2321 ⁽¹⁾ , PIC18F4221/4321 ⁽¹⁾ , PIC18F2221/2321T ⁽²⁾ , PIC18F4221/4321T ⁽²⁾ ; VDD range 4.2V to 5.5V PIC18LF2221/2321 ⁽¹⁾ , PIC18LF4221/4321 ⁽¹⁾ , PIC18LF2221/2321T ⁽²⁾ , PIC18LF4221/4321T ⁽²⁾ ; VDD range 2.0V to 5.5V		
Temperature Range	I = -40°C to +85°C (Industrial) E = -40°C to +125°C (Extended)		
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SS = SSOP SP = Skinny Plastic DIP P = PDIP ML = QFN		
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)		

Examples:

- a) PIC18F4321-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301.
- b) PIC18LF2321-I/SO = Industrial temp., SOIC package, Extended VDD limits.
- c) PIC18LF4321-I/P = Industrial temp., PDIP package, normal VDD limits.

Note 1: F = Standard Voltage Range
 LF = Wide Voltage Range
2: T = in tape and reel