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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	4.2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18f2321t-i-so

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

REGISTER 7-1:	EECON1:	DATA EEF	PROM CO	NTROL RE	GISTER 1					
	R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0		
	EEPGD	CFGS	—	FREE	WRERR	WREN	WR	RD		
	bit 7							bit 0		
bit 7	EEPGD: F	lash Prograr	n or Data El	EPROM Me	mory Select	bit				
	1 = Acces 0 = Acces	s Flash prog s data EEPF	ram memor ROM memor	у Ту						
bit 6	CFGS: Fla	sh Program/	Data EEPR	OM or Conf	iguration Sel	lect bit				
	1 = Acces 0 = Acces	s Configurat s Flash prog	ion registers ram or data	s EEPROM r	nemory					
bit 5	Unimplem	ented: Read	<b>d as</b> '0'							
bit 4	FREE: Flas	sh Row Eras	e Enable bi	t						
	1 = Erase (cleare 0 = Perfor	the program ed by comple m write-only	memory ro etion of eras	w addresse e operation)	d by TBLPTF )	R on the ne	kt WR comn	hand		
bit 3	WRERR: F	lash Progra	m/Data EEF	PROM Error	Flag bit					
	1 = A write norma 0 = The wr	e operation i l operation, rite operatio	s premature or an improj n completec	ely terminate per write atte	d (any Rese empt)	et during sel	f-timed prog	ramming in		
	<b>Note:</b> When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.									
bit 2	WREN: Fla	ash Program	/Data EEPF	ROM Write E	nable bit					
	1 = Allows 0 = Inhibits	write cycles s write cycle	s to Flash pr s to Flash p	ogram/data rogram/data	EEPROM EEPROM					
bit 1	WR: Write	Control bit								
<ul> <li>1 = Initiates a data EEPROM erase/write cycle or a program memory erase/write cycle. (The operation is self-timed and the bit is cleared by hardware once write is comp The WR bit can only be set (not cleared) in software.)</li> <li>0 = Write cycle to the EEPROM is complete</li> </ul>							cle. omplete.			
bit 0	RD: Read Control bit									
	<ul> <li>1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1 or CFGS = 1.)</li> <li>0 = Does not initiate an EEPROM read</li> </ul>									
	Legend:									
	R = Reada	ble bit	W = W	/ritable bit						
	S = Bit can	be set by s	oftware, but	not cleared	U = Unim	plemented	bit, read as	'0'		

'1' = Bit is set

'0' = Bit is cleared

-n = Value at POR

x = Bit is unknown

Pin	Function	TRIS Setting	I/O	I/O Type	Description
RA0/AN0	RA0	0	0	DIG	LATA<0> data output; not affected by analog input.
		1	I	TTL	PORTA<0> data input; disabled when analog input enabled.
	AN0	1	I	ANA	A/D Input Channel 0 and Comparator C1- input. Default input configuration on POR; does not affect digital output.
RA1/AN1	RA1	0	0	DIG	LATA<1> data output; not affected by analog input.
		1	I	TTL	PORTA<1> data input; disabled when analog input enabled.
	AN1	1	I	ANA	A/D Input Channel 1 and Comparator C2- input. Default input configuration on POR; does not affect digital output.
RA2/AN2/ Vref-/CVref	RA2	0	0	DIG	LATA<2> data output; not affected by analog input. Disabled when CVREF output enabled.
		1	I	TTL	PORTA<2> data input. Disabled when analog functions enabled; disabled when CVREF output enabled.
	AN2	1	I	ANA	A/D Input Channel 2 and Comparator C2+ input. Default input configuration on POR; not affected by analog output.
	VREF-	1	I	ANA	A/D and comparator voltage reference low input.
	CVREF	х	0	ANA	Comparator voltage reference output. Enabling this feature disables digital I/O.
RA3/AN3/VREF+	RA3	0	0	DIG	LATA<3> data output; not affected by analog input.
		1	Ι	TTL	PORTA<3> data input; disabled when analog input enabled.
	AN3	1	Ι	ANA	A/D Input Channel 3 and Comparator C1+ input. Default input configuration on POR.
	VREF+	1	Ι	ANA	A/D and comparator voltage reference high input.
RA4/T0CKI/C1OUT	RA4	0	0	DIG	LATA<4> data output.
		1	I	ST	PORTA<4> data input; default configuration on POR.
	T0CKI	1	I	ST	Timer0 clock input.
	C10UT	0	0	DIG	Comparator 1 output; takes priority over port data.
RA5/AN4/SS/	RA5	0	0	DIG	LATA<5> data output; not affected by analog input.
HLVDIN/C2OUT		1	I	TTL	PORTA<5> data input; disabled when analog input enabled.
	AN4	1	I	ANA	A/D Input Channel 4. Default configuration on POR.
	SS	1	Ι	TTL	Slave Select input for MSSP (MSSP module).
	HLVDIN	1	I	ANA	High/Low-Voltage Detect external trip point input.
	C2OUT	0	0	DIG	Comparator 2 output; takes priority over port data.
OSC2/CLKO/RA6	RA6	0	0	DIG	LATA<6> data output. Enabled in RCIO, INTIO2 and ECIO modes only.
		1	I	TTL	PORTA<6> data input. Enabled in RCIO, INTIO2 and ECIO modes only.
	OSC2	х	0	ANA	Main oscillator feedback output connection (XT, HS and LP modes).
	CLKO	х	0	DIG	System cycle clock output (Fosc/4) in RC, INTIO1 and EC Oscillator modes.
OSC1/CLKI/RA7	RA7	0	0	DIG	LATA<7> data output. Disabled in external oscillator modes.
		1	I	TTL	PORTA<7> data input. Disabled in external oscillator modes.
	OSC1	x	Ι	ANA	Main oscillator input connection.
	CLKI	х	I	ANA	Main clock input connection.

# TABLE 11-1: PORTA I/O SUMMARY

Legend: DIG = Digital level output; TTL = TTL input buffer; ST = Schmitt Trigger input buffer; ANA = Analog level input/output; x = Don't care (TRIS bit does not affect port direction or is overridden for this option).

#### TABLE 11-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	58
LATD	PORTD Data Latch Register (Read and Write to Data Latch)								58
TRISD	PORTD Data Direction Register							58	
TRISE	IBF	OBF	IBOV	PSPMODE		TRISE2	TRISE1	TRISE0	58
CCP1CON	P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	57

**Legend:** — = unimplemented, read as '0'. Shaded cells are not used by PORTD.

# 12.0 TIMER0 MODULE

The Timer0 module incorporates the following features:

- Software selectable operation as a timer or counter in both 8-bit or 16-bit modes
- · Readable and writable registers
- Dedicated 8-bit, software programmable
   prescaler
- Selectable clock source (internal or external)
- Edge select for external clock
- · Interrupt-on-overflow

The T0CON register (Register 12-1) controls all aspects of the module's operation, including the prescale selection. It is both readable and writable.

A simplified block diagram of the Timer0 module in 8-bit mode is shown in Figure 12-1. Figure 12-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

### REGISTER 12-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	TOCS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

- bit 7 TMR0ON: Timer0 On/Off Control bit
  - 1 = Enables Timer0
  - 0 = Stops Timer0
- bit 6 **T08BIT**: Timer0 8-Bit/16-Bit Control bit
  - 1 = Timer0 is configured as an 8-bit timer/counter
  - 0 = Timer0 is configured as a 16-bit timer/counter
- bit 5 **TOCS**: Timer0 Clock Source Select bit
  - 1 = Transition on T0CKI pin
  - 0 = Internal instruction cycle clock (CLKO)
- bit 4 TOSE: Timer0 Source Edge Select bit
  - 1 = Increment on high-to-low transition on TOCKI pin
  - 0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA**: Timer0 Prescaler Assignment bit
  - 1 = TImer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
  - 0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.
- bit 2-0 TOPS<2:0>: Timer0 Prescaler Select bits
  - 111 = 1:256 Prescale value
  - 110 = 1:128 Prescale value
  - 101 = 1:64 Prescale value
  - 100 = 1:32 Prescale value
  - 011 = 1:16 Prescale value
  - 010 = 1:8 Prescale value
  - 001 = 1:4 Prescale value
  - 000 = 1:2 Prescale value

#### Legend:

Legenu.			
R = Readable bit	W = Writable bit	U = Unimplemented b	it, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

# 13.2 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 13-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 high byte buffer. This provides the user with the ability to accurately read all 16 bits of Timer1 without having to determine whether a read of the high byte, followed by a read of the low byte, has become invalid due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H Buffer register. The Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 High Byte Buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

# 13.3 Timer1 Oscillator

An on-chip crystal oscillator circuit is incorporated between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting the Timer1 Oscillator Enable bit, T1OSCEN (T1CON<3>). The oscillator is a low-power circuit rated for 32 kHz crystals. It will continue to run during all power-managed modes. The circuit for a typical LP oscillator is shown in Figure 13-3. Table 13-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

#### FIGURE 13-3: EXTERNAL COMPONENTS FOR THE TIMER1 LP OSCILLATOR



# TABLE 13-1:CAPACITOR SELECTION FOR<br/>THE TIMER OSCILLATOR

Osc Type	Freq	C1	C2			
LP	32 kHz	27 pF <sup>(1)</sup>	27 pF <sup>(1)</sup>			
Note 1: 1	Microchip sug starting point sircuit.	gests these in validating	values as a the oscillator			
2: H	Higher capacitance increases the stability of the oscillator but also increases the start-up time.					
3: 5 t a	Since each rescharacteristics haracteristics he resonator appropriate components.	sonator/crysta , the user sh /crystal mani values o	l has its own ould consult ufacturer for f external			
<b>4</b> : (	Capacitor valuonly.	es are for des	ign guidance			

#### 13.3.1 USING TIMER1 AS A CLOCK SOURCE

The Timer1 oscillator is also available as a clock source in power-managed modes. By setting the clock select bits, SCS<1:0> (OSCCON<1:0>), to '01', the device switches to SEC\_RUN mode; both the CPU and peripherals are clocked from the Timer1 oscillator. If the IDLEN bit (OSCCON<7>) is cleared and a SLEEP instruction is executed, the device enters SEC\_IDLE mode. Additional details are available in **Section 4.0 "Power-Managed Modes"**.

Whenever the Timer1 oscillator is providing the clock source, the Timer1 system clock status flag, T1RUN (T1CON<6>), is set. This can be used to determine the controller's current clocking mode. It can also indicate the clock source being currently used by the Fail-Safe Clock Monitor. If the Clock Monitor is enabled and the Timer1 oscillator fails while providing the clock, polling the T1RUN bit will indicate whether the clock is being provided by the Timer1 oscillator or another source.

# 13.3.2 LOW-POWER TIMER1 OPTION

The Timer1 oscillator can operate at two distinct levels of power consumption based on device configuration. When the LPT1OSC Configuration bit is set, the Timer1 oscillator operates in a low-power mode. When LPT1OSC is not set, Timer1 operates at a higher power level. Power consumption for a particular mode is relatively constant, regardless of the device's operating mode. The default Timer1 configuration is the higher power mode.

As the low-power Timer1 mode tends to be more sensitive to interference, high noise environments may cause some oscillator instability. The low-power option is, therefore, best suited for low noise applications where power conservation is an important design consideration.

### 17.4.4 HALF-BRIDGE MODE

In the Half-Bridge Output mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the P1A pin, while the complementary PWM output signal is output on the P1B pin (Figure 17-4). This mode can be used for half-bridge applications, as shown in Figure 17-5, or for full-bridge applications where four power switches are being modulated with two PWM signals.

In Half-Bridge Output mode, the programmable deadband delay can be used to prevent shoot-through current in half-bridge power devices. The value of bits, PDC<6:0>, sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 17.4.6 "Programmable Dead-Band Delay"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORTC<2> and PORTD<5> data latches, the TRISC<2> and TRISD<5> bits must be cleared to configure P1A and P1B as outputs.

# FIGURE 17-4: HALF-BRIDGE PWM



### FIGURE 17-5: EXAMPLES OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



REGISTER 17-3:	ECCP1AS: ENHANCED CAPTURE/COMPARE/PWM AUTO-SHUTDOWN CONTROL REGISTER									
	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0		
	ECCPASE	ECCPAS2	ECCPAS1	ECCPAS0	PSSAC1	PSSAC0	PSSBD1 <sup>(1)</sup>	PSSBD0 <sup>(1)</sup>		
	bit 7							bit 0		
bit 7	ECCPASE:	ECCP Auto	-Shutdown	Event Status	bit					
	1 = A shutcome = ECCP	outputs are	nas occurreo operating	d; ECCP out	puts are in	shutdown	state			
bit 6-4	ECCPAS<2	:0>: ECCP	Auto-Shutdo	own Source	Select bits					
bit 3-2	<ul> <li>111 = FLT0 or Comparator 1 or Comparator 2</li> <li>110 = FLT0 or Comparator 2</li> <li>101 = FLT0 or Comparator 1</li> <li>100 = FLT0</li> <li>011 = Either Comparator 1 or 2</li> <li>010 = Comparator 2 output</li> <li>001 = Comparator 1 output</li> <li>000 = Auto-shutdown is disabled</li> </ul>									
	<ul> <li>1x = Pins A and C are tri-state (40/44-pin devices);</li> <li>PWM output is tri-state (28-pin devices)</li> <li>01 = Drive Pins A and C to '1'</li> <li>00 = Drive Pins A and C to '0'</li> </ul>									
bit 1-0	PSSBD<1:0>: Pins B and D Shutdown State Control bits <sup>(1)</sup> 1x = Pins B and D tri-state 01 = Drive Pins B and D to '1' 00 = Drive Pins B and D to '0'									
	Note 1:	Unimpleme	nted on 28-p	oin devices; l	bits read as	<b>3</b> 'O'.				

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

### 18.3.6 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

Before enabling the module in SPI Slave mode, the clock line must match the proper Idle state. The clock line can be observed by reading the SCK pin. The Idle state is determined by the CKP bit (SSPCON1<4>).

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in Sleep mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from Sleep.

### 18.3.7 SLAVE SELECT SYNCHRONIZATION

The  $\overline{SS}$  pin allows a Synchronous Slave mode. The SPI operation must be in Slave mode with the  $\overline{SS}$  pin control enabled (SSPCON1<3:0> = 04h). When the  $\overline{SS}$  pin is low, transmission and reception are enabled and the

SDO pin is driven. When the  $\overline{SS}$  pin goes high, the SDO pin is no longer driven, even if in the middle of a transmitted byte and becomes a floating output. External pull-up/pull-down resistors may be desirable depending on the application.

Note 1:	When	the SPI	interfa	ace is in Sla	ave mode
	with	SS	pin	control	enabled
	(SSPC	ON1<3	:0>=0	100), the SI	PI module
	will res	et if the	SS pir	n is set to Vi	DD.

2: If the SPI interface is used in Slave mode with CKE set, then the SS pin control must be enabled.

When the SPI module resets, the bit counter is forced to '0'. This can be done by either forcing the  $\overline{SS}$  pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function) since it cannot create a bus conflict.

### FIGURE 18-4: SLAVE SYNCHRONIZATION WAVEFORM



#### 18.4.3.2 Address Masking

Masking an address bit causes that bit to become a "don't care". When one address bit is masked, two addresses will be Acknowledged and cause an interrupt. It is possible to mask more than one address bit at a time, which makes it possible to Acknowledge up to 31 addresses in 7-Bit Addressing mode and up to 63 addresses in 10-Bit Addressing mode (see Example 18-2).

The  $l^2C$  slave behaves the same way whether address masking is used or not. However, when address masking is used, the  $l^2C$  slave can Acknowledge multiple addresses and cause interrupts. When this occurs, it is necessary to determine which address caused the interrupt by checking the SSPBUF register.

• 7-Bit Addressing mode

Address mask bits, ADMSK<5:1>, mask the corresponding address bits in the SSPADD register. For any ADMSK bits that are active (ADMSK<n> = 1), the corresponding address bit is ignored (ADD<n> = x). For the module to issue an address Acknowledge, it is sufficient to match only on addresses that do not have an active address mask.

#### • 10-Bit Addressing mode

Address mask bits, ADMSK<5:2>, mask the corresponding address bits in the SSPADD register. In addition, ADMSK<1> simultaneously masks the two LSBs of the address, ADD<1:0>. For any ADMSK bits that are active (ADMSK<n> = 1), the corresponding address bit is ignored (ADD<n> = x). Also note that although in 10-Bit Addressing mode, the upper address bits reuse part of the SSPADD register bits, the address mask bits do not interact with those bits. They only affect the lower address bits.

Note 1: ADMSK<1> masks the two Least Significant bits of the address.

2: The two Most Significant bits of the address are not affected by address masking.

### EXAMPLE 18-2: ADDRESS MASKING

#### 7-Bit Addressing mode:

SSPADD<7:1> = 1010 0000

ADMSK<5:1> = 00 111

Addresses Acknowledged = 0xA0, 0xA2, 0xA4, 0xA6, 0xA8, 0xAA, 0xAC, 0xAE

#### 10-Bit Addressing mode:

SSPADD<7:0> = 1010 0000 (The two MSbs are ignored in this example since they are not affected)

ADMSK<5:1> = 00 111

Addresses Acknowledged = 0xA0, 0xA1, 0xA2, 0xA3, 0xA4, 0xA5, 0xA6, 0xA7, 0xA8, 0xA9, 0xAA, 0xAB, 0xAC, 0xAD, 0xAE, 0xAF

The upper two bits are not affected by the address masking.

#### FIGURE 18-29: BUS COLLISION DURING START CONDITION (SCL = 0)



#### FIGURE 18-30: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



The value in the ADRESH:ADRESL registers is not modified for a Power-on Reset. The ADRESH:ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see **Section 20.1 "A/D Acquisition Requirements"**. After this acquisition time has elapsed, the A/D conversion can be started. An acquisition time can be programmed to occur between setting the GO/DONE bit and the actual start of the conversion.

The following steps should be followed to perform an A/D conversion:

- 1. Configure the A/D module:
  - Configure analog pins, voltage reference and digital I/O (ADCON1)
  - Select A/D input channel (ADCON0)
  - Select A/D acquisition time (ADCON2)
  - Select A/D conversion clock (ADCON2)
  - Turn on A/D module (ADCON0)
- 2. Configure A/D interrupt (if desired):
  - · Clear ADIF bit
  - · Set ADIE bit
  - Set GIE bit
- 3. Wait the required acquisition time (if required).
- 4. Start conversion:
  - Set GO/DONE bit (ADCON0 register)

5. Wait for A/D conversion to complete, by either:

# • Polling for the GO/DONE bit to be cleared OR

• Waiting for the A/D interrupt

- 6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
- 7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before the next acquisition starts.

### FIGURE 20-2: A/D TRANSFER FUNCTION





# FIGURE 20-3: ANALOG INPUT MODEL

# 23.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

PIC18F2221/2321/4221/4321 family devices have a High/Low-Voltage Detect module (HLVD). This is a programmable circuit that allows the user to specify both a device voltage trip point and the direction of change from that point. If the device experiences an excursion past the trip point in that direction, an interrupt flag is set. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The High/Low-Voltage Detect Control register (Register 23-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

The block diagram for the HLVD module is shown in Figure 23-1.

### REGISTER 23-1: HLVDCON: HIGH/LOW-VOLTAGE DETECT CONTROL REGISTER

F	R/W-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
VD	IRMAG		IRVST	HLVDEN	HLVDL3	HLVDL2	HLVDL1	HLVDL0
bit 7	7							bit 0

+ 7	VDIRMAG: Voltage Direction Magnitude Select hit
. /	
	1 = Event occurs when voltage equals or exceeds trip point (HLVDL<3:0>)
	0 = Event occurs when voltage equals or falls below trip point (HLVDL<3:0>)
t 6	Unimplemented: Read as '0'
t 5	IRVST: Internal Reference Voltage Stable Flag bit
	1 = Indicates that the voltage detect logic will generate the interrupt flag at the specified voltage range
	<ul> <li>Indicates that the voltage detect logic will not generate the interrupt flag at the specified voltage range and the HLVD interrupt should not be enabled</li> </ul>
t 4	HLVDEN: High/Low-Voltage Detect Power Enable bit
	1 = HLVD enabled
	0 = HLVD disabled
t 3-0	HLVDL<3:0>: Voltage Detection Limit bits
	1111 = External analog input is used (input comes from the HI VDIN pin)
	1110 = Maximum setting
	0000 = Minimum setting
	Note: See Table 27-4 in Section 27.0 "Electrical Characteristics" for the specifications.
	Logondy

Legena:			
R = Readable bit	W = Writable bit	U = Unimplemented	bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

The module is enabled by setting the HLVDEN bit. Each time that the HLVD module is enabled, the circuitry requires some time to stabilize. The IRVST bit is a read-only bit and is used to indicate when the circuit is stable. The module can only generate an interrupt after the circuit is stable and IRVST is set. The VDIRMAG bit determines the overall operation of the module. When VDIRMAG is cleared, the module monitors for drops in VDD below a predetermined set point. When the bit is set, the module monitors for rises in VDD above the set point.

# 23.2 HLVD Setup

The following steps are needed to set up the HLVD module:

- 1. Disable the module by clearing the HLVDEN bit (HLVDCON<4>).
- 2. Write the value to the HLVDL<3:0> bits that selects the desired HLVD trip point.
- Set the VDIRMAG bit to detect high voltage (VDIRMAG = 1) or low voltage (VDIRMAG = 0).
- 4. Enable the HLVD module by setting the HLVDEN bit.
- 5. Clear the HLVD interrupt flag (PIR2<2>), which may have been set from a previous interrupt.
- Enable the HLVD interrupt if interrupts are desired by setting the HLVDIE and GIE bits (PIE<2> and INTCON<7>). An interrupt will not be generated until the IRVST bit is set.

### 23.3 Current Consumption

When the module is enabled, the HLVD comparator and voltage divider are enabled and will consume static current. The total current consumption, when enabled, is specified in electrical specification parameter D022B. Depending on the application, the HLVD module does not need to be operating constantly. To decrease the current requirements, the HLVD circuitry may only need to be enabled for short periods where the voltage is checked. After doing the check, the HLVD module may be disabled.

# 23.4 HLVD Start-up Time

The internal reference voltage of the HLVD module, specified in electrical specification parameter D420, may be used by other internal circuitry, such as the Programmable Brown-out Reset. If the HLVD or other circuits using the voltage reference are disabled to lower the device's current consumption, the reference voltage circuit will require time to become stable before a low or high-voltage condition can be reliably detected. This start-up time, TIRVST, is an interval that is independent of device clock speed. It is specified in electrical specification parameter 36.

The HLVD interrupt flag is not enabled until TIRVST has expired and a stable reference voltage is reached. For this reason, brief excursions beyond the set point may not be detected during this interval. Refer to Figure 23-2 or Figure 23-3.





#### REGISTER 24-3: CONFIG2H: CONFIGURATION REGISTER 2 HIGH (BYTE ADDRESS 300003h) R/P-1 R/P-1 U-0 U-0 U-0 R/P-1 R/P-1 R/P-1 WDTPS0 WDTEN WDTPS3 WDTPS2 WDTPS1 bit 7 bit 0

- bit 7-5 Unimplemented: Read as '0'
- bit 4-1 WDTPS<3:0>: Watchdog Timer Postscale Select bits

1111	=	1:32,768
1110	=	1:16,384
1101	=	1:8,192
1100	=	1:4,096
1011	=	1:2,048
1010	=	1:1,024
1001	=	1:512
1000	=	1:256
0111	=	1:128
0110	=	1:64
0101	=	1:32
0100	=	1:16
0011	=	1:8
0010	=	1:4
0001	=	1:2
0000	=	1:1
		I. Wotobd

- bit 0 WDTEN: Watchdog Timer Enable bit
  - 1 = WDT enabled
  - 0 = WDT disabled (control is placed on the SWDTEN bit)

Legend:					
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'			
-n = Value when device is unprogrammed		u = Unchanged from programmed state			

# 24.3 Two-Speed Start-up

The Two-Speed Start-up feature helps to minimize the latency period from oscillator start-up to code execution by allowing the microcontroller to use the INTOSC oscillator as a clock source until the primary clock source is available. It is enabled by setting the IESO Configuration bit.

Two-Speed Start-up should be enabled only if the primary oscillator mode is LP, XT, HS or HSPLL (crystal-based modes). Other sources do not require an OST start-up delay; for these, Two-Speed Start-up should be disabled.

When enabled, Resets and wake-ups from Sleep mode cause the device to configure itself to run from the internal oscillator block as the clock source, following the time-out of the Power-up Timer after a Power-on Reset is enabled. This allows almost immediate code execution while the primary oscillator starts and the OST is running. Once the OST times out, the device automatically switches to PRI\_RUN mode.

To use a higher clock speed on wake-up, the INTOSC or postscaler clock sources can be selected to provide a higher clock speed by setting bits, IRCF<2:0>, immediately after Reset. For wake-ups from Sleep, the INTOSC or postscaler clock sources can be selected by setting the IRCF<2:0> bits prior to entering Sleep mode.

In all other power-managed modes, Two-Speed Startup is not used. The device will be clocked by the currently selected clock source until the primary clock source becomes available. The setting of the IESO bit is ignored.

#### 24.3.1 SPECIAL CONSIDERATIONS FOR USING TWO-SPEED START-UP

While using the INTOSC oscillator in Two-Speed Startup, the device still obeys the normal command sequences for entering power-managed modes, including multiple SLEEP instructions (refer to **Section 4.1.4 "Multiple Sleep Commands"**). In practice, this means that user code can change the SCS<1:0> bit settings or issue SLEEP instructions before the OST times out. This would allow an application to briefly wake-up, perform routine "housekeeping" tasks and return to Sleep before the device starts to operate from the primary oscillator.

User code can also check if the primary clock source is currently providing the device clocking by checking the status of the OSTS bit (OSCCON<3>). If the bit is set, the primary oscillator is providing the clock. Otherwise, the internal oscillator block is providing the clock during wake-up from Reset or Sleep mode.



	J- <u>Z</u> .								1
Mnemonic, Operands		Description	Cycles	16-Bit Instruction Word			Status	Neter	
				MSb			LSb	Affected	NOLES
BIT-ORIENTED OPERATIONS									
BCF	f, b, a	Bit Clear f	1	1001	bbba	ffff	ffff	None	1, 2
BSF	f, b, a	Bit Set f	1	1000	bbba	ffff	ffff	None	1, 2
BTFSC	f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011	bbba	ffff	ffff	None	3, 4
BTFSS	f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010	bbba	ffff	ffff	None	3, 4
BTG	f, d, a	Bit Toggle f	1	0111	bbba	ffff	ffff	None	1, 2
CONTROL OPERATIONS									
BC	n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN	n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC	n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN	n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV	n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ	n	Branch if Not Zero	1 (2)	1110	0001	nnnn	nnnn	None	
BOV	n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA	n	Branch Unconditionally	2	1101	0nnn	nnnn	nnnn	None	
BZ	n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL	n, s	Call Subroutine 1st Word	2	1110	110s	kkkk	kkkk	None	
		2nd Word		1111	kkkk	kkkk	kkkk	l	
CLRWDT	—	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW	—	Decimal Adjust WREG	1	0000	0000	0000	0111	С	
GOTO	n	Go to Address 1st Word	2	1110	1111	kkkk	kkkk	None	
		2nd Word		1111	kkkk	kkkk	kkkk		
NOP	_	No Operation	1	0000	0000	0000	0000	None	
NOP	—	No Operation	1	1111	XXXX	XXXX	XXXX	None	4
POP	—	Pop Top of Return Stack (TOS)	1	0000	0000	0000	0110	None	
PUSH	—	Push Top of Return Stack (TOS)	1	0000	0000	0000	0101	None	
RCALL	n	Relative Call	2	1101	lnnn	nnnn	nnnn	None	
RESET		Software Device Reset	1	0000	0000	1111	1111	All	
RETFIE	S	Return from Interrupt Enable	2	0000	0000	0001	000s	GIE/GIEH, PEIE/GIEL	
RETLW	k	Return with Literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN	s	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP	_	Go into Standby mode	1	0000	0000	0000	0011	TO, PD	

#### TABLE 25-2: PIC18FXXXX INSTRUCTION SET (CONTINUED)

**Note 1:** When a PORT register is modified as a function of itself (e.g., MOVF PORTE, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

2: If this instruction is executed on the TMR0 register (and where applicable, 'd' = 1), the prescaler will be cleared if assigned.

**3:** If the Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

4: Some instructions are two-word instructions. The second word of these instructions will be executed as a NOP unless the first word of the instruction retrieves the information embedded in these 16 bits. This ensures that all program memory locations have a valid instruction.

# 25.2.5 SPECIAL CONSIDERATIONS WITH MICROCHIP MPLAB<sup>®</sup> IDE TOOLS

The latest versions of Microchip's software tools have been designed to fully support the extended instruction set of the PIC18F2221/2321/4221/4321 family family of devices. This includes the MPLAB C18 C Compiler, MPASM Assembly language and MPLAB Integrated Development Environment (IDE).

When selecting a target device for software development, MPLAB IDE will automatically set default Configuration bits for that device. The default setting for the XINST Configuration bit is '0', disabling the extended instruction set and Indexed Literal Offset Addressing mode. For proper execution of applications developed to take advantage of the extended instruction set, XINST must be set during programming.

To develop software for the extended instruction set, the user must enable support for the instructions and the Indexed Addressing mode in their language tool(s). Depending on the environment being used, this may be done in several ways:

- A menu option, or dialog box within the environment, that allows the user to configure the language tool and its settings for the project
- A command line option
- · A directive in the source code

These options vary between different compilers, assemblers and development environments. Users are encouraged to review the documentation accompanying their development systems for the appropriate information.





NOTES:

# 28-Lead Plastic Small Outline (SO) – Wide, 7.50 mm Body [SOIC]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging









	Units	MILLIMETERS				
Dimensi	ion Limits	MIN	NOM	MAX		
Number of Pins	Ν	28				
Pitch	е	1.27 BSC				
Overall Height	Α	-	-	2.65		
Molded Package Thickness	A2	2.05	-	-		
Standoff §	A1	0.10	-	0.30		
Overall Width	E	10.30 BSC				
Molded Package Width	E1	7.50 BSC				
Overall Length	D	17.90 BSC				
Chamfer (optional)	h	0.25	_	0.75		
Foot Length	L	0.40	-	1.27		
Footprint	L1	1.40 REF				
Foot Angle Top	φ	0°	_	8°		
Lead Thickness	С	0.18	-	0.33		
Lead Width	b	0.31	-	0.51		
Mold Draft Angle Top	α	5°	-	15°		
Mold Draft Angle Bottom	β	5° – 15°				

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. § Significant Characteristic.

3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.

4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-052B