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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I ² C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	4KB (2K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 10x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic18lf2221-i-ml

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Din Nome	Pi	n Numt	ber	Pin Buffer		Description			
	PDIP	QFN	TQFP	Туре	Туре	Description			
						PORTD is a bidirectional I/O port or a Parallel Slave Port (PSP) for interfacing to a microprocessor port. These pins have TTL input buffers when the PSP module is enabled.			
RD0/PSP0 RD0 PSP0	19	38	38	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.			
RD1/PSP1 RD1 PSP1	20	39	39	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.			
RD2/PSP2 RD2 PSP2	21	40	40	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.			
RD3/PSP3 RD3 PSP3	22	41	41	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.			
RD4/PSP4 RD4 PSP4	27	2	2	I/O I/O	ST TTL	Digital I/O. Parallel Slave Port data.			
RD5/PSP5/P1B RD5 PSP5 P1B	28	3	3	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. Enhanced CCP1 output.			
RD6/PSP6/P1C RD6 PSP6 P1C	29	4	4	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. Enhanced CCP1 output.			
RD7/PSP7/P1D RD7 PSP7 P1D	30	5	5	I/O I/O O	ST TTL	Digital I/O. Parallel Slave Port data. Enhanced CCP1 output.			
Legend: TTL = TTL c ST = Schm I^2C = ST wi	egend: TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = ST with I^2C^{TM} or SMB levels O = Output								

TABLE 1-3: PIC18F4221/4321 PINOUT I/O DESCRIPTIONS (CONTINUED)

Note 1: Default assignment for CCP2 when Configuration bit, CCP2MX, is set.

2: Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

3.7.1 OSCILLATOR CONTROL REGISTER

The OSCCON register (Register 3-2) controls several aspects of the device clock's operation, both in full power operation and in power-managed modes.

The System Clock Select bits, SCS<1:0>, select the clock source. The available clock sources are the primary clock (defined by the FOSC<3:0> Configuration bits), the secondary clock (Timer1 oscillator) and the internal oscillator block. The clock source changes immediately after either of the SCS<1:0> bits are changed, following a brief clock transition interval. The SCS bits are reset on all forms of Reset.

The Internal Oscillator Frequency Select bits (IRCF<2:0>) select the frequency output of the internal oscillator block to drive the device clock. The choices are the INTRC source (31 kHz), the INTOSC source (8 MHz) or one of the frequencies derived from the INTOSC postscaler (31.25 kHz to 4 MHz). If the internal oscillator block is supplying the device clock, changing the states of these bits will have an immediate change on the internal oscillator's output. On device Resets, the default output frequency of the internal oscillator block is set at 1 MHz.

When a nominal output frequency of 31 kHz is selected (IRCF<2:0> = 000), users may choose which internal oscillator acts as the source. This is done with the INTSRC bit in the OSCTUNE register (OSCTUNE<7>). Setting this bit selects INTOSC as a 31.25 kHz clock source derived from the INTOSC postscaler. Clearing INTSRC selects INTRC (nominally 31 kHz) as the clock source and disables the INTOSC to reduce current consumption.

This option allows users to select the tunable and more precise INTOSC as a clock source, while maintaining power savings with a very low clock speed. Additionally, the INTOSC source will already be stable should a switch to a higher frequency be needed quickly. Regardless of the setting of INTSRC, INTRC always remains the clock source for features such as the Watchdog Timer and the Fail-Safe Clock Monitor.

The OSTS, IOFS and T1RUN bits indicate which clock source is currently providing the device clock. The OSTS bit indicates that the Oscillator Start-up Timer and PLL Start-up Timer (if enabled) have timed out and the primary clock is providing the device clock in primary clock modes. The IOFS bit indicates when the internal oscillator block has stabilized and is providing the device clock in RC Clock modes. The T1RUN bit (T1CON<6>) indicates when the Timer1 oscillator is providing the device clock in secondary clock modes. In power-managed modes, only one of these three bits will be set at any time. If none of these bits are set, the INTRC is providing the clock or the internal oscillator block has just started and is not yet stable.

The IDLEN bit controls whether the device goes into Sleep mode or one of the Idle modes when the SLEEP instruction is executed.

The use of the flag and control bits in the OSCCON register is discussed in more detail in **Section 4.0** "**Power-Managed Modes**".

Note 1:	The Timer1 oscillator must be enabled to									
	select the secondary clock source. The									
	Timer1 oscillator is enabled by setting the									
	T1OSCEN bit in the Timer1 Control regis-									
	ter (T1CON<3>). If the Timer1 oscillator									
	is not enabled, then any attempt to select									
	a secondary clock source will be ignored.									
2:	It is recommended that the Timer1									

2: It is recommended that the Timer1 oscillator be operating and stable before selecting the secondary clock source or a very long delay may occur while the Timer1 oscillator starts.

3.7.2 OSCILLATOR TRANSITIONS

The PIC18F2221/2321/4221/4321 family of devices contains circuitry to prevent clock "glitches" when switching between clock sources. A short pause in the device clock occurs during the clock switch. The length of this pause is the sum of two cycles of the old clock source and three to four cycles of the new clock source. This formula assumes that the new clock source is stable.

Clock transitions are discussed in greater detail in **Section 4.1.2 "Entering Power-Managed Modes"**.

5.0 RESET

The PIC18F2221/2321/4221/4321 family devices differentiate between various kinds of Reset:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during power-managed modes
- d) Watchdog Timer (WDT) Reset (during execution)
- e) Programmable Brown-out Reset (BOR)
- f) RESET Instruction
- g) Stack Full Reset
- h) Stack Underflow Reset

This section discusses Resets generated by MCLR, POR and BOR and covers the operation of the various start-up timers. Stack Reset events are covered in Section 6.1.2.4 "Stack Full and Underflow Resets". WDT Resets are covered in Section 24.2 "Watchdog Timer (WDT)". A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 5-1.

5.1 RCON Register

Device Reset events are tracked through the RCON register (Register 5-1). The lower five bits of the register indicate that a specific Reset event has occurred. In most cases, these bits can only be cleared by the event and must be set by the application after the event. The state of these flag bits, taken together, can be read to indicate the type of Reset that just occurred. This is described in more detail in **Section 5.6 "Reset State of Registers"**.

The RCON register also has control bits for setting interrupt priority (IPEN) and software control of the BOR (SBOREN). Interrupt priority is discussed in Section 10.0 "Interrupts". BOR is covered in Section 5.4 "Brown-out Reset (BOR)".





6.2 PIC18 Instruction Cycle

6.2.1 CLOCKING SCHEME

The microcontroller clock input, whether from an internal or external source, is internally divided by four to generate four non-overlapping quadrature clocks (Q1, Q2, Q3 and Q4). Internally, the program counter is incremented on every Q1; the instruction is fetched from the program memory and latched into the Instruction Register (IR) during Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 6-3.

6.2.2 INSTRUCTION FLOW/PIPELINING

An "Instruction Cycle" consists of four Q cycles: Q1 through Q4. The instruction fetch and execute are pipelined in such a manner that a fetch takes one instruction cycle, while the decode and execute take another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO), then two cycles are required to complete the instruction (Example 6-3).

A fetch cycle begins with the Program Counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the Instruction Register (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3 and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).



FIGURE 6-3: CLOCK/INSTRUCTION CYCLE

EXAMPLE 6-3: INSTRUCTION PIPELINE FLOW

	Тсү0	TCY1	Tcy2	TCY3	TcY4	TCY5
1. MOVLW 55h	Fetch 1	Execute 1				
2. MOVWF PORTB		Fetch 2	Execute 2			
3. BRA SUB_1			Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (2	Forced NOP)			Fetch 4	Flush (NOP)	
5. Instruction @ addre	ss SUB_1				Fetch SUB_1	Execute SUB_1
All instructions are single is "flushed" from the pipel	cycle, except line while the	for any progra new instructio	im branches.∃ n is being feto	These take tw ched and then	o cycles since t executed.	the fetch instruction

6.3.5 STATUS REGISTER

The STATUS register, shown in Register 6-2, contains the arithmetic status of the ALU. As with any other SFR, it can be the operand for any instruction.

If the STATUS register is the destination for an instruction that affects the Z, DC, C, OV or N bits, the results of the instruction are not written; instead, the STATUS register is updated according to the instruction performed. Therefore, the result of an instruction with the STATUS register as its destination may be different than intended. As an example, CLRF STATUS will set the Z bit and leave the remaining Status bits unchanged ('000u u1uu'). It is recommended that only BCF, BSF, SWAPF, MOVFF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect the Z, C, DC, OV or N bits in the STATUS register.

For other instructions that do not affect Status bits, see the instruction set summaries in Table 24-2 and Table 24-3.

Note: The C and DC bits operate as the borrow and digit borrow bits, respectively, in subtraction.

REGISTER 6-2: STATUS REGISTER

	U-0	U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x					
		—	_	N	OV	Z	DC	С					
	bit 7							bit 0					
bit 7-5	Unimplen	nented: Read	d as '0'										
bit 4	N: Negativ	/e bit											
	This bit is negative (<i>i</i>	used for sign ALU MSB = 1	ed arithmeti	c (2's comp	lement). It ir	idicates whe	ther the res	ult was					
	1 = Result was negative 0 = Result was positive												
bit 3	OV: Overflow bit												
	This bit is used for signed arithmetic (2's complement). It indicates an overflow of the 7-bit magnitude which causes the sign bit (bit 7 of the result) to change state. 1 = Overflow occurred for signed arithmetic (in this arithmetic operation) 0 = No overflow occurred												
bit 2	Z: Zero bit	t											
	1 = The re 0 = The re	esult of an arit esult of an arit	thmetic or lo thmetic or lo	ogic operatio ogic operatio	n is zero n is not zero)							
bit 1	DC: Digit	Carry/borrow	bit										
	For ADDWE	F, ADDLW, SUE	BLW and SU	BWF instructi	ons:								
	1 = A carr 0 = No car	y-out from the rry-out from tl	e 4th Iow-or he 4th Iow-c	der bit of the order bit of th	e result occu ne result	rred							
	Note:	Note: For borrow, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either bit 4 or bit 3 of the source register.											
bit 0	C: Carry/b	orrow bit											
	For ADDWF, ADDLW, SUBLW and SUBWF instructions:												
	1 = A carr 0 = No car	 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred 											
	Note:	Note: For borrow, the polarity is reversed. A subtraction is executed by adding the 2's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low-order bit of the source register.											
	l egend:												
	R = Reada	able bit	W = W	/ritable bit	U = Unin	nplemented	bit, read as	'0'					

'1' = Bit is set

-n = Value at POR

x = Bit is unknown

'0' = Bit is cleared

12.3 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not directly readable or writable; its value is set by the PSA and T0PS<2:0> bits (T0CON<3:0>) which determine the prescaler assignment and prescale ratio.

Clearing the PSA bit assigns the prescaler to the Timer0 module. When it is assigned, prescale values from 1:2 through 1:256 in power-of-2 increments are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF TMR0, MOVWF TMR0, BSF TMR0, etc.) clear the prescaler count.

Note:	Writing to TMR0 when the prescaler is
	assigned to Timer0 will clear the prescaler
	count but will not change the prescaler
	assignment.

12.3.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control and can be changed "on-the-fly" during program execution.

12.4 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or from FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF flag bit. The interrupt can be masked by clearing the TMR0IE bit (INTCON<5>). Before reenabling the interrupt, the TMR0IF bit must be cleared in software by the Interrupt Service Routine.

Since Timer0 is shut down in Sleep mode, the TMR0 interrupt cannot awaken the processor from Sleep.

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page	
TMR0L	Timer0 Register Low Byte									
TMR0H	Timer0 Register High Byte									
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55	
TOCON	TMR0ON	T08BIT	TOCS	T0SE	PSA	T0PS2	T0PS1	T0PS0	56	
TRISA	RA7 ⁽¹⁾	RA6 ⁽¹⁾	RA5	RA4	RA3	RA2	RA1	RA0	58	

 TABLE 12-1:
 REGISTERS ASSOCIATED WITH TIMER0

Legend: Shaded cells are not used by Timer0.

Note 1: PORTA<7:6> and their direction bits are individually configured as port pins based on various primary oscillator modes. When disabled, these bits read as '0'.

13.3.3 TIMER1 OSCILLATOR LAYOUT CONSIDERATIONS

The Timer1 oscillator circuit draws very little power during operation. Due to the low-power nature of the oscillator, it may also be sensitive to rapidly changing signals in close proximity.

The oscillator circuit, shown in Figure 13-3, should be located as close as possible to the microcontroller. There should be no circuits passing within the oscillator circuit boundaries other than Vss or VDD.

If a high-speed circuit must be located near the oscillator (such as the CCP1 pin in Output Compare or PWM mode, or the primary oscillator using the OSC2 pin), a grounded guard ring around the oscillator circuit, as shown in Figure 13-4, may be helpful when used on a single-sided PCB or in addition to a ground plane.

FIGURE 13-4: OSCILLATOR CIRCUIT WITH GROUNDED GUARD RING



13.4 Timer1 Interrupt

The TMR1 register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The Timer1 interrupt, if enabled, is generated on overflow which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled or disabled by setting or clearing the Timer1 Interrupt Enable bit, TMR1IE (PIE1<0>).

13.5 Resetting Timer1 Using the CCP Special Event Trigger

If either of the CCP modules is configured to use Timer1 and generate a Special Event Trigger in Compare mode (CCP1M<3:0> or CCP2M<3:0> = 1011), this signal will reset Timer1. The trigger from CCP2 will also start an A/D conversion if the A/D module is enabled (see **Section 16.3.4 "Special Event Trigger"** for more information).

The module must be configured as either a timer or a synchronous counter to take advantage of this feature. When used this way, the CCPRH:CCPRL register pair effectively becomes a period register for Timer1.

If Timer1 is running in Asynchronous Counter mode, this Reset operation may not work.

In the event that a write to Timer1 coincides with a Special Event Trigger, the write operation will take precedence.

Note:	The Special Event Triggers from the
	CCP2 module will not set the TMR1IF
	interrupt flag bit (PIR1<0>).

13.6 Using Timer1 as a Real-Time Clock

Adding an external LP oscillator to Timer1 (such as the one described in **Section 13.3 "Timer1 Oscillator**") gives users the option to include RTC functionality to their applications. This is accomplished with an inexpensive watch crystal to provide an accurate time base and several lines of application code to calculate the time. When operating in Sleep mode and using a battery or supercapacitor as a power source, it can completely eliminate the need for a separate RTC device and battery backup.

The application code routine, RTCisr, shown in Example 13-1, demonstrates a simple method to increment a counter at one-second intervals using an Interrupt Service Routine. Incrementing the TMR1 register pair to overflow, triggers the interrupt and calls the routine, which increments the seconds counter by one. Additional counters for minutes and hours are incremented as the previous counter overflow.

Since the register pair is 16 bits wide, counting up to overflow the register directly from a 32.768 kHz clock would take 2 seconds. To force the overflow at the required one-second intervals, it is necessary to preload it. The simplest method is to set the MSb of TMR1H with a BSF instruction. Note that the TMR1L register is never preloaded or altered. Doing so may introduce cumulative errors over many cycles.

For this method to be accurate, Timer1 must operate in Asynchronous mode and the Timer1 overflow interrupt must be enabled (PIE1<0> = 1), as shown in the routine, RTCinit. The Timer1 oscillator must also be enabled and running at all times.

NOTES:

NOTES:

17.0 ENHANCED CAPTURE/ COMPARE/PWM (ECCP) MODULE

Note:	The ECCP module is implemented only in
	40/44-pin devices.

In PIC18F4221/4321 devices, CCP1 is implemented as a standard CCP module with Enhanced PWM capabilities. These include the provision for 2 or 4 output channels, user-selectable polarity, dead-band control and automatic shutdown and restart. The Enhanced features are discussed in detail in **Section 17.4 "Enhanced PWM Mode"**. Capture, Compare and single-output PWM functions of the ECCP module are the same as described for the standard CCP module.

The control register for the Enhanced CCP module is shown in Register 17-1. It differs from the CCPxCON registers in PIC18F2221/2321 devices in that the two Most Significant bits are implemented to control PWM functionality.

REGISTER 17-1: CCP1CON REGISTER (ECCP1 MODULE, 40/44-PIN DEVICES)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
P1M1	P1M0	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0
bit 7							bit 0

bit 7-6 P1M<1:0>: Enhanced PWM Output Configuration bits

If CCP1M<3:2> = 00, 01, 10:

xx = P1A assigned as Capture/Compare input/output; P1B, P1C, P1D assigned as port pins
If CCP1M<3:2> = 11:

- 00 = Single output: P1A modulated; P1B, P1C, P1D assigned as port pins
- 01 = Full-bridge output forward: P1D modulated; P1A active; P1B, P1C inactive
- 10 = Half-bridge output: P1A, P1B modulated with dead-band control; P1C, P1D assigned as port pins
- 11 = Full-bridge output reverse: P1B modulated; P1C active; P1A, P1D inactive
- bit 5-4 **DC1B<1:0>**: PWM Duty Cycle bit 1 and bit 0

Capture mode:

Unused.

Compare mode:

Unused.

PWM mode:

These bits are the two LSbs of the 10-bit PWM duty cycle. The eight MSbs of the duty cycle are found in CCPR1L.

bit 3-0 **CCP1M<3:0>**: Enhanced CCP Mode Select bits

- 0000 = Capture/Compare/PWM off (resets ECCP module)
- 0001 = Reserved
- 0010 = Compare mode, toggle output on match
- 0011 = Capture mode
- 0100 = Capture mode, every falling edge
- 0101 = Capture mode, every rising edge
- 0110 = Capture mode, every 4th rising edge
- 0111 = Capture mode, every 16th rising edge
- 1000 = Compare mode, initialize CCP1 pin low, set output on compare match (set CCP1IF)
- 1001 = Compare mode, initialize CCP1 pin high, clear output on compare match (set CCP1IF)
- 1010 = Compare mode, generate software interrupt only, CCP1 pin reverts to I/O state
- 1011 = Compare mode, trigger special event (ECCP resets TMR1 or TMR3, sets CC1IF bit)
- 1100 = PWM mode; P1A, P1C active-high; P1B, P1D active-high
- 1101 = PWM mode; P1A, P1C active-high; P1B, P1D active-low
- 1110 = PWM mode; P1A, P1C active-low; P1B, P1D active-high
- 1111 = PWM mode; P1A, P1C active-low; P1B, P1D active-low

Legend:					
R = Readable bit	W = Writable bit U = Unimplemented bit, read as '0'				
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown		

17.4.4 HALF-BRIDGE MODE

In the Half-Bridge Output mode, two pins are used as outputs to drive push-pull loads. The PWM output signal is output on the P1A pin, while the complementary PWM output signal is output on the P1B pin (Figure 17-4). This mode can be used for half-bridge applications, as shown in Figure 17-5, or for full-bridge applications where four power switches are being modulated with two PWM signals.

In Half-Bridge Output mode, the programmable deadband delay can be used to prevent shoot-through current in half-bridge power devices. The value of bits, PDC<6:0>, sets the number of instruction cycles before the output is driven active. If the value is greater than the duty cycle, the corresponding output remains inactive during the entire cycle. See **Section 17.4.6 "Programmable Dead-Band Delay"** for more details of the dead-band delay operations.

Since the P1A and P1B outputs are multiplexed with the PORTC<2> and PORTD<5> data latches, the TRISC<2> and TRISD<5> bits must be cleared to configure P1A and P1B as outputs.

FIGURE 17-4: HALF-BRIDGE PWM



FIGURE 17-5: EXAMPLES OF HALF-BRIDGE OUTPUT MODE APPLICATIONS



FIGURE 18-5:	SPI N	IODE W	/AVEFO	RM (SL	AVE MC	DE WIT	H CKE :	= 0)			
- SS Opäend	• • •										
940R (C242P = 0											
- CBASS # 30) - SACK	: 4		· · ·	· · ·		· ·		· : : ······			3 3
(ONA + 1 OKE + 0)	: : :										
Write to SSPSUF		•	2 2 2 2	: : : :	e Garana E E	•	2 2 2	· 	(*
9870		K 158 V	 X	X 58.6		×68.3	X 68.0			<u>(3</u> 3-6)	
809 (9849 = 0)	· · · · ·										* 1
inguja Samagoiae	- - - 		, , , , , , , , , , , , , , , , , , , ,	. 49.						a.	
(68892 # 0) 6582999 100800896 20820896	: : :		- 5 5 5 5	e • • • •	- 5 5 6 6	: :	· 5 5 5 5	, , ; ;			
SSPSR 5 SSPSLF	, , 6	• • •)) //////////////////////////////////	: : 	t t 5	• • •) ; ,	: : · · · · · · · · · · · · · · · · · ·		2002 (22 2022 (22 2023 (22	n yayoker Ta

FIGURE 18-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)





19.2 EUSART Asynchronous Mode

The Asynchronous mode of operation is selected by clearing the SYNC bit (TXSTA<4>). In this mode, the EUSART uses standard Non-Return-to-Zero (NRZ) format (one Start bit, eight or nine data bits and one Stop bit). The most common data format is 8 bits. An on-chip dedicated 8-bit/16-bit Baud Rate Generator can be used to derive standard baud rate frequencies from the oscillator.

The EUSART transmits and receives the LSb first. The EUSART's transmitter and receiver are functionally independent but use the same data format and baud rate. The Baud Rate Generator produces a clock, either x16 or x64 of the bit shift rate depending on the BRGH and BRG16 bits (TXSTA<2> and BAUDCON<3>). Parity is not supported by the hardware but can be implemented in software and stored as the 9th data bit.

The TXCKP (BAUDCON<4>) and RXDTP (BAUDCON<5>) bits allow the TX and RX signals to be inverted (polarity reversed). Devices that buffer signals between TTL and RS-232 levels also invert the signal. Setting the TXCKP and RXDTP bits allows for the use of circuits that provide buffering without inverting the signal.

In Asynchronous mode, clock polarity is selected with the TXCKP bit (BAUDCON<4>). Setting TXCKP sets the Idle state on CK as high, while clearing the bit sets the Idle state as Iow. Data polarity is selected with the RXDTP bit (BAUDCON<5>). Setting RXDTP inverts data on RX, while clearing the bit has no affect on received data.

When operating in Asynchronous mode, the EUSART module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver
- Auto-Wake-up on Break signal
- 12-bit Break Character Transmit
- Auto-Baud Rate Detection
- · Pin State Polarity

19.2.1 EUSART ASYNCHRONOUS TRANSMITTER

The EUSART transmitter block diagram is shown in Figure 19-3. The heart of the transmitter is the Transmit (Serial) Shift Register (TSR). The Shift register obtains its data from the Read/Write Transmit Buffer register, TXREG. The TXREG register is loaded with data in software. The TSR register is not loaded until the Stop bit has been transmitted from the previous load. As soon as the Stop bit is transmitted, the TSR is loaded with new data from the TXREG register (if available).

Once the TXREG register transfers the data to the TSR register (occurs in one TCY), the TXREG register is empty and the TXIF flag bit (PIR1<4>) is set. This interrupt can be enabled or disabled by setting or clearing the interrupt enable bit, TXIE (PIE1<4>). TXIF will be set regardless of the state of TXIE; it cannot be cleared in software. TXIF is also not cleared immediately upon loading TXREG, but becomes valid in the second instruction cycle following the load instruction. Polling TXIF immediately following a load of TXREG will return invalid results.

While TXIF indicates the status of the TXREG register, another bit, TRMT (TXSTA<1>), shows the status of the TSR register. TRMT is a read-only bit which is set when the TSR register is empty. No interrupt logic is tied to this bit so the user has to poll this bit in order to determine if the TSR register is empty.

The TXCKP bit (BAUDCON<4>) allows the TX signal to be inverted (polarity reversed). Devices that buffer signals from TTL to RS-232 levels also invert the signal (when TTL = 1, RS-232 = negative). Inverting the polarity of the TX pin data by setting the TXCKP bit allows for use of circuits that provide buffering without inverting the signal.

Note 1: The TSR register is not mapped in data memory so it is not available to the user.2: Flag bit TXIF is set when enable bit TXEN is set.

To set up an Asynchronous Transmission:

- 1. Initialize the SPBRGH:SPBRG registers for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
- 2. Enable the asynchronous serial port by clearing bit, SYNC, and setting bit, SPEN.
- 3. If the signal from the TX pin is to be inverted, set the TXCKP bit.
- 4. If interrupts are desired, set enable bit, TXIE.
- 5. If 9-bit transmission is desired, set transmit bit, TX9; can be used as address/data bit.
- 6. Enable the transmission by setting bit, TXEN, which will also set bit, TXIF.
- 7. If 9-bit transmission is selected, the ninth bit should be loaded in bit, TX9D.
- 8. Load data to the TXREG register (starts transmission).
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

BRA		Unconditional Branch					
Syntax:		BRA n					
Operands:		$-1024 \le n \le 1$	023				
Oper	ation:	(PC) + 2 + 2n	\rightarrow PC				
Statu	s Affected:	None					
Enco	ding:	1101	0nnn nnnr		nnnn		
Description:		Add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC + 2 + 2n. This instruction is a two-cycle instruction.					
Words:		1					
Cycles:		2					
Q Cycle Activity:							
	Q1	Q2	(23	Q4		
	Decode	Read literal 'n'	Pro D	cess ata	Write to PC		
	No operation	No operation	۱ opei	No ration	No operation		
Exam	<u>nple:</u>	HERE	BRA	Jump			
	Before Instruc PC After Instructi	ction = ac on	dress	(HERE)			
	PC	= ac	dress	(Jump)			

BSF		Bit Set f						
Syntax:		BSF f, b	{,a}					
Operands:		0 ≤ f ≤ 255 0 ≤ b ≤ 7 a ∈ [0,1]	$0 \le f \le 255$ $0 \le b \le 7$ $a \in [0, 1]$					
Oper	ation:	$1 \rightarrow \text{f}$	1 → f 					
Statu	is Affected:	None						
Enco	oding:	1000	bbba	ffff	ffff			
Description:		Bit 'b' in re If 'a' is '0', ' If 'a' is '1', 1 GPR bank If 'a' is '0' a set is enab in Indexed mode when Section 25 Bit-Orienta Literal Off	Bit 'b' in register 'f' is set. If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default). If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever $f \le 95$ (5Fh). See Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode" for details					
Word	ls:	1						
Cycle	es:	1	1					
QC	ycle Activity:							
	Q1	Q2	Q3		Q4			
Decode		Read register 'f'	Read Process register 'f' Data		Write egister 'f'			
<u>Exan</u>	nple:	BSF 1	FLAG_RE	G, 7, 1				
	Before Instruction FLAG_REG = 0Ah After Instruction FLAG REG = 8Ah							

27.2 DC Characteristics: Power-Down and Supply Current PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

PIC18LF2221/2321/4221/4321 (Industrial)		Standard Operating Conditions (unless otherwise stated)Operating temperature $-40^{\circ}C \le TA \le +85^{\circ}C$ for industrial					
PIC18F2221/2321/4221/4321 (Industrial, Extended)		$\begin{array}{l} \mbox{Standard Operating Conditions (unless otherwise stated)} \\ \mbox{Operating temperature} & -40^{\circ}C \leq TA \leq +85^{\circ}C \mbox{ for industrial} \\ -40^{\circ}C \leq TA \leq +125^{\circ}C \mbox{ for extended} \end{array}$					
Param Device		Тур	Max	Units	Conditions		
	Supply Current (IDD) ⁽²⁾						
	PIC18LF2X21/4X21	0.69	0.9	mA	-40°C		
		0.70	0.9	mA	+25°C	VDD = 2.0V	Fosc = 4 MHz (RC_RUN mode, INTOSC source)
		0.71	0.9	mA	+85°C]	
	PIC18LF2X21/4X21	1.17	1.45	mA	-40°C		
		1.15	1.45	mA	+25°C	VDD = 3.0V VDD = 5.0V	
		1.14	1.45	mA	+85°C		
	All Devices	2.24	2.9	mA	-40°C		
		2.20	2.9	mA	+25°C		
		2.16	2.8	mA	+85°C		
	Extended Devices Only	2.18	2.8	mA	+125°C		
	PIC18LF2X21/4X21	3	5	μA	-40°C		
		3	5	μA	+25°C	VDD = 2.0V	
		3	5.6	μA	+85°C	VDD = 3.0V	
	PIC18LF2X21/4X21	4	7	μA	-40°C		Fosc = 31 kHz
		5	7	μA	+25°C		
		5	10	μA	+85°C		INTRC source)
	All Devices	10	12	μA	-40°C		
		10	12	μA	+25°C		
		10	16	μΑ	+85°C	VDD - 5.0V	
	Extended Devices Only	17	50	μA	+125°C		

Legend: Shading of rows is to assist in readability of the table.

Note 1: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to VDD or VSS, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR, etc.).

2: The supply current is mainly a function of operating voltage, frequency and mode. Other factors, such as I/O pin loading and switching rate, oscillator type and circuit, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD or VSS;

MCLR = VDD; WDT enabled/disabled as specified.

3: Low-power, Timer1 oscillator is selected unless otherwise indicated, where LPT1OSC (CONFIG3H<2>) = 1.

4: BOR and HLVD enable internal band gap reference. With both modules enabled, current consumption will be less than the sum of both specifications.

5: When operation below -10°C is expected, use T1OSC High-Power mode, where LPT1OSC (CONFIG3H<2>) = 0.

28.0 PACKAGING INFORMATION

28.1 Package Marking Information

28-Lead SPDIP



28-Lead SOIC



28-Lead QFN



28-Lead SSOP





Example



Example



Example



Legend	: XXX Y YY WW NNN @3 *	Customer-specific information Year code (last digit of calendar year) Year code (last 2 digits of calendar year) Week code (week of January 1 is week '01') Alphanumeric traceability code Pb-free JEDEC designator for Matte Tin (Sn) This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.	
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.		

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Features	PIC18F2221	PIC18F2321	PIC18F4221	PIC18F4321
Program Memory (Bytes)	4096	8192	4096	8192
Program Memory (Instructions)	2048	4096	2048	4096
Interrupt Sources	19	19	20	20
I/O Ports	Ports A, B, C, (E)	Ports A, B, C, (E)	Ports A, B, C, D, E	Ports A, B, C, D, E
Capture/Compare/PWM Modules	2	2	1	1
Enhanced Capture/Compare/ PWM Modules	0	0	1	1
Parallel Communications (PSP)	No	No	Yes	Yes
10-Bit Analog-to-Digital Module	10 input channels	10 input channels	13 input channels	13 input channels
Packages	28-pin SPDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	28-pin SPDIP 28-pin SOIC 28-pin SSOP 28-pin QFN	40-pin PDIP 44-pin TQFP 44-pin QFN	40-pin PDIP 44-pin TQFP 44-pin QFN

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PIC18F2221/2321/4221/4321 PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	x <u>xx</u> xxx	Examples:
Device	Temperature Package Pattern Range	 a) PIC18F4321-I/P 301 = Industrial temp., PDIP package, Extended VDD limits, QTP pattern #301. b) PIC18LF2321-I/SO = Industrial temp., SOIC
Device	PIC18F2221/2321 ⁽¹⁾ , PIC18F4221/4321 ⁽¹⁾ , PIC18F2221/2321T ⁽²⁾ , PIC18F4221/4321T ⁽²⁾ ; VDD range 4.2V to 5.5V PIC18LF2221/2321 ⁽¹⁾ , PIC18LF4221/4321 ⁽¹⁾ , PIC18LF2221/2321T ⁽²⁾ , PIC18LF4221/4321T ⁽²⁾ ; VDD range 2.0V to 5.5V	 package, Extended VDD limits. c) PIC18LF4321-I/P = Industrial temp., PDIP package, normal VDD limits.
Temperature Range	I = -40° C to $+85^{\circ}$ C (Industrial) E = -40° C to $+125^{\circ}$ C (Extended)	
Package	PT = TQFP (Thin Quad Flatpack) SO = SOIC SS = SSOP SP = Skinny Plastic DIP P = PDIP ML = QFN	 Note 1: F = Standard Voltage Range LF = Wide Voltage Range 2: T = in tape and reel
Pattern	QTP, SQTP, Code or Special Requirements (blank otherwise)	