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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	40MHz
Connectivity	I <sup>2</sup> C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, HLVD, POR, PWM, WDT
Number of I/O	36
Program Memory Size	8KB (4K x 16)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	512 x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 5.5V
Data Converters	A/D 13x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4321t-i-pt">https://www.e-xfl.com/product-detail/microchip-technology/pic18lf4321t-i-pt</a>

# PIC18F2221/2321/4221/4321 FAMILY

**TABLE 1-2: PIC18F2221/2321 PINOUT I/O DESCRIPTIONS**

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	SPDIP, SOIC, SSOP	QFN			
MCLR/VPP/RE3 MCLR  VPP RE3	1	26	I  P I	ST  ST	Master Clear (input) or programming voltage (input). Master Clear (Reset) input. This pin is an active-low Reset to the device. Programming voltage input. Digital input.
OSC1/CLKI/RA7 OSC1  CLKI  RA7	9	6	I  I  I/O	Analog  CMOS  TTL	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode; CMOS otherwise. External clock source input. Always associated with pin function OSC1. (See related OSC1/CLKI, OSC2/CLKO pins.) General purpose I/O pin.
OSC2/CLKO/RA6 OSC2  CLKO  RA6	10	7	O  O  I/O	—  —  TTL	Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC, EC and INTIO modes, OSC2 pin outputs CLKO which has one-fourth the frequency of OSC1 and denotes the instruction cycle rate. General purpose I/O pin.

**Legend:** TTL = TTL compatible input      CMOS = CMOS compatible input or output  
ST = Schmitt Trigger input with CMOS levels      I = Input      P = Power  
I<sup>2</sup>C = ST with I<sup>2</sup>C™ or SMB levels      O = Output

**Note 1:** Default assignment for CCP2 when Configuration bit, CCP2MX, is set.  
**2:** Alternate assignment for CCP2 when Configuration bit, CCP2MX, is cleared.

# PIC18F2221/2321/4221/4321 FAMILY

## 2.4 ICSP Pins

The PGC and PGD pins are used for In-Circuit Serial Programming (ICSP) and debugging purposes. It is recommended to keep the trace length between the ICSP connector and the ICSP pins on the device as short as possible. If the ICSP connector is expected to experience an ESD event, a series resistor is recommended, with the value in the range of a few tens of ohms, not to exceed 100Ω.

Pull-up resistors, series diodes and capacitors on the PGC and PGD pins are not recommended as they will interfere with the programmer/debugger communications to the device. If such discrete components are an application requirement, they should be removed from the circuit during programming and debugging. Alternatively, refer to the AC/DC characteristics and timing requirements information in the respective device Flash programming specification for information on capacitive loading limits and pin input voltage high ( $V_{IH}$ ) and input low ( $V_{IL}$ ) requirements.

For device emulation, ensure that the “Communication Channel Select” (i.e., PGC/PGD pins) programmed into the device matches the physical connections for the ICSP to the MPLAB® ICD 2, MPLAB ICD 3 or REAL ICE™ emulator.

For more information on the ICD 2, ICD 3 and REAL ICE emulator connection requirements, refer to the following documents that are available on the Microchip web site.

- “MPLAB® ICD 2 In-Circuit Debugger User’s Guide” (DS51331)
- “Using MPLAB® ICD 2” (poster) (DS51265)
- “MPLAB® ICD 2 Design Advisory” (DS51566)
- “Using MPLAB® ICD 3” (poster) (DS51765)
- “MPLAB® ICD 3 Design Advisory” (DS51764)
- “MPLAB® REAL ICE™ In-Circuit Emulator User’s Guide” (DS51616)
- “Using MPLAB® REAL ICE™ In-Circuit Emulator” (poster) (DS51749)

## 2.5 External Oscillator Pins

Many microcontrollers have options for at least two oscillators: a high-frequency primary oscillator and a low-frequency secondary oscillator (refer to **Section 3.0 “Oscillator Configurations”** for details).

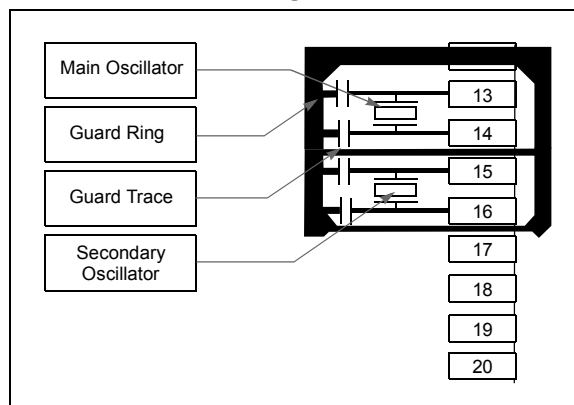
The oscillator circuit should be placed on the same side of the board as the device. Place the oscillator circuit close to the respective oscillator pins with no more than 0.5 inch (12 mm) between the circuit components and the pins. The load capacitors should be placed next to the oscillator itself, on the same side of the board.

Use a grounded copper pour around the oscillator circuit to isolate it from surrounding circuits. The grounded copper pour should be routed directly to the MCU ground. Do not run any signal traces or power traces inside the ground pour. Also, if using a two-sided board, avoid any traces on the other side of the board where the crystal is placed. A suggested layout is shown in Figure 2-3.

For additional information and design guidance on oscillator circuits, please refer to these Microchip Application Notes, available at the corporate web site ([www.microchip.com](http://www.microchip.com)):

- AN826, “Crystal Oscillator Basics and Crystal Selection for rPIC™ and PICmicro® Devices”
- AN849, “Basic PICmicro® Oscillator Design”
- AN943, “Practical PICmicro® Oscillator Analysis and Design”
- AN949, “Making Your Oscillator Work”

**FIGURE 2-3: SUGGESTED PLACEMENT OF THE OSCILLATOR CIRCUIT**



## 2.6 Unused I/Os

Unused I/O pins should be configured as outputs and driven to a logic low state. Alternatively, connect a 1 kΩ to 10 kΩ resistor to Vss on unused pins and drive the output to logic low.

# PIC18F2221/2321/4221/4321 FAMILY

## 5.4 Brown-out Reset (BOR)

PIC18F2221/2321/4221/4321 family devices implement a BOR circuit that provides the user with a number of configuration and power-saving options. The BOR is controlled by the BORV<1:0> and BOREN<1:0> Configuration bits. There are a total of four BOR configurations which are summarized in Table 5-1.

The BOR threshold is set by the BORV<1:0> bits. If BOR is enabled (any values of BOREN<1:0>, except '00'), any drop of VDD below VBOR (parameter D005) for greater than TBOR (parameter 35) will reset the device. A Reset may or may not occur if VDD falls below VBOR for less than TBOR. The chip will remain in Brown-out Reset until VDD rises above VBOR.

If the Power-up Timer is enabled, it will be invoked after VDD rises above VBOR; it then will keep the chip in Reset for an additional time delay, TPWRT (parameter 33). If VDD drops below VBOR while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above VBOR, the Power-up Timer will execute the additional time delay.

BOR and the Power-on Timer (PWRT) are independently configured. Enabling BOR Reset does not automatically enable the PWRT.

### 5.4.1 SOFTWARE ENABLED BOR

When BOREN<1:0> = 01, the BOR can be enabled or disabled by the user in software. This is done with the control bit, SBOREN (RCON<6>). Setting SBOREN enables the BOR to function as previously described. Clearing SBOREN disables the BOR entirely. The SBOREN bit operates only in this mode; otherwise it is read as '0'.

Placing the BOR under software control gives the user the additional flexibility of tailoring the application to its environment without having to reprogram the device to

change BOR configuration. It also allows the user to tailor device power consumption in software by eliminating the incremental current that the BOR consumes. While the BOR current is typically very small, it may have some impact in low-power applications.

**Note:** Even when BOR is under software control, the Brown-out Reset voltage level is still set by the BORV<1:0> Configuration bits. It cannot be changed in software.

### 5.4.2 DETECTING BOR

When Brown-out Reset is enabled, the  $\overline{\text{BOR}}$  bit always resets to '0' on any Brown-out Reset or Power-on Reset event. This makes it difficult to determine if a Brown-out Reset event has occurred just by reading the state of BOR alone. A more reliable method is to simultaneously check the state of both  $\overline{\text{POR}}$  and  $\overline{\text{BOR}}$ . This assumes that the  $\overline{\text{POR}}$  bit is reset to '1' in software immediately after any Power-on Reset event. If  $\overline{\text{BOR}}$  is '0' while  $\overline{\text{POR}}$  is '1', it can be reliably assumed that a Brown-out Reset event has occurred.

### 5.4.3 DISABLING BOR IN SLEEP MODE

When BOREN<1:0> = 10, the BOR remains under hardware control and operates as previously described. Whenever the device enters Sleep mode, however, the BOR is automatically disabled. When the device returns to any other operating mode, BOR is automatically re-enabled.

This mode allows for applications to recover from brown-out situations, while actively executing code, when the device requires BOR protection the most. At the same time, it saves additional power in Sleep mode by eliminating the small incremental BOR current.

**TABLE 5-1: BOR CONFIGURATIONS**

BOR Configuration		Status of SBOREN (RCON<6>)	BOR Operation
BOREN1	BOREN0		
0	0	Unavailable	BOR disabled; must be enabled by reprogramming the Configuration bits.
0	1	Available	BOR enabled in software; operation controlled by SBOREN.
1	0	Unavailable	BOR enabled in hardware in Run and Idle modes, disabled during Sleep mode.
1	1	Unavailable	BOR enabled in hardware; must be disabled by reprogramming the Configuration bits.

# PIC18F2221/2321/4221/4321 FAMILY

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NOTES:

# PIC18F2221/2321/4221/4321 FAMILY

## 12.0 TIMER0 MODULE

The Timer0 module incorporates the following features:

- Software selectable operation as a timer or counter in both 8-bit or 16-bit modes
- Readable and writable registers
- Dedicated 8-bit, software programmable prescaler
- Selectable clock source (internal or external)
- Edge select for external clock
- Interrupt-on-overflow

The T0CON register (Register 12-1) controls all aspects of the module's operation, including the prescale selection. It is both readable and writable.

A simplified block diagram of the Timer0 module in 8-bit mode is shown in Figure 12-1. Figure 12-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

### REGISTER 12-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

- bit 7 **TMR0ON:** Timer0 On/Off Control bit  
1 = Enables Timer0  
0 = Stops Timer0
- bit 6 **T08BIT:** Timer0 8-Bit/16-Bit Control bit  
1 = Timer0 is configured as an 8-bit timer/counter  
0 = Timer0 is configured as a 16-bit timer/counter
- bit 5 **T0CS:** Timer0 Clock Source Select bit  
1 = Transition on T0CKI pin  
0 = Internal instruction cycle clock (CLKO)
- bit 4 **T0SE:** Timer0 Source Edge Select bit  
1 = Increment on high-to-low transition on T0CKI pin  
0 = Increment on low-to-high transition on T0CKI pin
- bit 3 **PSA:** Timer0 Prescaler Assignment bit  
1 = Timer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.  
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output.
- bit 2-0 **T0PS<2:0>:** Timer0 Prescaler Select bits  
111 = 1:256 Prescale value  
110 = 1:128 Prescale value  
101 = 1:64 Prescale value  
100 = 1:32 Prescale value  
011 = 1:16 Prescale value  
010 = 1:8 Prescale value  
001 = 1:4 Prescale value  
000 = 1:2 Prescale value

#### Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared    x = Bit is unknown

# PIC18F2221/2321/4221/4321 FAMILY

## 14.2 Timer2 Interrupt

Timer2 can also generate an optional device interrupt. The Timer2 output signal (TMR2 to PR2 match) provides the input for the 4-bit output counter/postscaler. This counter generates the TMR2 match interrupt flag which is latched in TMR2IF (PIR1<1>). The interrupt is enabled by setting the TMR2 Match Interrupt Enable bit, TMR2IE (PIE1<1>).

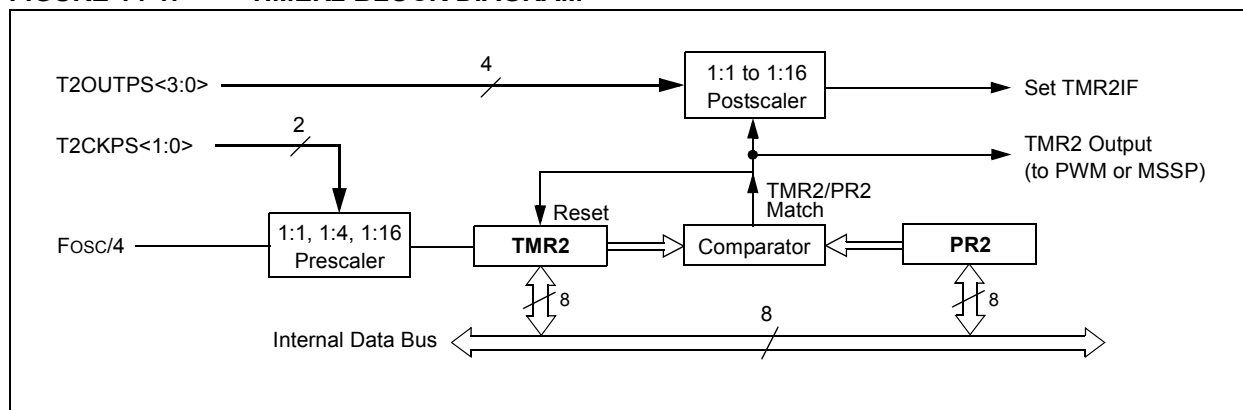
A range of 16 postscale options (from 1:1 through 1:16 inclusive) can be selected with the postscale control bits, T2OUTPS<3:0> (T2CON<6:3>).

## 14.3 Timer2 Output

The unscaled output of TMR2 is available primarily to the CCP modules, where it is used as a time base for operations in PWM mode.

Timer2 can be optionally used as the shift clock source for the MSSP module operating in SPI mode. Additional information is provided in **Section 18.0 “Master Synchronous Serial Port (MSSP) Module”**.

**FIGURE 14-1: TIMER2 BLOCK DIAGRAM**



**TABLE 14-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on page
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	55
PIR1	PSPIF <sup>(1)</sup>	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	58
PIE1	PSPIE <sup>(1)</sup>	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	58
IPR1	PSPIP <sup>(1)</sup>	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	58
TMR2	Timer2 Register								56
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	56
PR2	Timer2 Period Register								56

**Legend:** — = unimplemented, read as ‘0’. Shaded cells are not used by the Timer2 module.

**Note 1:** These bits are unimplemented on 28-pin devices and read as ‘0’.

# PIC18F2221/2321/4221/4321 FAMILY

## 18.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

### 18.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I<sup>2</sup>C™)
  - Full Master mode
  - Slave mode (with address masking for both 10-bit and 7-bit addressing)

The I<sup>2</sup>C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- Slave mode

### 18.2 Control Registers

The MSSP module has three associated registers. These include a status register (SSPSTAT) and two control registers (SSPCON1 and SSPCON2). The use of these registers and their individual Configuration bits differ significantly depending on whether the MSSP module is operated in SPI or I<sup>2</sup>C mode.

Additional details are provided under the individual sections.

### 18.3 SPI Mode

The SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. All four SPI modes are supported. To accomplish communication, typically three pins are used:

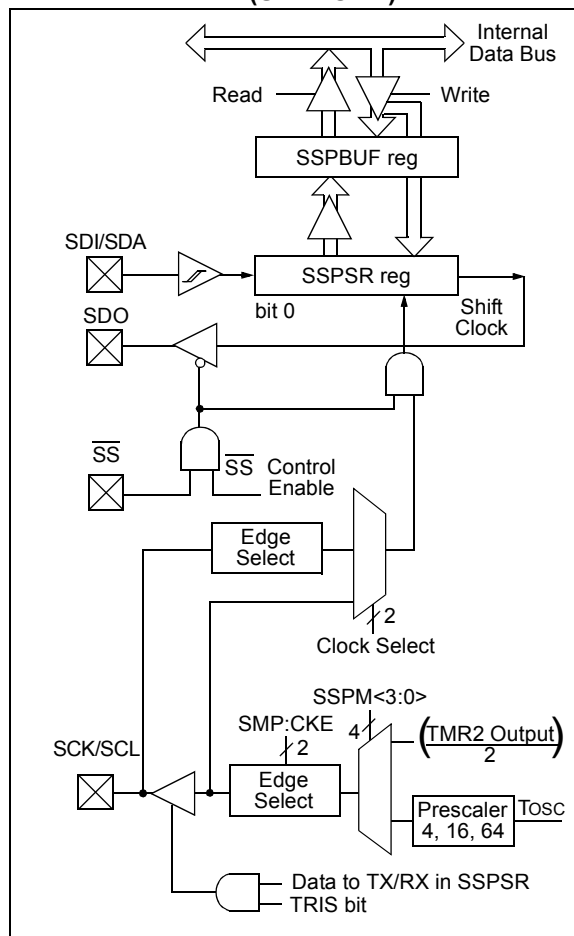
- Serial Data Out (SDO) – SDO
- Serial Data In (SDI) – SDI/SDA
- Serial Clock (SCK) – SCK/SCL

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select ( $\overline{SS}$ )

Figure 18-1 shows the block diagram of the MSSP module when operating in SPI mode.

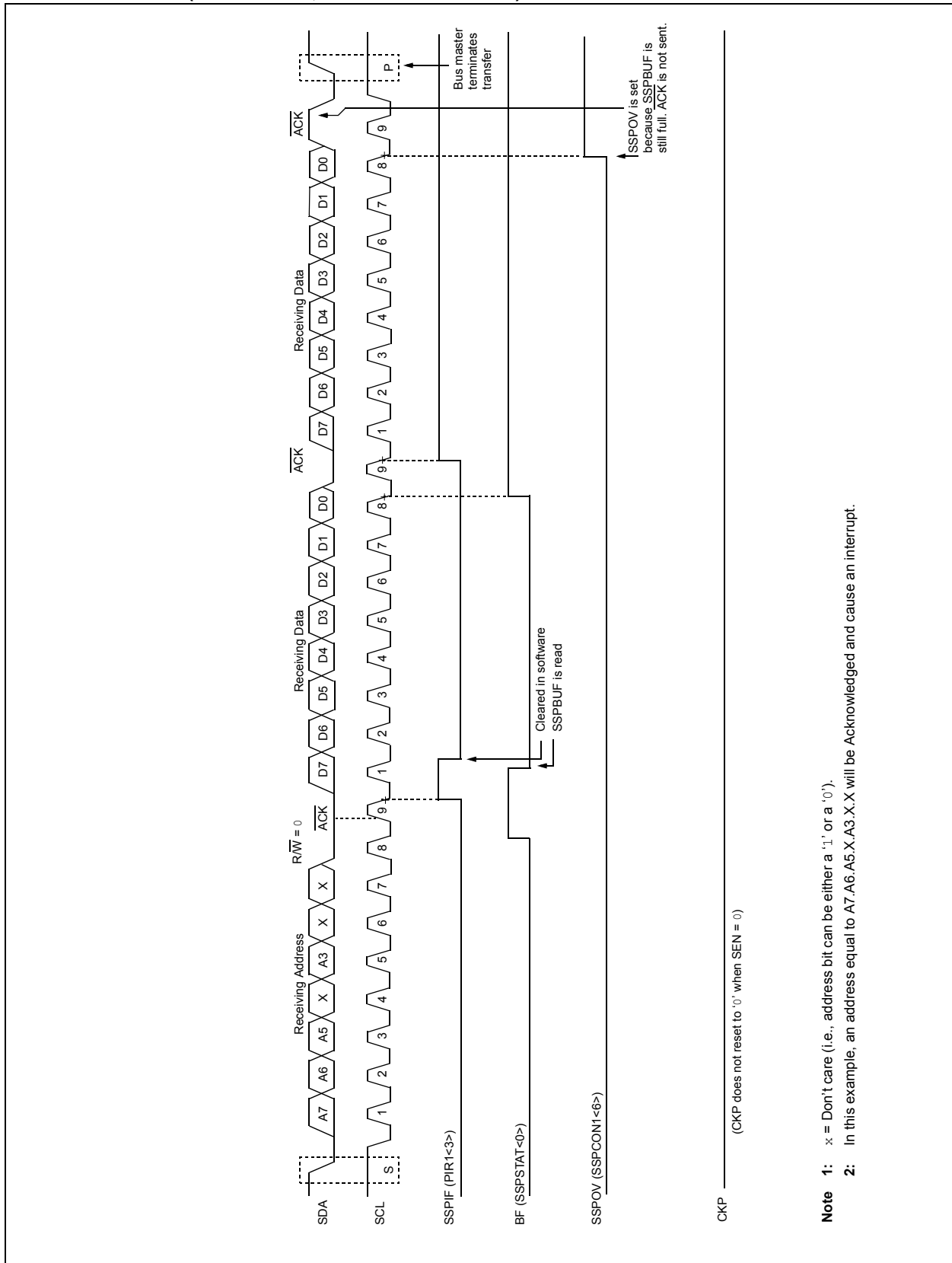
**FIGURE 18-1: MSSP BLOCK DIAGRAM (SPI MODE)**





# PIC18F2221/2321/4221/4321 FAMILY

**FIGURE 18-9: I<sup>2</sup>C™ SLAVE MODE TIMING WITH SEN = 0 AND ADMSK<5:1> = 01011 (RECEPTION, 7-BIT ADDRESSING)**



# PIC18F2221/2321/4221/4321 FAMILY

## 18.4.6 MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON1 and by setting the SSPEN bit. In Master mode, the SCL and SDA lines are manipulated by the MSSP hardware.

Master mode of operation is supported by interrupt generation on the detection of the Start and Stop conditions. The Stop (P) and Start (S) bits are cleared from a Reset or when the MSSP module is disabled. Control of the I<sup>2</sup>C bus may be taken when the P bit is set, or the bus is Idle, with both the S and P bits clear.

In Firmware Controlled Master mode, user code conducts all I<sup>2</sup>C bus operations based on Start and Stop bit conditions.

Once Master mode is enabled, the user has six options.

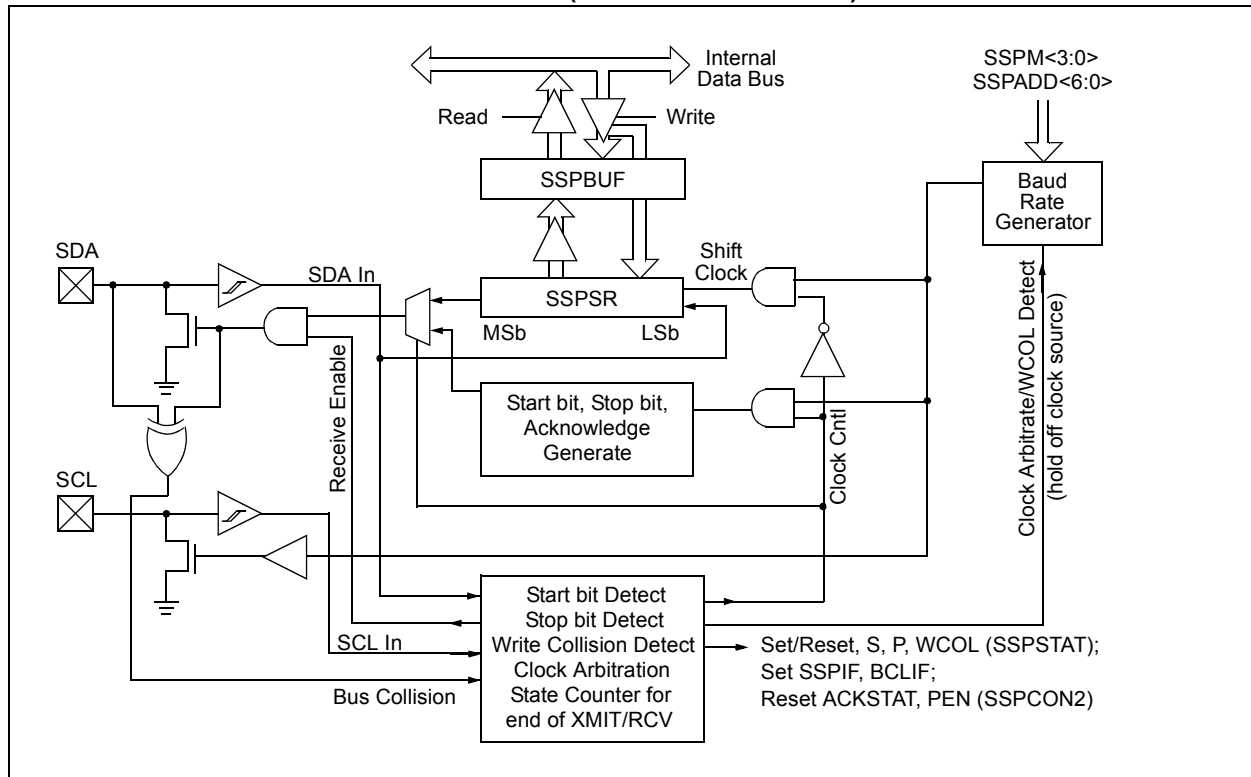
1. Assert a Start condition on SDA and SCL.
2. Assert a Repeated Start condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Configure the I<sup>2</sup>C port to receive data.
5. Generate an Acknowledge condition at the end of a received byte of data.
6. Generate a Stop condition on SDA and SCL.

**Note:** The MSSP module, when configured in I<sup>2</sup>C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a Start condition and immediately write the SSPBUF register to initiate transmission before the Start condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

The following events will cause the MSSP Interrupt Flag bit, SSPIF, to be set (MSSP interrupt, if enabled):

- Start condition
- Stop condition
- Data transfer byte transmitted/received
- Acknowledge transmit
- Repeated Start

**FIGURE 18-18: MSSP BLOCK DIAGRAM (I<sup>2</sup>C™ MASTER MODE)**





# PIC18F2221/2321/4221/4321 FAMILY

## 18.4.17.1 Bus Collision During a Start Condition

During a Start condition, a bus collision occurs if:

- SDA or SCL are sampled low at the beginning of the Start condition (Figure 18-28).
- SCL is sampled low before SDA is asserted low (Figure 18-29).

During a Start condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

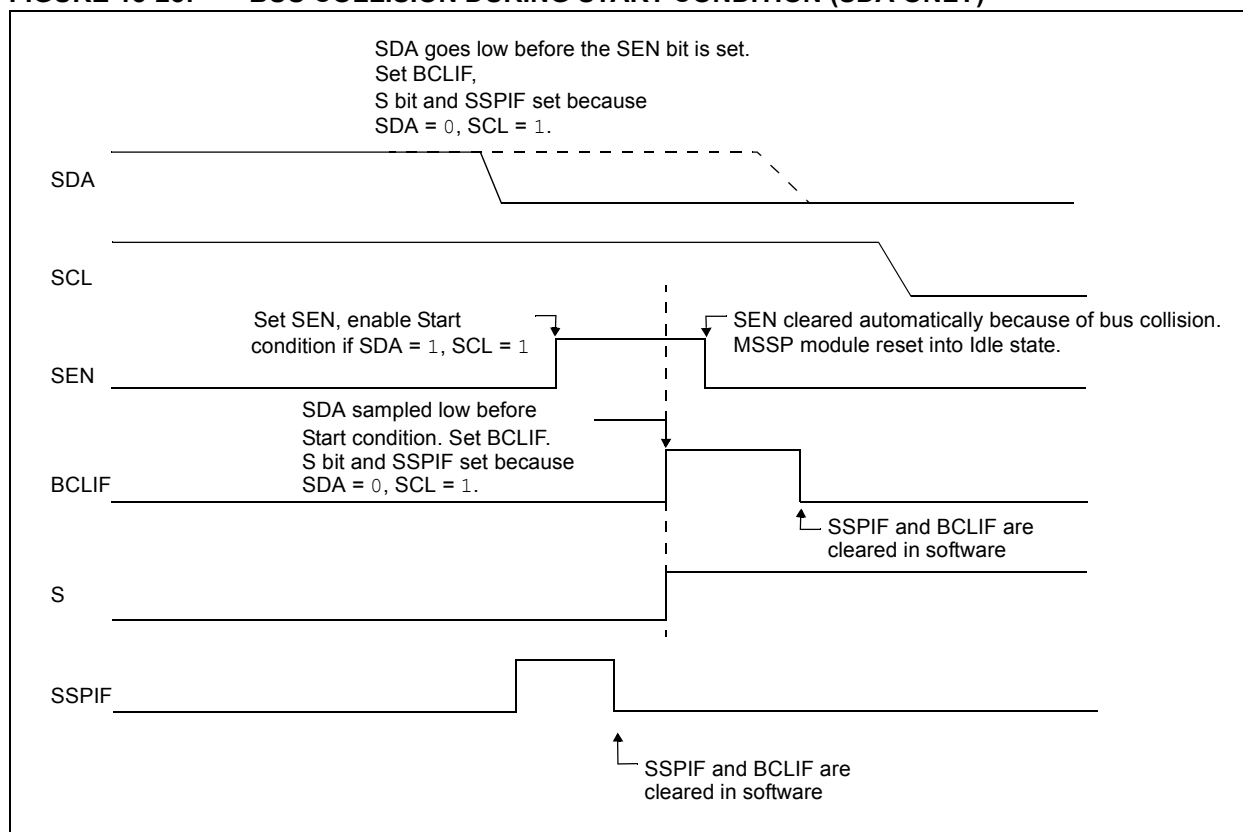
- the Start condition is aborted,
- the BCLIF flag is set and
- the MSSP module is reset to its Idle state (Figure 18-28).

The Start condition begins with the SDA and SCL pins deasserted. When the SDA pin is sampled high, the Baud Rate Generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs because it is assumed that another master is attempting to drive a data '1' during the Start condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 18-30). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The Baud Rate Generator is then reloaded and counts down to 0; if the SCL pin is sampled as '0' during this time, a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

**Note:** The reason that bus collision is not a factor during a Start condition is that no two bus masters can assert a Start condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision because the two masters must be allowed to arbitrate the first address following the Start condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated Start or Stop conditions.

**FIGURE 18-28: BUS COLLISION DURING START CONDITION (SDA ONLY)**



# PIC18F2221/2321/4221/4321 FAMILY

## 19.2.4 AUTO-WAKE-UP ON SYNC BREAK CHARACTER

During Sleep mode, all clocks to the EUSART are suspended. Because of this, the Baud Rate Generator is inactive and a proper byte reception cannot be performed. The auto-wake-up feature allows the controller to wake-up due to activity on the RX/DT line while the EUSART is operating in Asynchronous mode.

The auto-wake-up feature is enabled by setting the WUE bit (BAUDCON<1>). Once set, the typical receive sequence on RX/DT is disabled and the EUSART remains in an Idle state, monitoring for a wake-up event independent of the CPU mode. A wake-up event consists of a high-to-low transition on the RX/DT line. (This coincides with the start of a Sync Break or a Wake-up Signal character for the LIN/J2602 protocol.)

Following a wake-up event, the module generates an RCIF interrupt. The interrupt is generated synchronously to the Q clocks in normal operating modes (Figure 19-8) and asynchronously, if the device is in Sleep mode (Figure 19-9). The interrupt condition is cleared by reading the RCREG register.

The WUE bit is automatically cleared once a low-to-high transition is observed on the RX line following the wake-up event. At this point, the EUSART module is in Idle mode and returns to normal operation. This signals to the user that the Sync Break event is over.

### 19.2.4.1 Special Considerations Using Auto-Wake-up

Since auto-wake-up functions by sensing rising edge transitions on RX/DT, information with any state changes before the Stop bit may signal a false end-of-character

and cause data or framing errors. To work properly, therefore, the initial character in the transmission must be all '0's. This can be 00h (8 bytes) for standard RS-232 devices or 000h (12 bits) for the LIN/J2602 bus.

Oscillator start-up time must also be considered, especially in applications using oscillators with longer start-up intervals (i.e., XT or HS mode). The Sync Break (or Wake-up Signal) character must be of sufficient length and be followed by a sufficient interval to allow enough time for the selected oscillator to start and provide proper initialization of the EUSART.

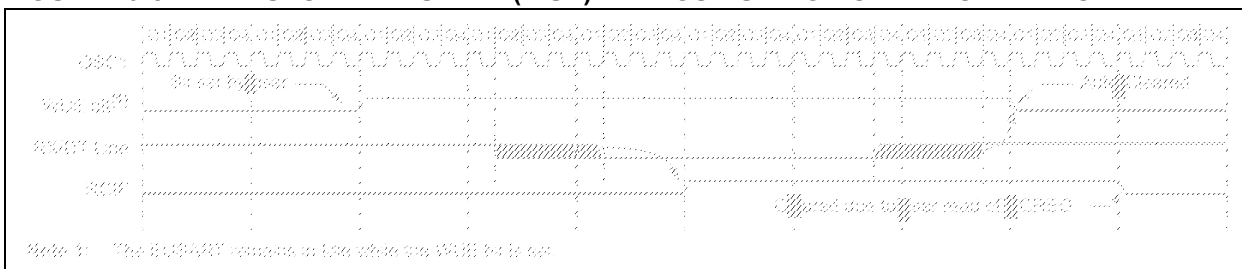
### 19.2.4.2 Special Considerations Using the WUE Bit

The timing of WUE and RCIF events may cause some confusion when it comes to determining the validity of received data. As noted, setting the WUE bit places the EUSART in an Idle mode. The wake-up event causes a receive interrupt by setting the RCIF bit. The WUE bit is cleared after this when a rising edge is seen on RX/DT. The interrupt condition is then cleared by reading the RCREG register. Ordinarily, the data in RCREG will be dummy data and should be discarded.

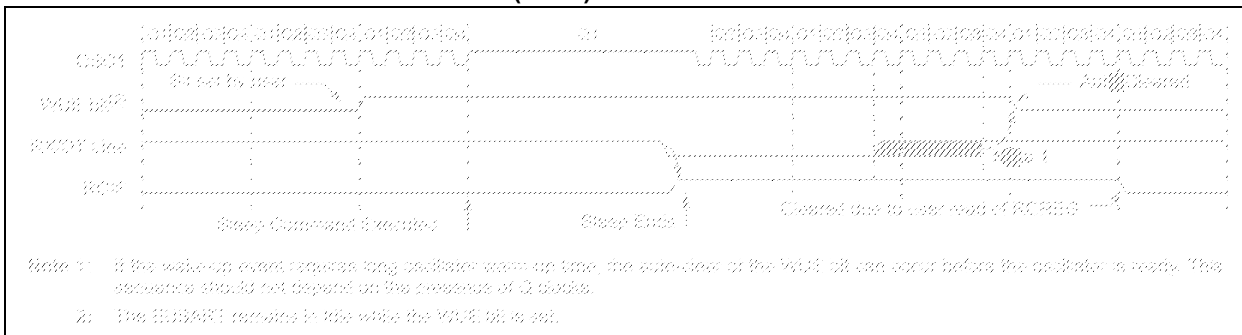
The fact that the WUE bit has been cleared (or is still set) and the RCIF flag is set should not be used as an indicator of the integrity of the data in RCREG. Users should consider implementing a parallel method in firmware to verify received data integrity.

To assure that no actual data is lost, check the RCIDL bit to verify that a receive operation is not in process. If a receive operation is not occurring, the WUE bit may then be set just prior to entering the Sleep mode.

**FIGURE 19-8: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING NORMAL OPERATION**

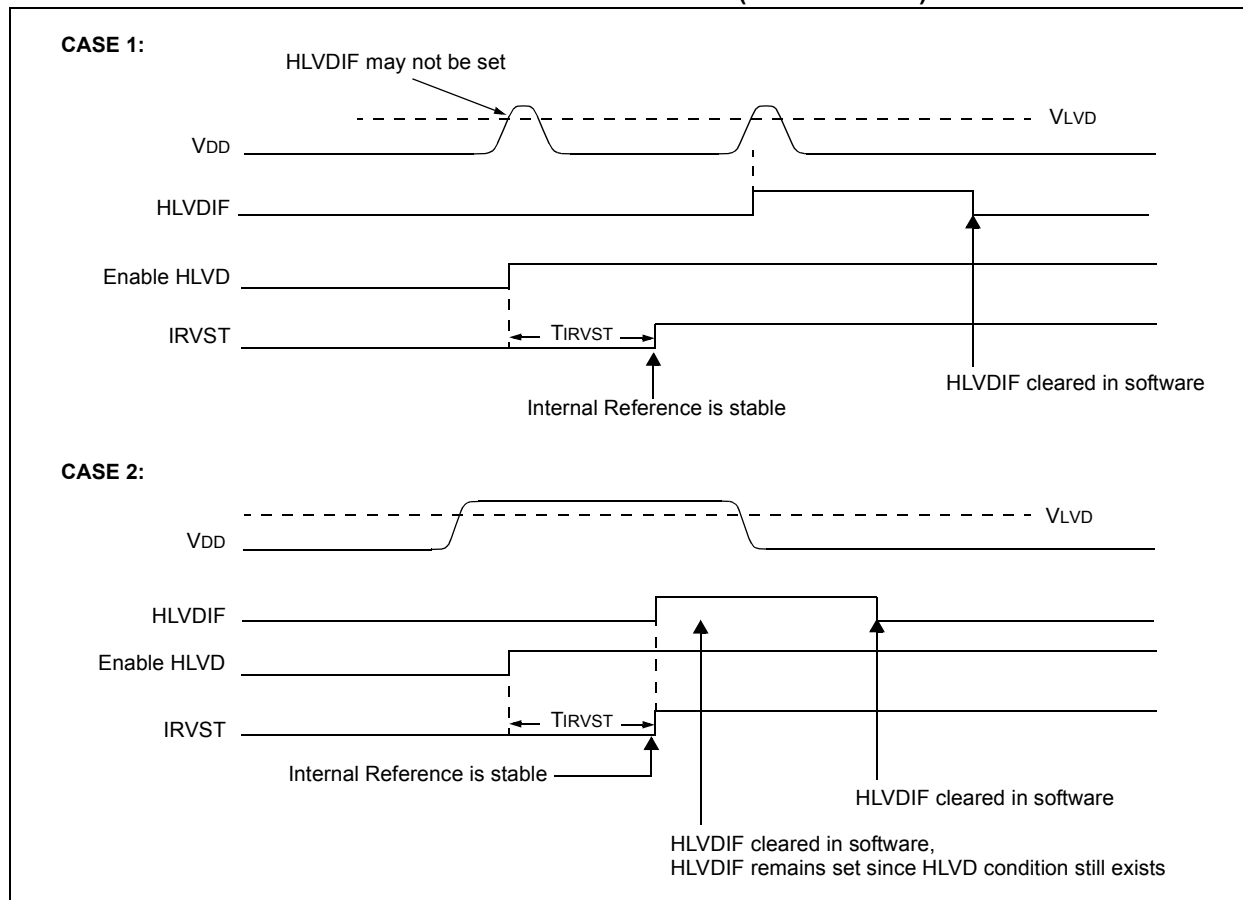


**FIGURE 19-9: AUTO-WAKE-UP BIT (WUE) TIMINGS DURING SLEEP**



# PIC18F2221/2321/4221/4321 FAMILY

**FIGURE 23-3: HIGH-VOLTAGE DETECT OPERATION (VDIRMAG = 1)**

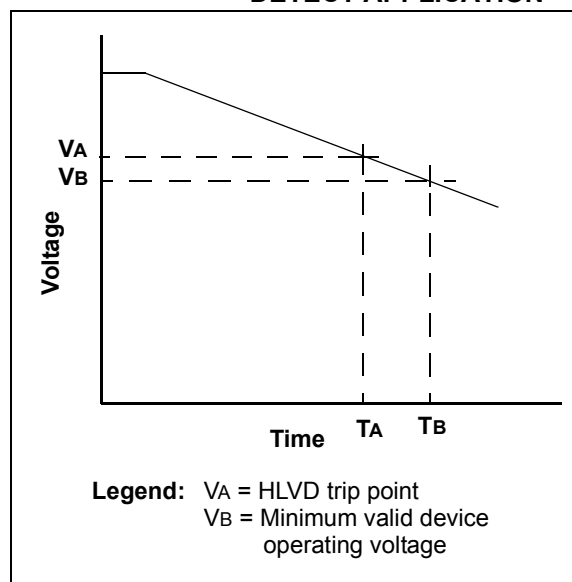


## 23.5 Applications

In many applications, the ability to detect a drop below or rise above a particular threshold is desirable. For example, the HLVD module could be periodically enabled to detect a Universal Serial Bus (USB) attach or detach. This assumes the device is powered by a lower voltage source than the USB when detached. An attach would indicate a high-voltage detect from, for example, 3.3V to 5V (the voltage on USB) and vice versa for a detach. This feature could save a design a few extra components and an attach signal (input pin).

For general battery applications, Figure 23-4 shows a possible voltage curve. Over time, the device voltage decreases. When the device voltage reaches voltage V<sub>A</sub>, the HLVD logic generates an interrupt at time T<sub>A</sub>. The interrupt could cause the execution of an ISR, which would allow the application to perform “house-keeping tasks” and perform a controlled shutdown before the device voltage exits the valid operating range at T<sub>B</sub>. The HLVD, thus, would give the application a time window, represented by the difference between T<sub>A</sub> and T<sub>B</sub>, to safely exit.

**FIGURE 23-4: TYPICAL LOW-VOLTAGE DETECT APPLICATION**



# PIC18F2221/2321/4221/4321 FAMILY

## REGISTER 24-4: CONFIG3H: CONFIGURATION REGISTER 3 HIGH (BYTE ADDRESS 300005h)

R/P-1	U-0	U-0	U-0	U-0	R/P-0	R/P-1	R/P-1
MCLRE	—	—	—	—	LPT1OSC	PBADEN	CCP2MX
bit 7							bit 0

- bit 7 **MCLRE:**  $\overline{\text{MCLR}}$  Pin Enable bit  
1 =  $\overline{\text{MCLR}}$  pin enabled; RE3 input pin disabled  
0 = RE3 input pin enabled;  $\overline{\text{MCLR}}$  disabled
- bit 6-3 **Unimplemented:** Read as '0'
- bit 2 **LPT1OSC:** Low-Power Timer1 Oscillator Enable bit  
1 = Timer1 configured for low-power operation  
0 = Timer1 configured for higher power operation
- bit 1 **PBADEN:** PORTB A/D Enable bit  
(Affects ADCON1 Reset state. ADCON1 controls PORTB<4:0> pin configuration.)  
1 = PORTB<4:0> pins are configured as analog input channels on Reset  
0 = PORTB<4:0> pins are configured as digital I/O on Reset
- bit 0 **CCP2MX:** CCP2 MUX bit  
1 = CCP2 input/output is multiplexed with RC1  
0 = CCP2 input/output is multiplexed with RB3

### Legend:

R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
-n = Value when device is unprogrammed	u = Unchanged from programmed state	

# PIC18F2221/2321/4221/4321 FAMILY

FIGURE 24-7: EXTERNAL BLOCK TABLE READ (EBTRn) DISALLOWED

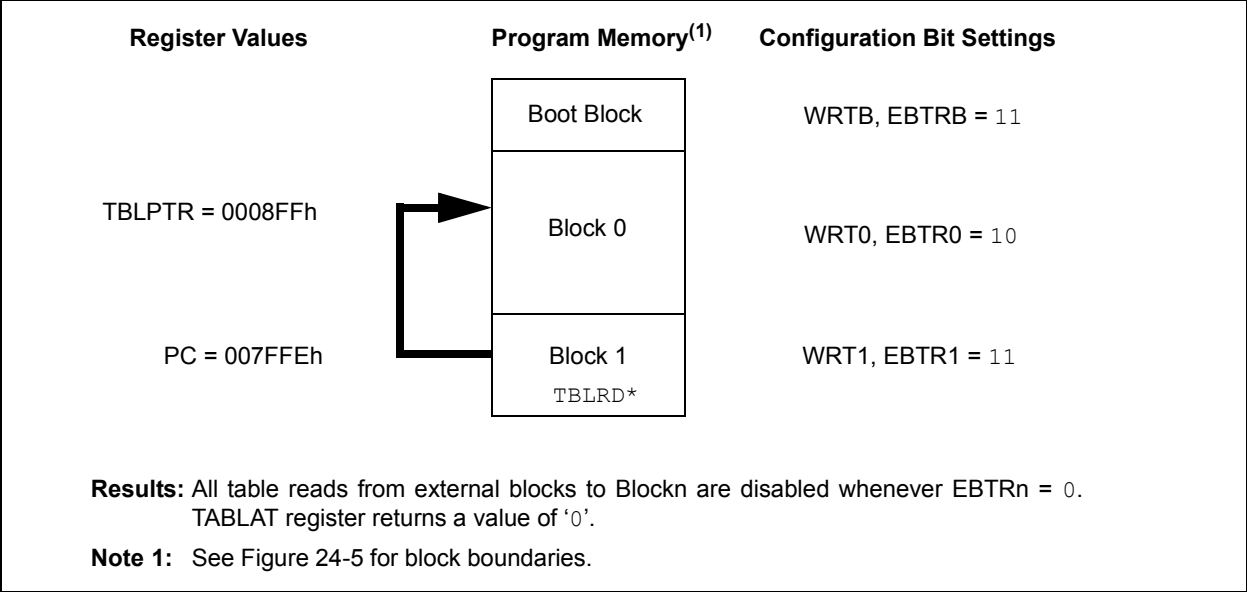
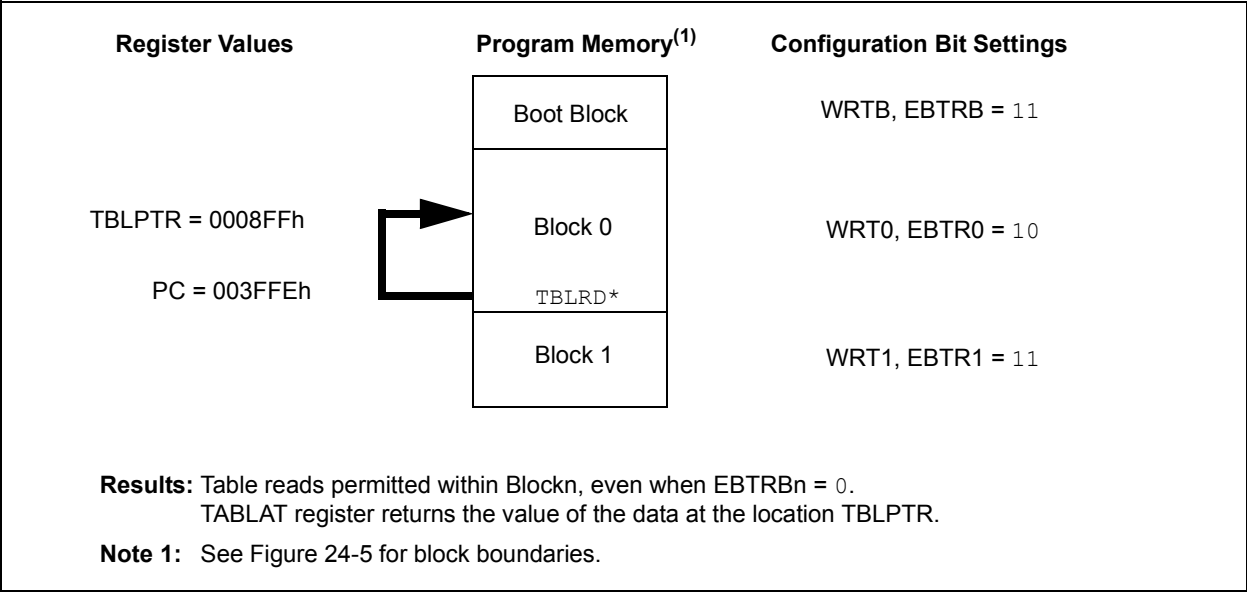


FIGURE 24-8: EXTERNAL BLOCK TABLE READ (EBTRn) ALLOWED





# PIC18F2221/2321/4221/4321 FAMILY

## LFSR Load FSR

Syntax: LFSR f, k

Operands:  $0 \leq f \leq 2$   
 $0 \leq k \leq 4095$

Operation:  $k \rightarrow \text{FSRf}$

Status Affected: None

Encoding:

1110	1110	00ff	$k_{11}kkk$
1111	0000	$k_7kkk$	$kkkk$

Description: The 12-bit literal 'k' is loaded into the File Select Register pointed to by 'f'.

Words: 2

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read literal 'k' MSB	Process Data	Write literal 'k' MSB to FSRfH
Decode	Read literal 'k' LSB	Process Data	Write literal 'k' to FSRfL

Example: LFSR 2, 3ABh

After Instruction

FSR2H = 03h  
 FSR2L = ABh

## MOVf Move f

Syntax: MOVf f {,d {,a}}

Operands:  $0 \leq f \leq 255$   
 $d \in [0, 1]$   
 $a \in [0, 1]$

Operation:  $f \rightarrow \text{dest}$

Status Affected: N, Z

Encoding:

0101	00da	ffff	ffff
------	------	------	------

Description: The contents of register 'f' are moved to a destination dependent upon the status of 'd'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed back in register 'f' (default). Location 'f' can be anywhere in the 256-byte bank.

If 'a' is '0', the Access Bank is selected. If 'a' is '1', the BSR is used to select the GPR bank (default).

If 'a' is '0' and the extended instruction set is enabled, this instruction operates in Indexed Literal Offset Addressing mode whenever  $f \leq 95$  (5Fh). See **Section 25.2.3 "Byte-Oriented and Bit-Oriented Instructions in Indexed Literal Offset Mode"** for details.

Words: 1

Cycles: 1

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write W

Example: MOVf REG, 0, 0

Before Instruction

REG = 22h  
 W = FFh

After Instruction

REG = 22h  
 W = 22h

# PIC18F2221/2321/4221/4321 FAMILY

## TBLRD Table Read

**Syntax:** TBLRD ( \*, \*+, \*-; +\*)

**Operands:** None

**Operation:** if TBLRD \*,  
(Prog Mem (TBLPTR)) → TABLAT,  
TBLPTR – No Change;  
if TBLRD \*+,  
(Prog Mem (TBLPTR)) → TABLAT,  
(TBLPTR) + 1 → TBLPTR;  
if TBLRD \*-,  
(Prog Mem (TBLPTR)) → TABLAT,  
(TBLPTR) – 1 → TBLPTR;  
if TBLRD +\*,  
(TBLPTR) + 1 → TBLPTR,  
(Prog Mem (TBLPTR)) → TABLAT

**Status Affected:** None

Encoding:	0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*
-----------	------	------	------	---

**Description:** This instruction is used to read the contents of Program Memory (P.M.). To address the program memory, a pointer called Table Pointer (TBLPTR) is used. The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2-Mbyte address range.

TBLPTR[0] = 0: Least Significant Byte of Program Memory Word

TBLPTR[0] = 1: Most Significant Byte of Program Memory Word

The TBLRD instruction can modify the value of TBLPTR as follows:

- no change
- post-increment
- post-decrement
- pre-increment

**Words:** 1

**Cycles:** 2

**Q Cycle Activity:**

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation
No operation	No operation (Read Program Memory)	No operation	No operation (Write TABLAT)

## TBLRD Table Read (Continued)

**Example 1:** TBLRD \*+ ;

Before Instruction  
 TABLAT = 55h  
 TBLPTR = 00A356h  
 MEMORY (00A356h) = 34h  
 After Instruction  
 TABLAT = 34h  
 TBLPTR = 00A357h

**Example 2:** TBLRD +\* ;

Before Instruction  
 TABLAT = AAh  
 TBLPTR = 01A357h  
 MEMORY (01A357h) = 12h  
 MEMORY (01A358h) = 34h  
 After Instruction  
 TABLAT = 34h  
 TBLPTR = 01A358h

# PIC18F2221/2321/4221/4321 FAMILY

## 27.3 DC Characteristics: PIC18F2221/2321/4221/4321 (Industrial) PIC18LF2221/2321/4221/4321 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq T_A \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ for extended			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D070	IPU IPURB	<b>Weak Pull-up Current</b> <b>PORTB Weak Pull-up Current</b>	50	400	$\mu\text{A}$	$V_{DD} = 5\text{V}$ , $V_{PIN} = V_{SS}$
D080	VOL	<b>Output Low Voltage</b> I/O Ports	—	0.6	V	$I_{OL} = 8.5\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
D083		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	—	0.6	V	$I_{OL} = 1.6\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
D090	VOH	<b>Output High Voltage</b> <sup>(3)</sup> I/O Ports	$V_{DD} - 0.7$	—	V	$I_{OH} = -3.0\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
D092		OSC2/CLKO (RC, RCIO, EC, ECIO modes)	$V_{DD} - 0.7$	—	V	$I_{OH} = -1.3\text{ mA}$ , $V_{DD} = 4.5\text{V}$ , $-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$
D100	COSC2	<b>Capacitive Loading Specs on Output Pins</b> OSC2 Pin	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	Cio	All I/O Pins and OSC2 (in RC mode)	—	50	pF	Maximum that allows the AC Timing Specifications to be met
D102	Cb	SCL, SDA	—	400	pF	Maximum bus capacitance permitted by I <sup>2</sup> C™ Specification

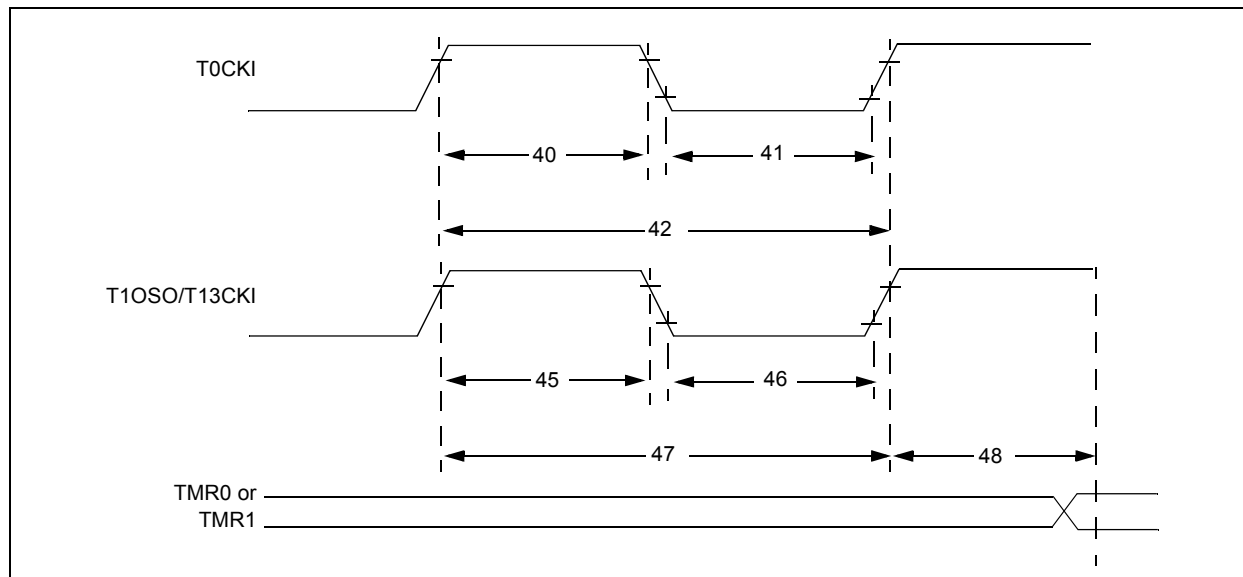
**Note 1:** In RC oscillator configuration, the OSC1/CLKI pin is a Schmitt Trigger input. It is not recommended that the PIC® device be driven with an external clock while in RC mode.

**2:** The leakage current on the  $\overline{\text{MCLR}}$  pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

**3:** Negative current is defined as current sourced by the pin.

# PIC18F2221/2321/4221/4321 FAMILY

**FIGURE 27-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS**



**TABLE 27-11: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS**

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No prescaler	$0.5 T_{CY} + 20$	—	ns	
			With prescaler	10	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No prescaler	$0.5 T_{CY} + 20$	—	ns	
			With prescaler	10	—	ns	
42	Tt0P	T0CKI Period	No prescaler	$T_{CY} + 10$	—	ns	
			With prescaler	Greater of: 20 ns or $(T_{CY} + 40)/N$	—	ns	
45	Tt1H	T13CKI High Time	Synchronous, no prescaler	$0.5 T_{CY} + 20$	—	ns	V <sub>DD</sub> = 2.0V
			Synchronous, with prescaler	PIC18FXXXX	10	ns	
				PIC18LFXXXX	25	ns	
			Asynchronous	PIC18FXXXX	30	ns	
46	Tt1L	T13CKI Low Time	Synchronous, no prescaler	$0.5 T_{CY} + 5$	—	ns	V <sub>DD</sub> = 2.0V
			Synchronous, with prescaler	PIC18FXXXX	10	ns	
				PIC18LFXXXX	25	ns	
			Asynchronous	PIC18FXXXX	30	ns	
47	Tt1P	T13CKI Input Period	Synchronous	Greater of: 20 ns or $(T_{CY} + 40)/N$	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	ns	
	Ft1	T13CKI Oscillator Input Frequency Range		DC	50	kHz	
48	Tcke2tmr1	Delay from External T13CKI Clock Edge to Timer Increment		2 T <sub>osc</sub>	7 T <sub>osc</sub>	—	

# PIC18F2221/2321/4221/4321 FAMILY

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## APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC16C74A to a PIC16C74B.

The PIC18F2221/2321/4221/4321 family of devices is functionally the same as the PIC18F4320 family. Code written for a PIC18F4320 will generally work on a PIC18F4321 with few or no changes.

The following is a list of changes the user should be aware of when migrating an application from the PIC18F4320 to the PIC18F4321. Code written for the PIC18F4321 may not run as expected due to these differences.

1. Entry to power-managed modes has changed. Modifying the SCS1:SCS0 bits (OSCCON<1:0>) immediately changes the current clock source. It is not necessary to execute a `SLEEP` instruction to change clock sources. Refer to **Section 4.1.2 “Entering Power-Managed Modes”** for details.
2. Exit from power-managed modes has changed. A WDT wake or interrupt does not cause an automatic return to `PRI_RUN` mode. The controller will execute code while continuing to use the current clock source. If the controller was operating in `RC_IDLE` or `RC_RUN` mode, an interrupt will cause entry to `RC_RUN` mode until code selects another power-managed mode. Refer to **Section 4.4 “Idle Modes”** for details.
3. The extended instruction set can be configured as enabled using the `XINST` bit (`CONFIG4L<6>`). The access memory map is also modified when the extended instruction set is enabled. Refer to **Section 6.5 “Data Memory and the Extended Instruction Set”** and **Section 24.2 “Extended Instruction Set”** for details.
4. There may also be changes to the electrical specifications. Refer to **Section 27.0 “Electrical Characteristics”** for details.

## APPENDIX D: MIGRATION FROM BASELINE TO ENHANCED DEVICES

This section discusses how to migrate from a Baseline device (i.e., PIC16C5X) to an Enhanced MCU device (i.e., PIC18FXXX).

The following are the list of modifications over the PIC16C5X microcontroller family:

**Not Currently Available**