Infineon Technologies - MB90561APFM-GS-313-BNDE1 Datasheet

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90561apfm-gs-313-bnde1

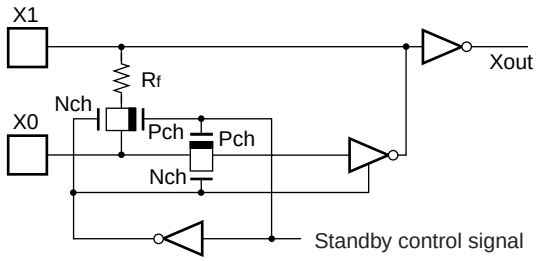
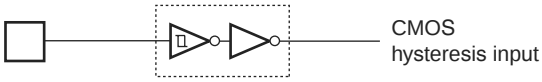
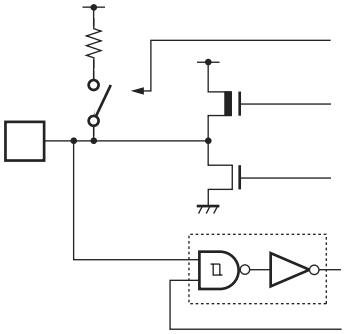
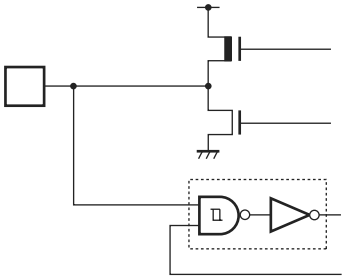
(Continued)

- **Instruction set**
  - Bit, byte, word, and long word data types
  - 23 different addressing modes
  - Enhanced calculation precision using a 32-bit accumulator
  - Enhanced signed multiplication and division instructions and RETI instruction
- **Instruction set designed for high level language (C) and multi-tasking**
  - Uses a system stack pointer
  - Symmetric instruction set and barrel shift instructions
- **Program patch function (2 address pointers) .**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 32 interrupts
- **Data transfer function**
  - Extended intelligent I/O service function : Up to 16 channels
- **Low-power consumption modes**
  - Sleep mode (CPU operating clock stops.)
  - Timebase timer mode (Only oscillation clock and timebase timer continue to operate.)
  - Stop mode (Oscillation clock stops.)
  - CPU intermittent operation mode (The CPU operates intermittently at the specified interval.)
- **Package**
  - LQFP-64P (FTP-64P-M23 : 0.65 mm pin pitch)
  - QFP-64P (FTP-64P-M06 : 1.00 mm pin pitch)
  - SH-DIP (DIP-64P-M01 : 1.778 mm pin pitch)
- **Process : CMOS technology**

■ PERIPHERAL FUNCTIONS (RESOURCES)

- **I/O ports : 51 ports (max.)**
- **Timebase timer : 1 channel**
- **Watchdog timer : 1 channel**
- **16-bit reload timer : 2 channels**
- **Multi-function timer**
  - 16-bit free-run timer : 1 channel
  - Output compare : 6 channels
    Can output an interrupt request when a match occurs between the count in the 16-bit freerun timer and the value set in the compare register.
  - Input capture : 4 channels
    On detecting an active edge on the input signal from an external input pin, copies the count value of the 16-bit freerun timer to the input capture data register and generates an interrupt request.
  - 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) The period and duty of the output pulse can be set by the program.
  - Waveform generator (8-bit timer : 3 channels)
- **UART** : **2 channels**
  - Full-duplex, double-buffered (8-bit)
  - Can be set to asynchronous or clock synchronous serial transfer (I/O expansion serial) operation
- **DTP/external interrupt circuit (8 channels)**
  - External interrupts can activate the extended intelligent I/O service.
  - Generates interrupts in response to external interrupt inputs.

■ I/O CIRCUITS

Type	Circuit	Remarks
A		• Oscillation circuit Internal oscillation feedback resistor (R_f)
B		• CMOS hysteresis input
C		• CMOS hysteresis I/O pin with pull-up control CMOS output CMOS hysteresis input (with input cut-off function in standby mode) Internal pull-up resistor (R_p) < Note > • The pull-up resistor is active when the port is set as an input.
D		• CMOS hysteresis I/O pin CMOS output CMOS hysteresis input (with input cut-off function in standby mode) < Notes > • The I/O port output and internal resource output share the same output buffer. • The I/O port input and internal resource input share the same input buffer.

(Continued)

■ I/O MAP

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
000000H	PDR0	Port 0 data register	R/W	Port 0	XXXXXXXXB
000001H	PDR1	Port 1 data register	R/W	Port 1	XXXXXXXXB
000002H	PDR2	Port 2 data register	R/W	Port 2	XXXXXXXXB
000003H	PDR3	Port 3 data register	R/W	Port 3	XXXXXXXXB
000004H	PDR4	Port 4 data register	R/W	Port 4	XXXXXXXXB
000005H	PDR5	Port 5 data register	R/W	Port 5	XXXXXXXXB
000006H	PDR6	Port 6 data register	R/W	Port 6	XXXXXXXXB
000007H to 00000FH	Access prohibited				
000010H	DDR0	Port 0 direction register	R/W	Port 0	0 0 0 0 0 0 0 0B
000011H	DDR1	Port 1 direction register	R/W	Port 1	0 0 0 0 0 0 0 0B
000012H	DDR2	Port 2 direction register	R/W	Port 2	0 0 0 0 0 0 0 0B
000013H	DDR3	Port 3 direction register	R/W	Port 3	0 0 0 0 0 0 0 0B
000014H	DDR4	Port 4 direction register	R/W	Port 4	X 0 0 0 0 0 0 0B
000015H	DDR5	Port 5 direction register	R/W	Port 5	0 0 0 0 0 0 0 0B
000016H	DDR6	Port 6 direction register	R/W	Port 6	XXXX 0 0 0 0B
000017H	ADER	Analog input enable register	R/W	Port 5, A/D converter	1 1 1 1 1 1 1 1B
000018H to 00001FH	Access prohibited				
000020H	SMR0	Mode register ch0	R/W	UART0	0 0 0 0 0 X 0 0B
000021H	SCR0	Control register ch0	W, R/W		0 0 0 0 0 1 0 0B
000022H	SIDR0	Input data register ch0	R		XXXXXXXXB
	SODR0	Output data register ch0	W		
000023H	SSR0	Status register ch0	R, R/W		0 0 0 0 1 0 0 0B
000024H	SMR1	Mode register ch1	R/W	UART1	0 0 0 0 0 X 0 0B
000025H	SCR1	Control register ch1	W, R/W		0 0 0 0 0 1 0 0B
000026H	SIDR1	Input data register ch1	R		XXXXXXXXB
	SODR1	Output data register ch1	W		
000027H	SSR1	Status register ch1	R, R/W		0 0 0 0 1 0 0 0B
000028H	Access prohibited				
000029H	CDCR0	Communication prescaler control register ch0	R/W	Communication prescaler	0 XXX 0 0 0 0B

(Continued)

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
00004D$_H$	PPGC5	PPG control register ch5 (upper)	R/W	8/16-bit PPG timer	0 0 0 0 0 0 0 1$_B$
00004E$_H$	PCS45	PPG clock control register ch4, ch5	R/W		0 0 0 0 0 0 XX$_B$
00004F$_H$	Access prohibited				
000050$_H$	TMRR0	8-bit reload register ch0	R/W	Waveform generator	XXXXXXXX$_B$
000051$_H$	DTCR0	8-bit timer control register ch0	R/W		0 0 0 0 0 0 0 0$_B$
000052$_H$	TMRR1	8-bit reload register ch1	R/W		XXXXXXXX$_B$
000053$_H$	DTCR1	8-bit timer control register ch1	R/W		0 0 0 0 0 0 0 0$_B$
000054$_H$	TMRR2	8-bit reload register ch2	R/W		XXXXXXXX$_B$
000055$_H$	DTCR2	8-bit timer control register ch2	R/W		0 0 0 0 0 0 0 0$_B$
000056$_H$	SIGCR	Waveform control register	R/W		0 0 0 0 0 0 0 0$_B$
000057$_H$	Access prohibited				
000058$_H$	CPCLR	Compare clear register (lower)	R/W	16-bit freerun timer	XXXXXXXX$_B$
000059$_H$		Compare clear register (upper)	R/W		XXXXXXXX$_B$
00005A$_H$	TCDT	Timer data register (lower)	R/W		0 0 0 0 0 0 0 0$_B$
00005B$_H$		Timer data register (upper)	R/W		0 0 0 0 0 0 0 0$_B$
00005C$_H$	TCCS	Timer control/status register (lower)	R/W		0 0 0 0 0 0 0 0$_B$
00005D$_H$		Timer control/status register (upper)	R/W		0 XX 0 0 0 0 0$_B$
00005E$_H$	Access prohibited				
00005F$_H$					
000060$_H$	IPCP0	Input capture data register ch0 (lower)	R	Input capture	XXXXXXXX$_B$
000061$_H$		Input capture data register ch0 (upper)	R		XXXXXXXX$_B$
000062$_H$	IPCP1	Input capture data register ch1 (lower)	R		XXXXXXXX$_B$
000063$_H$		Input capture data register ch1 (upper)	R		XXXXXXXX$_B$
000064$_H$	IPCP2	Input capture data register ch2 (lower)	R		XXXXXXXX$_B$
000065$_H$		Input capture data register ch2 (upper)	R		XXXXXXXX$_B$
000066$_H$	IPCP3	Input capture data register ch3 (lower)	R		XXXXXXXX$_B$
000067$_H$		Input capture data register ch3 (upper)	R		XXXXXXXX$_B$
000068$_H$	ICS01	Input capture control register 01	R/W		0 0 0 0 0 0 0 0$_B$
000069$_H$	Access prohibited				
00006A$_H$	ICS23	Input capture control register 23	R/W	Input capture	0 0 0 0 0 0 0 0$_B$
00006B$_H$ to 00006E$_H$	Access prohibited				

(Continued)

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
00006F$_H$	ROMM	ROM mirror function selection register	W	ROM mirror function selection module	XXXXXXX 1$_B$
000070$_H$	OCCP0	Compare register ch0 (lower)	R/W	Output compare	XXXXXXXX$_B$
000071$_H$		Compare register ch0 (upper)	R/W		XXXXXXXX$_B$
000072$_H$	OCCP1	Compare register ch1 (lower)	R/W		XXXXXXXX$_B$
000073$_H$		Compare register ch1 (upper)	R/W		XXXXXXXX$_B$
000074$_H$	OCCP2	Compare register ch2 (lower)	R/W		XXXXXXXX$_B$
000075$_H$		Compare register ch2 (upper)	R/W		XXXXXXXX$_B$
000076$_H$	OCCP3	Compare register ch3 (lower)	R/W		XXXXXXXX$_B$
000077$_H$		Compare register ch3 (upper)	R/W		XXXXXXXX$_B$
000078$_H$	OCCP4	Compare register ch4 (lower)	R/W		XXXXXXXX$_B$
000079$_H$		Compare register ch4 (upper)	R/W		XXXXXXXX$_B$
00007A$_H$	OCCP5	Compare register ch5 (lower)	R/W		XXXXXXXX$_B$
00007B$_H$		Compare register ch5 (upper)	R/W		XXXXXXXX$_B$
00007C$_H$	OCS0	Compare control register ch0 (lower)	R/W		0 0 0 0 XX 0 0$_B$
00007D$_H$	OCS1	Compare control register ch1 (upper)	R/W		XXX 0 0 0 0 0$_B$
00007E$_H$	OCS2	Compare control register ch2 (lower)	R/W		0 0 0 0 XX 0 0$_B$
00007F$_H$	OCS3	Compare control register ch3 (upper)	R/W		XXX 0 0 0 0 0$_B$
000080$_H$	OCS4	Compare control register ch4 (lower)	R/W		0 0 0 0 XX 0 0$_B$
000081$_H$	OCS5	Compare control register ch5 (upper)	R/W		XXX 0 0 0 0 0$_B$
000082$_H$	TMCSR0 : L	Timer control status register ch0 (lower)	R/W	16-bit reload timer	0 0 0 0 0 0 0 0$_B$
000083$_H$	TMCSR0 : H	Timer control status register ch0 (upper)	R/W		XXXX 0 0 0 0$_B$
000084$_H$	TMR0	16-bit timer register ch0 (lower)	R		XXXXXXXX$_B$
	TMRLR0	16-bit reload register ch0 (lower)	W		XXXXXXXX$_B$
000085$_H$	TMR0	16-bit timer register ch0 (upper)	R		XXXXXXXX$_B$
	TMRHR0	16-bit reload register ch0 (upper)	W		XXXXXXXX$_B$
000086$_H$	TMCSR1 : L	Timer control status register ch1 (lower)	R/W		0 0 0 0 0 0 0 0$_B$
000087$_H$	TMCSR1 : H	Timer control status register ch1 (upper)	R/W		XXXX 0 0 0 0$_B$
000088$_H$	TMR1	16-bit timer register ch1 (lower)	R		XXXXXXXX$_B$
	TMRLR1	16-bit reload register ch1 (lower)	W		XXXXXXXX$_B$
000089$_H$	TMR1	16-bit timer register ch1 (upper)	R		XXXXXXXX$_B$
	TMRHR1	16-bit reload register ch1 (upper)	W		XXXXXXXX$_B$

(Continued)

Address	Abbreviated Register Name	Register name	Read/ Write	Resource Name	Initial Value
0000B6H	ICR06	Interrupt control register 06 (for writing)	W, R/W	Interrupts	XXXX 0 1 1 1B
		Interrupt control register 06 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000B7H	ICR07	Interrupt control register 07 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 07 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000B8H	ICR08	Interrupt control register 08 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 08 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000B9H	ICR09	Interrupt control register 09 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 09 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BAH	ICR10	Interrupt control register 10 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 10 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BBH	ICR11	Interrupt control register 11 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 11 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BCH	ICR12	Interrupt control register 12 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 12 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BDH	ICR13	Interrupt control register 13 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 13 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BEH	ICR14	Interrupt control register 14 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 14 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000BFH	ICR15	Interrupt control register 15 (for writing)	W, R/W		XXXX 0 1 1 1B
		Interrupt control register 15 (for reading)	R, R/W		XX 0 0 0 1 1 1B
0000C0H to 0000FFH	Unused area				
000100H to #H	RAM area				
#H to 001FEFH	Reserved area				
001FF0H	PADR0	Program address detection register ch0 (lower)	R/W	Address match detection	XXXXXXXXB
001FF1H		Program address detection register ch0 (middle)	R/W		XXXXXXXXB
001FF2H		Program address detection register ch0 (lower)	R/W		XXXXXXXXB

(Continued)

4. 16-Bit Reload Timers 0 and 1 (With Event Count Function)

- The 16-bit reload timers have the following functions.
- The count clock can be selected from three internal clocks or the external event clock.
- An interrupt to the CPU can be generated when an underflow occurs on 16-bit reload timer 0 or 1. This interrupt allows the timers to be used as interval timers.
- Two different operation modes can be selected when an underflow occurs on 16-bit reload timer 0 or 1: one-shot mode in which timer operation halts when an underflow occurs or reload mode in which the value in the reload register is loaded into the timer and counting continues.
- Extended intelligent I/O service (EI^{2}OS) is supported.
- The MB90560/565 series contains two 16-bit reload timer channels.

- **16-bit reload timer operation modes**

Count Clock	Start Trigger	Operation When an Underflow Occurs
Internal clock	Software trigger	One-shot mode
		Reload mode
	External trigger	One-shot mode
		Reload mode
Event count mode (external clock mode)	Software trigger	One-shot mode
		Reload mode

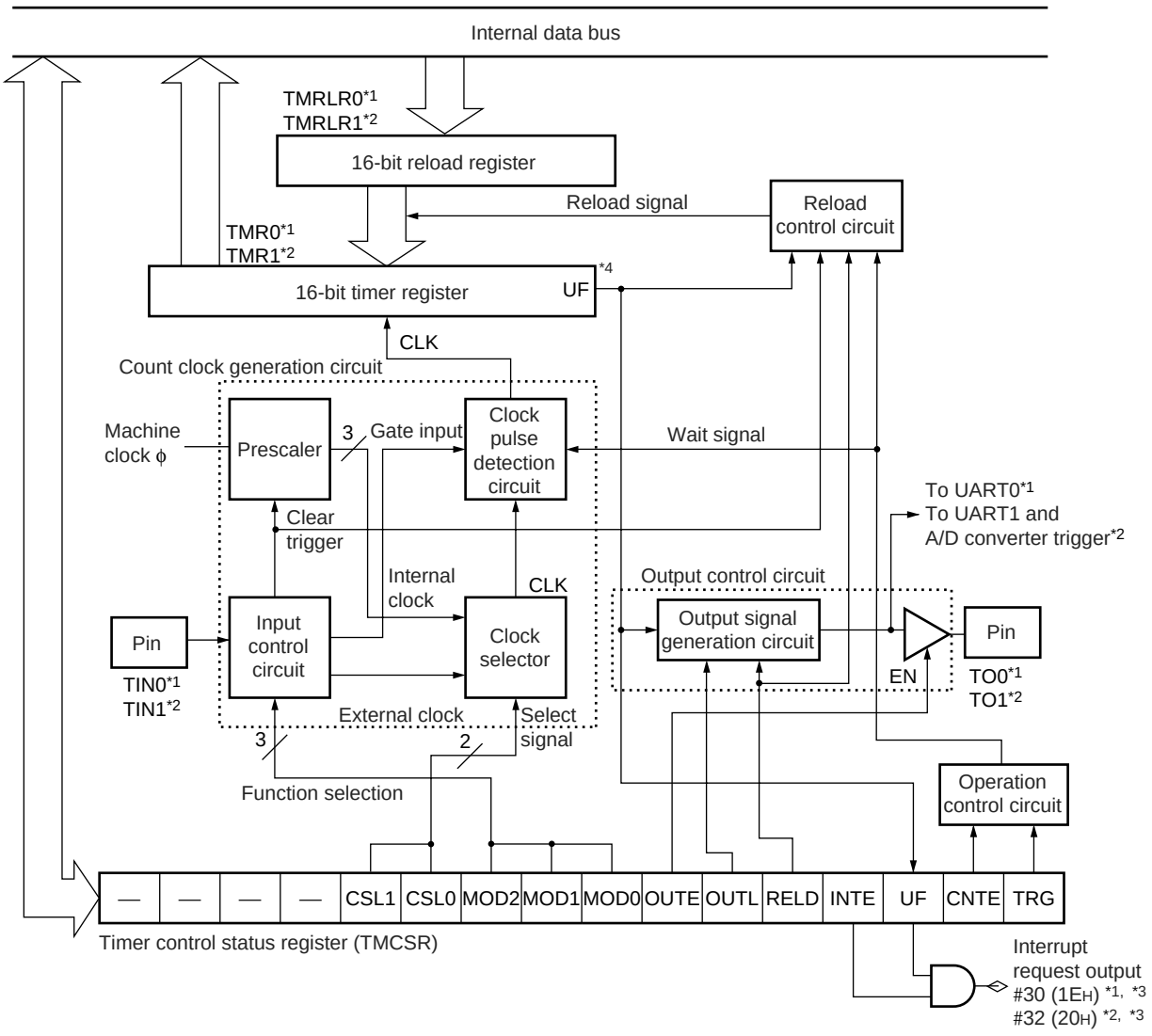
- **Interval times for the 16-bit reload timers**

Count Clock	Count Clock Period	Example of Interval Times
Internal clock	$2^1/\phi$ (0.125 µs)	0.125 µs to 8.192 ms
	$2^3/\phi$ (0.5 µs)	0.5 µs to 32.768 ms
	$2^5/\phi$ (2.0 µs)	2.0 µs to 131.1 ms
Event count mode	$2^3/\phi$ or longer	0.5 µs or longer

Note : The values enclosed in ( ) and the example of interval times is for a machine clock frequency of 16 MHz.
ϕ is the machine clock frequency value for the calculation.

Remarks : 16-bit reload timer 0 can be used to generate the baud rate for UART0.
16-bit reload timer 1 can be used to generate the baud rate for UART1 and activation trigger for the A/D converter.

- **Block diagram**



*1 : Channel 0
*2 : Channel 1
*3 : Interrupt number
*4 : Underflow

- An interrupt can be generated when an active edge is detected on the external signal (ICS01, ICS23 : ICE0 = “1”, ICE1 = “1”, ICE2 = “1”, ICE3 = “1”) .

- **8/16-bit PPG timer** (**8-bit** : **6 channels**, **16-bit** : **3 channels**)

The 8/16-bit PPG timer consists of an 8-bit down counter (PCNT) , PPG control registers (PPGC0 to PPGC 5) , PPG clock control registers (PCS01, PCS23, PCS45) , and PPG reload registers (PRLL0 to PRLL5, PRLH0 to PRLH5) .
When used as an 8/16-bit reload timer, the PPG operates as an event timer. The PPG can also be used to output pulses with specified frequency and duty ratio.

- 8-bit PPG mode
  Each channel operates as an independent 8-bit PPG.
- 8-bit prescaler + 8-bit PPG mode
  ch0 (ch2, ch4) operates as an 8-bit prescaler and ch1 (ch3, ch5) operates as a variable frequency PPG by counting up on the borrow output from ch0 (ch2, ch4) .
- 16-bit PPG mode
  ch0 (ch2, ch4) and ch1 (ch3, ch5) operate together as a 16-bit PPG.
- PPG operation
  Outputs pulses with the specified frequency and duty ratio (ratio of “H” level period and “L” level period), and can also be used as a D/A converter when combined with an external circuit.

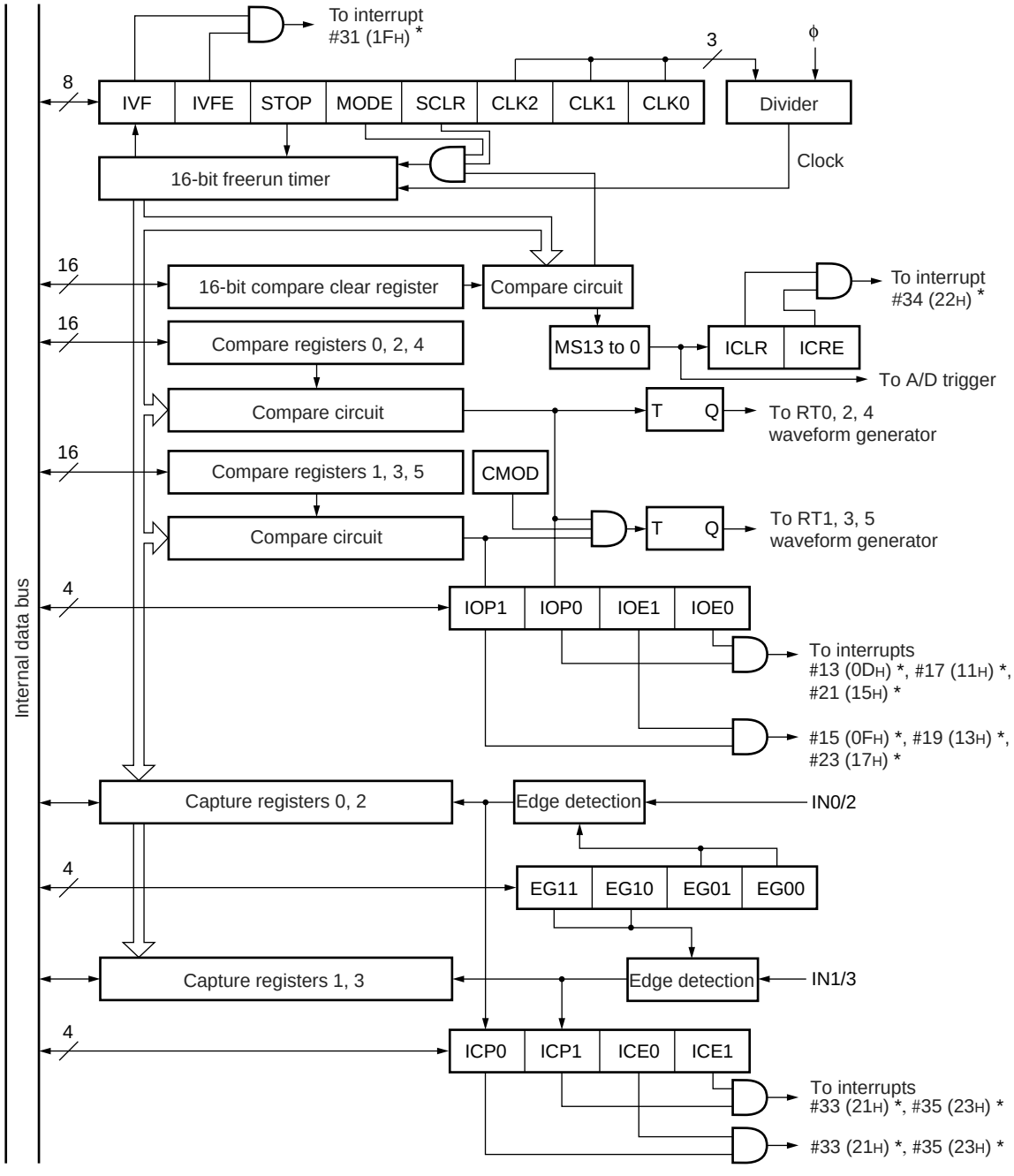
- **Waveform generator**

The waveform generator consists of an 8-bit timer, 8-bit timer control registers (DTCR0 to DTCR2) , 8-bit reload registers (TMRR0 to TMRR2) , and waveform control register (SIGCR) .

The waveform generator can generate a DC chopper output or non-overlapping three-phase waveform output for inverter control using the realtime outputs (RT0 to RT5) and 8/16-bit PPG timer.

- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the PPG timer pulse output. (Deadtime timer function)
- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the realtime outputs (RT1, RT3, RT5) . (Deadtime timer function)
- A GATE signal can be generated when a match occurs between the count from the 16-bit freerun timer and compare register in the output compare (OCCP0 to OCCP5) (rising edge on realtime output (RT)) to control the PPG timer operation. (GATE function)
- Can control the RTO0 to RTO5 pin outputs using the DTTI pin input.
  By making the DTTI pin input clockless, the pins can be controlled externally even when the oscillation clock is halted. (The level for each pin can be set by the program.) However, the I/O ports (P30 to P35) must have been set beforehand as outputs and the output values set in the port 3 data register (PDR3) .

- **Block diagram**
- **16-bit freerun timer, input capture, and output compare**



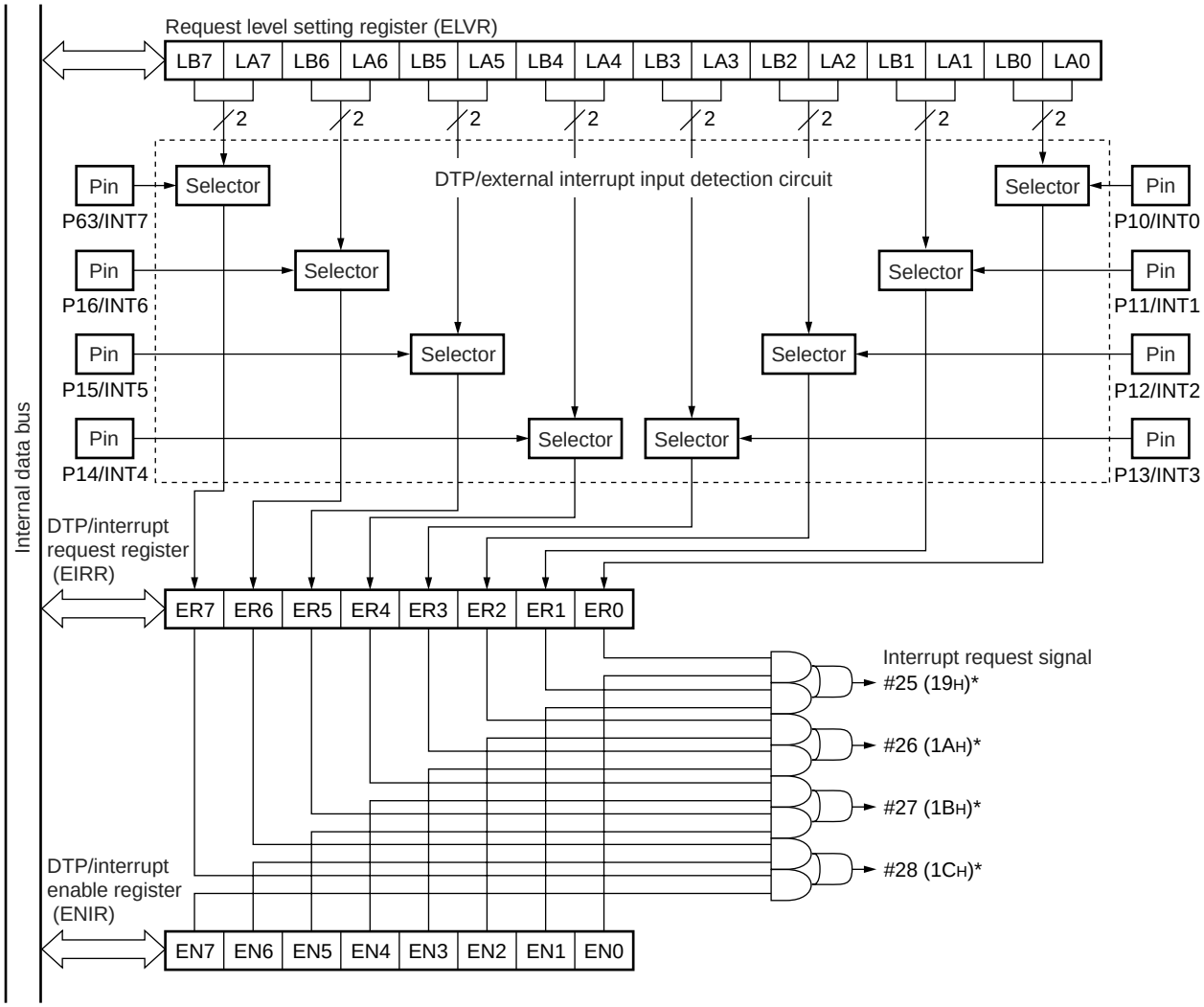
* : Interrupt number
ϕ : Machine clock frequency

(2) Structure of the DTP/external interrupt circuit

The DTP/external interrupt circuit consists of the following four blocks :

- DTP/interrupt detection circuit
- DTP/interrupt request register (EIRR)
- DTP/interrupt enable register (ENIR)
- Request level setting register (ELVR)

- **Block diagram**



* : Interrupt number

9. 8/10-Bit A/D Converter

- **Overview of the 8/10-bit A/D converter**
- The 8/10-bit A/D converter uses RC successive approximation to convert analog input voltages to an 8-bit or 10-bit digital value.
- The input signals can be selected from the eight analog input pin channels.

- **8/10-bit A/D converter functions**

A/D conversion time	The minimum conversion time is 6.13 µs (for a 16 MHz machine clock, including sampling time) . The minimum sampling time is 2.0 µs (for a 16 MHz machine clock)
Conversion method	RC successive approximation with sample & hold circuit
Resolution	8-bit or 10-bit, selectable
Analog input pins	Eight analog input pin channels are available. The input pin can be selected by the program.
Interrupts	An interrupt request can be generated and EI^{2}OS invoked when A/D conversion completes. The conversion data protection function operates when A/D conversion is performed with the interrupt enabled.
A/D conversion start trigger	The conversion start trigger can be set from the following options : software, output of 16-bit reload timer 1 (rising edge) , or zero detection edge from 16-bit freerun timer.
EI^{2}OS support	Supported by the extended intelligent I/O service (EI^{2}OS) .

- **8/10-bit A/D converter conversion modes**

Conversion Mode	Single Conversion Mode Operation	Scan Conversion Mode Operation
Single-shot conversion mode 1 Single-shot conversion mode 2	Performs one conversion for the specified channel (1 channel) then halts.	Sequentially performs one conversion for multiple channels (up to 8 channels can be set) , then halts.
Continuous conversion mode	Performs repeated conversions for the specified channel (1 channel) .	Performs repeated conversions for the specified channels (up to 8 channels can be set) .
Incremental conversion mode	Performs one conversion for the specified channel (1 channel) then halts and waits for the next activation.	Sequentially performs one conversion for multiple channels (up to 8 channels can be set) , then halts and waits for the next activation.

- **8/10-bit A/D converter interrupts and EI^{2}OS**

Interrupt No.	Interrupt Control Register		Vector Table Address			EI^{2}OS
	Register Name	Address	Lower	Upper	Bank	
#11 (0B$_H$)	ICR00	0000B0$_H$	FFFFD0$_H$	FFFFD1$_H$	FFFFD2$_H$	○

○ : Available

13. 1 Mbit Flash Memory

- This section describes the flash memory on the MB90F568 and does not apply to evaluation and mask ROM versions.
- The flash memory is located in banks FE to FF in the CPU memory map.

- **Flash memory functions**

	Function
Memory size	• 1 Mbit (128 KBytes)
Memory configuration	• 128 KWords × 8 bits or 64 KWords × 16 bits
Sector configuration	• 16 KBytes + 8 KBytes + 8 KBytes + 32 KBytes + 64 KBytes
Sector protect function	• Selectable for each sector
Programming algorithm	• Automatic programming algorithm (Embedded Algorithm : Equivalent to MBM29F400TA)
Operation commands	• Compatible with JEDEC standard commands • Includes an erase pause and restart function • Write/erase completion detection by data polling or toggle bit • Erasing by sector available (sectors can be combined in any combination)
No. of write/erase cycles	• Min. 10,000 guaranteed
Memory write/erase method	• Can be written and erased using a parallel writer • Can be written and erased using a dedicated serial writer • Can be written and erased by the program
Interrupts	• Write and erase completion interrupts
EI^{2}OS support	• Not supported by the extended intelligent I/O service (EI^{2}OS) .

- **Sector configuration of flash memory**

Flash memory	CPU address	Writer address*
SA0 (64 Kbyte)	FE0000H FEFFFFH	60000H 6FFFFH
SA1 (32 Kbyte)	FF0000H FF7FFFH	70000H 77FFFH
SA2 (8 Kbyte)	FF8000H FF9FFFH	78000H 79FFFH
SA3 (8 Kbyte)	FFA000H FFBFFFH	7A000H 7BFFFH
SA4 (16 Kbyte)	FFC000H FEFFFFH	7C000H 7FFFFH

* : The writer address is the address to be used instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing with a general-purpose parallel writer.

6. Flash Memory Erase and Programming Performance

Parameter	Condition	Value			Units	Remarks
		Min	Typ	Max		
Sector erase time	T_A = + 25 °C Vcc = 5.0 V	—	1	15	s	Excludes 00H programming prior erasure
Chip erase time		—	5	—	s	Excludes 00H programming prior erasure
Word (16 bit width) programming time		—	16	3,600	µs	Excludes system-level overhead
Erase/Program cycle	—	10,000	—	—	cycle	
Data holding time	—	100,000	—	—	h	

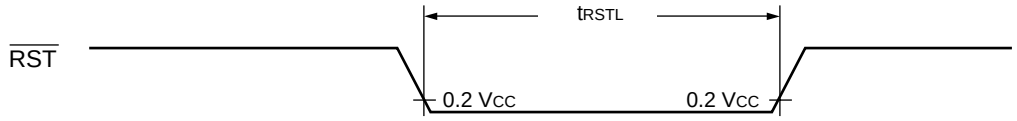
(2) Reset

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

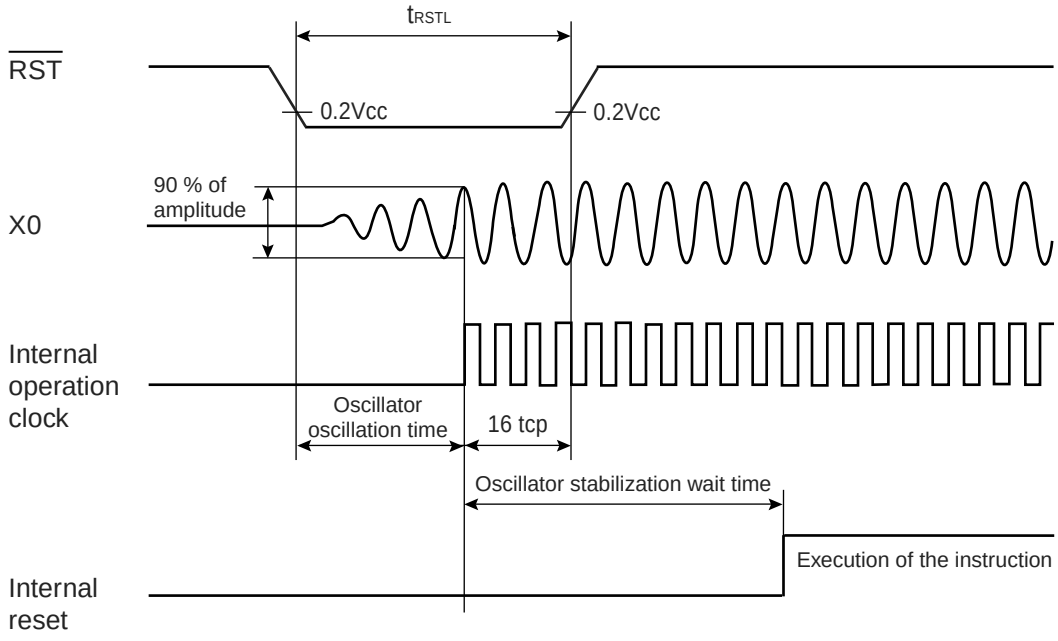
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTL}	$\overline{RST}$	—	16 t_{CP}	—	ns	In normal operation
				Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode

*: Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a ceramic oscillator, this is several hundred µs to a few ms, and for an external clock this is 0 ms.

• In normal operation



• In stop mode



(4) UART0 and UART1

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Serial clock cycle time	t_{SCYC}	SCK0, SCK1	Internal shift clock mode, output pin load is C_L = 80 pF + 1 TTL	8 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		–80	80	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		100	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
Serial clock “H” pulse width	t_{SHSL}	SCK0, SCK1	External shift clock mode, output pin load is C_L = 80 pF + 1 TTL	4 t_{CP}	—	ns	
Serial clock “L” pulse width	t_{SLSH}	SCK0, SCK1		4 t_{CP}	—	ns	
SCK ↓ → SOT delay time	t_{SLOV}	SCK0, SCK1 SOT0, SOT1		—	150	ns	
Valid SIN → SCK ↑	t_{IVSH}	SCK0, SCK1 SIN0, SIN1		60	—	ns	
SCK ↑ → valid SIN hold time	t_{SHIX}	SCK0, SCK1 SIN0, SIN1		60	—	ns	

Notes : • These are the AC ratings for CLK synchronous mode.
• CV is the load capacitor connected to the pin for testing.
• t_{CP} is the machine cycle period (unit = ns)

5. Electrical Characteristics for the A/D Converter

(MB90567/568/F568 : T_A = –40 °C to +85 °C, 2.7 V ≤ AVR, V_{CC} = AV_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

(MB90V560 : T_A = +25 °C, 3.0 V ≤ AVR, V_{CC} = AV_{CC} = 3.0 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Value			Unit	Remarks
			Min.	Typ.	Max.		
Resolution	—	—	—	—	10	bit	
Total error	—	—	—	—	±3.0	LSB	
Non-linearity error	—	—	—	—	±2.5	LSB	
Differential linearity error	—	—	—	—	±1.9	LSB	
Zero transition voltage	V_{OT}	AN0 to AN7	AV_{SS} –1.5 LSB	AV_{SS} +0.5 LSB	AV_{SS} +2.5 LSB	V	1 LSB = (AVR–AV_{SS}/ 1024
Full-scale transition voltage	V_{FST}	AN0 to AN7	AVR –3.5 LSB	AVR –1.5 LSB	AVR +0.5 LSB	V	
Conversion time	—	—	—	66 t_{CP}	—	ns	
Sampling time	—	—	—	32 t_{CP}	—	ns	
Analog port input current	I_{AIN}	AN0 to AN7	—	—	10	µA	
Analog input voltage	V_{AIN}	AN0 to AN7	0	—	AVR	V	
Reference voltage	—	AVR	2.7	—	AV_{CC}	V	
Power supply current	I_A	AV_{CC}	—	1	5	mA	
	I_{AH}	AV_{CC}	—	—	5	µA	*
Reference voltage supply current	I_R	AVR	—	100	200	µA	
	I_{RH}	AVR	—	—	5	µA	*
Variation between channels	—	AN0 to AN7	—	—	4	LSB	

* : Current when A/D converter is not used and CPU is in stop mode (V_{CC} = AV_{CC} = AVR = 3.3 V)

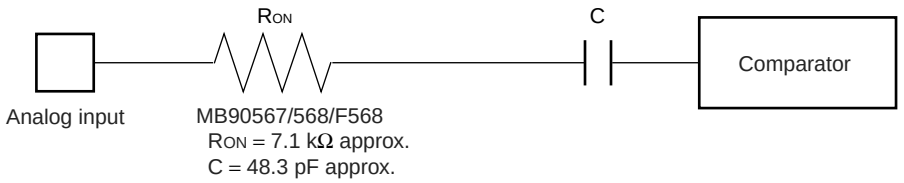
Notes : • The L reference voltage is fixed to AV_{SS}. The relative error increases as AVR becomes smaller.

- Ensure that the output impedance of the external circuit connected to the analog input meets the following condition :

  Output impedance of MB90F568 external circuit ≤ 14 kΩ (Sampling Time = 4 µs)

  Output impedance of MB90567/568 external circuit ≤ 7 kΩ (Sampling Time = 4 µs)
- If the output impedance of the external circuit is too high, the analog voltage sampling time may be too short.

- **Equivalent circuit of analog input circuit**



Note : The values listed are an indication only.

MEMO

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