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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	51
Program Memory Size	32KB (32K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	1K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90561apmc-g-417e1

FUJITSU MICROELECTRONICS
DATA SHEET

DS07-13715-5E

16-bit Proprietary Microcontrollers

CMOS

F²MC-16LX MB90560/565 Series

MB90561A/562A/F562B/V560/567/568/F568

■ DESCRIPTION

The MB90560/565 series is a general-purpose 16-bit microcontroller designed for industrial, OA, and process control applications that require high-speed real-time processing. The device features a multi-function timer able to output a programmable waveform.

The microcontroller instruction set is based on the same AT architecture as the F²MC-8L and F²MC-16L families with additional instructions for high-level languages, extended addressing modes, enhanced signed multiplication and division instructions, and a complete range of bit manipulation instructions. The microcontroller has a 32-bit accumulator for processing long word (32-bit) data.

Note: F²MC is the abbreviation of FUJITSU Flexible Microcontroller.

■ FEATURES

- **Clock**
  - Internal oscillator circuit and PLL clock multiplication circuit
  - Oscillation clock
    Clock speed selectable from either the machine clock, main clock, or PLL clock. The main clock is the oscillation clock divided into 2 (0.5 MHz to 8 MHz for a 1 MHz to 16 MHz base oscillation) . The PLL clock is the oscillation clock multiplied by one to four (4 MHz to 16 MHz for a 4 MHz base oscillation) .
  - Minimum instruction execution time : 62.5 ns (for oscillation = 4 MHz, PLL clock setting = × 4, V_{CC} = 5.0 V)
- **Maximum CPU memory space : 16 MB**
  - 24-bit addressing
  - Bank addressing

(Continued)

The information for microcontroller supports is shown in the following homepage.
Be sure to refer to the "Check Sheet" for the latest cautions on development.

"Check Sheet" is seen at the following support page

"Check Sheet" lists the minimal requirement items to be checked to prevent problems beforehand in system development.

http://edevice.fujitsu.com/micom/en-support/

2008.9

(Continued)

- **Instruction set**
  - Bit, byte, word, and long word data types
  - 23 different addressing modes
  - Enhanced calculation precision using a 32-bit accumulator
  - Enhanced signed multiplication and division instructions and RETI instruction
- **Instruction set designed for high level language (C) and multi-tasking**
  - Uses a system stack pointer
  - Symmetric instruction set and barrel shift instructions
- **Program patch function (2 address pointers) .**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 32 interrupts
- **Data transfer function**
  - Extended intelligent I/O service function : Up to 16 channels
- **Low-power consumption modes**
  - Sleep mode (CPU operating clock stops.)
  - Timebase timer mode (Only oscillation clock and timebase timer continue to operate.)
  - Stop mode (Oscillation clock stops.)
  - CPU intermittent operation mode (The CPU operates intermittently at the specified interval.)
- **Package**
  - LQFP-64P (FTP-64P-M23 : 0.65 mm pin pitch)
  - QFP-64P (FTP-64P-M06 : 1.00 mm pin pitch)
  - SH-DIP (DIP-64P-M01 : 1.778 mm pin pitch)
- **Process : CMOS technology**

■ PERIPHERAL FUNCTIONS (RESOURCES)

- **I/O ports : 51 ports (max.)**
- **Timebase timer : 1 channel**
- **Watchdog timer : 1 channel**
- **16-bit reload timer : 2 channels**
- **Multi-function timer**
  - 16-bit free-run timer : 1 channel
  - Output compare : 6 channels
    Can output an interrupt request when a match occurs between the count in the 16-bit freerun timer and the value set in the compare register.
  - Input capture : 4 channels
    On detecting an active edge on the input signal from an external input pin, copies the count value of the 16-bit freerun timer to the input capture data register and generates an interrupt request.
  - 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) The period and duty of the output pulse can be set by the program.
  - Waveform generator (8-bit timer : 3 channels)
- **UART** : **2 channels**
  - Full-duplex, double-buffered (8-bit)
  - Can be set to asynchronous or clock synchronous serial transfer (I/O expansion serial) operation
- **DTP/external interrupt circuit (8 channels)**
  - External interrupts can activate the extended intelligent I/O service.
  - Generates interrupts in response to external interrupt inputs.

- **Delayed interrupt generation module**
  - Generates an interrupt request for task switching.
- **8/10-bit A/D converter : 8 channels**
  - 8-bit or 10-bit resolution selectable

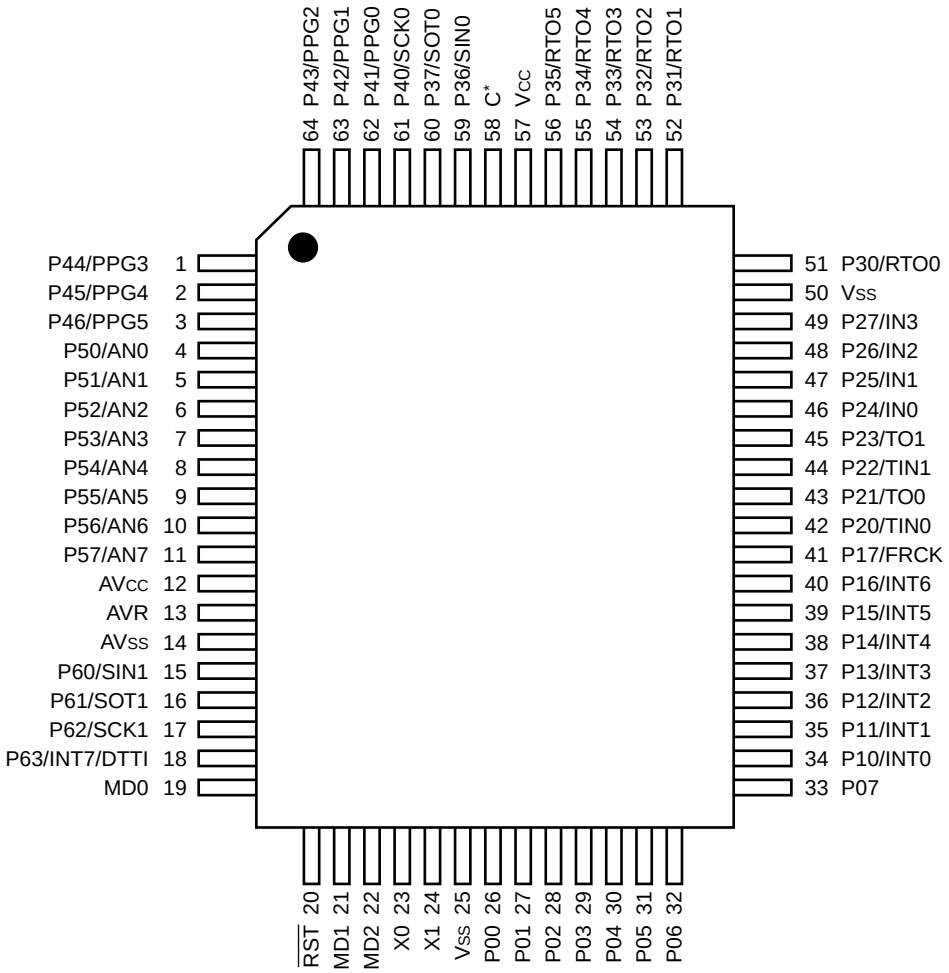
2. MB90565 Series

Part Number	MB90F568	MB90568	MB90567
Classification	Internal flash memory product	Internal mask ROM product	
ROM size	128 Kbytes		96 Kbytes
RAM size	4 Kbytes		4 Kbytes
Dedicated emulator power supply*	—		—
CPU functions	Number of instructions : 351 Minimum instruction execution time : 62.5 ns for a 4 MHz oscillation (with ×4 multiplier) Addressing modes : 23 modes Program patch function : 2 address pointers Maximum memory space : 16 Mbytes		
Ports	I/O ports (CMOS) : 51		
UART	Full-duplex, double-buffered Clock synchronous or asynchronous operation selectable Can be used as I/O serial Internal dedicated baud rate generator 2 channels		
16-bit reload timer	16-bit reload timer operation 2 channels		
Multi-function timer	16-bit free-run timer × 1 channel Output compare × 6 channels Input capture × 4 channels 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) Waveform generator (8-bit timer × 3 channels) 3-phase waveform output, deadtime output		
8/10-bit A/D converter	8 channels (multiplexed input) 8-bit or 10-bit resolution selectable Conversion time : 6.13 µs (min.) (for maximum machine clock speed 16 MHz)		
DTP/external interrupts	8 channels (8 channels available, shared with A/D input) Interrupt triggers : “L” → “H” edge, “H” → “L” edge, “L” level, “H” level (selectable)		
Low power consumption modes	Sleep mode, timebase timer mode, stop mode, and CPU intermittent operation mode		
Process	CMOS		
Operating voltage	3.3 V ± 0.3 V		

* : DIP switch setting (S2) when using the emulation pod (MB2145-507) .
Refer to “2.7 Dedicated Emulator Power Supply” in the “MB2145-507 Hardware Manual” for details.

■ PIN ASSIGNMENTS

(TOP VIEW)

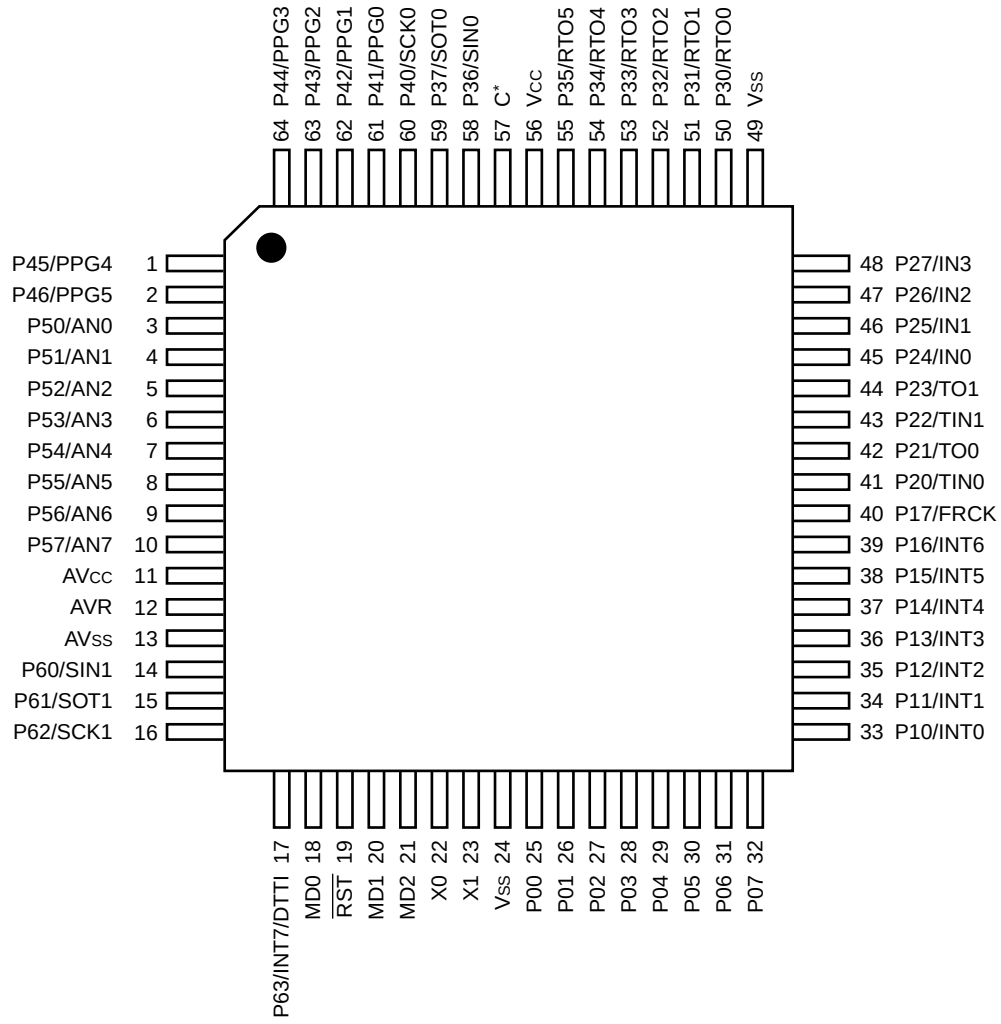


(FPT-64P-M06)

* : N.C. on the MB90F568, MB90567, and MB90568.

(Continued)

(TOP VIEW)



(FPT-64P-M23)

* : N.C. on the MB90F568, MB90567, and MB90568.

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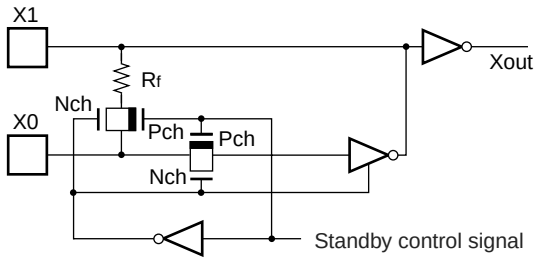
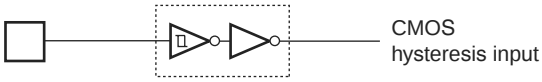
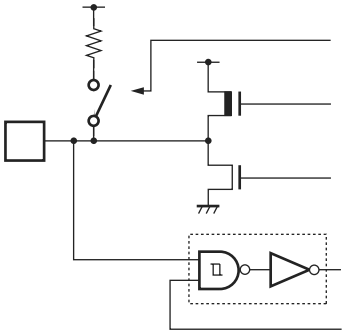
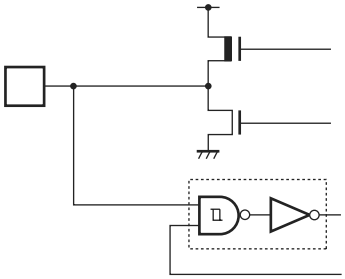
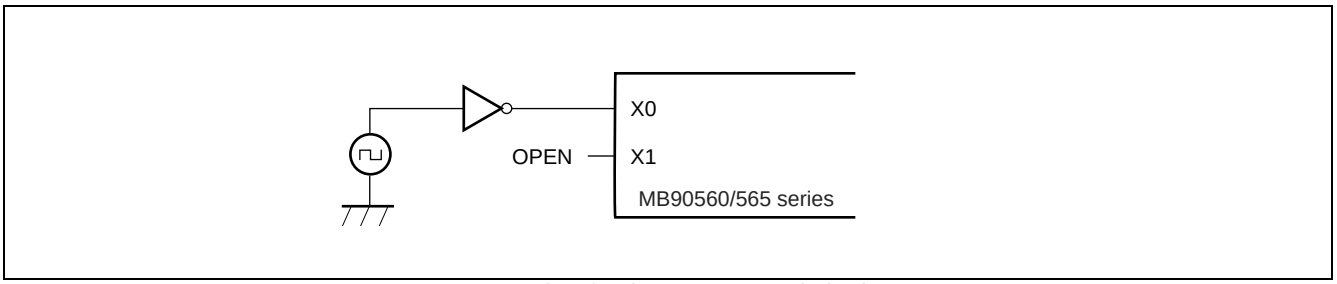
■ I/O CIRCUITS

Type	Circuit	Remarks
A		• Oscillation circuit Internal oscillation feedback resistor (R_f)
B		• CMOS hysteresis input
C		• CMOS hysteresis I/O pin with pull-up control CMOS output CMOS hysteresis input (with input cut-off function in standby mode) Internal pull-up resistor (R_p) < Note > • The pull-up resistor is active when the port is set as an input.
D		• CMOS hysteresis I/O pin CMOS output CMOS hysteresis input (with input cut-off function in standby mode) < Notes > • The I/O port output and internal resource output share the same output buffer. • The I/O port input and internal resource input share the same input buffer.

(Continued)



Example of using an external clock

(7) Power supply pins

The multiple V_{CC} and V_{SS} pins are connected together in the internal device design so as to prevent misoperation such as latch-up. However, always connect all V_{CC} and V_{SS} pins to the same potential externally to minimize spurious radiation, prevent misoperation of strobe signals due to increases in the ground level, and maintain the overall output current rating.

Also, ensure that the impedance of the V_{CC} and V_{SS} connections to the power supply is as low as possible. To minimize these problems, connect a bypass capacitor of approximately 0.1 µF between V_{CC} and V_{SS}. Connect the capacitor close to the V_{CC} and V_{SS} pins.

(8) Sequence for connecting and disconnecting power supply

Do not apply voltage to the A/D converter power supply pins (AV_{CC}, AVR, AV_{SS}) or analog inputs (AN0 to AN7) until the digital power supply (V_{CC}) is turned on. When turning the device off, turn off the digital power supply after disconnecting the A/D converter power supply and analog inputs. When turning the power on or off, ensure that AVR does not exceed AV_{CC}.

When using the I/O ports that share pins with the analog inputs, ensure that the input voltage does not exceed AV_{CC} (turning the analog and digital power supplies on and off simultaneously is OK) .

(9) Conditions when output from ports 0 and 1 is undefined

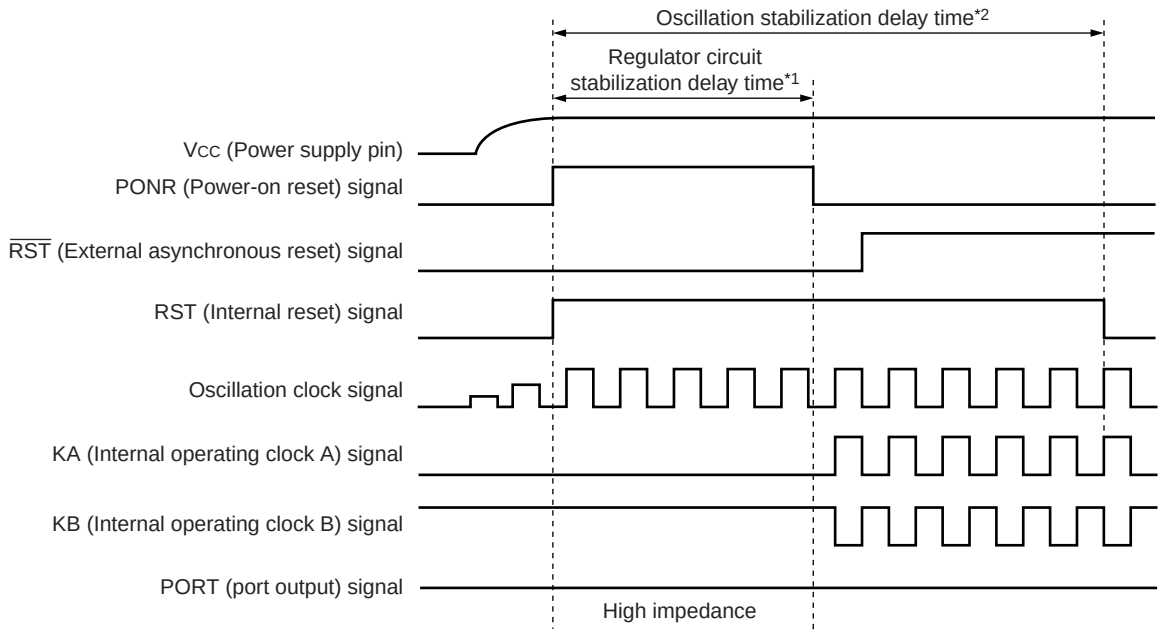
After turning on the power supply, the outputs from ports 0 and 1 are undefined during the oscillation stabilization delay time controlled by the regulator circuit (during the power-on reset) if the $\overline{RST}$ pin level is “H”. When the $\overline{RST}$ pin level is “L”, ports 0 and 1 go to high impedance.

Figures 1 and 2 show the timing (for the MB90F562B and MB90V560) .

Note that this undefined output period does not occur on products without an internal regulator circuit as these products do not have an oscillation stabilization delay time.

(MB90561A, MB90562A, MB90F568, MB90567 and MB90568)

• **Figure 2 Timing chart for ports 0 and 1 going to high impedance state (When $\overline{RST}$ pin level is "L")**



*1 : Regulator circuit oscillation stabilization delay time :
2^{17}/Oscillation clock frequency (approx. 8.19 ms for a 16 MHz oscillation clock frequency)

*2 : Oscillation stabilization delay time :
2^{18}/Oscillation clock frequency (approx. 16.38 ms for a 16 MHz oscillation clock frequency)

(10) Notes on using the DIV A, Ri and DIVW A, RWi instructions

The location in which the remainder value produced by the signed division instructions "DIV A, Ri" and "DIVW A, RWi" is stored depends on the bank register. The remainder is stored in an address in the memory bank specified in the bank register.

Set the bank register to "00_H" when using the "DIV A, Ri" and "DIVW A, RWi" instructions.

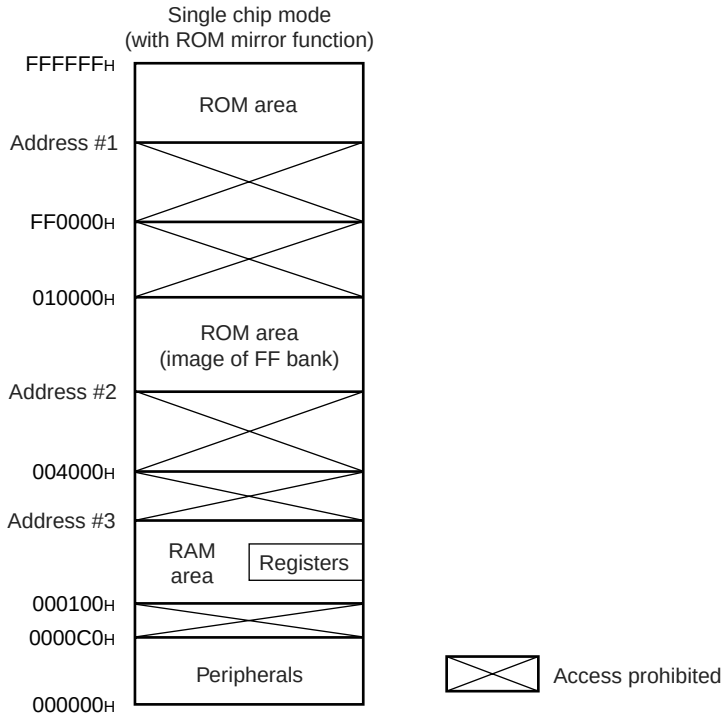
(11) Notes on using REALOS

The extended intelligent I/O service (EI^{2}OS) cannot be used when using REALOS.

(12) Caution on Operations during PLL Clock Mode

If the PLL clock mode is selected in the microcontroller, it may attempt to continue the operation using the free-running frequency of the self oscillation circuit in the PLL circuitry even if the oscillator is out of place or the clock input is stopped. Performance of this operation, however, cannot be guaranteed.

■ MEMORY MAP



Part No.	Address#1	Address#2	Address#3
MB90561A	FF8000H	008000H	000500H
MB90562A	FF0000H	004000H	000900H
MB90F562B	FF0000H	004000H	000900H
MB90567	FE8000H	004000H	001100H
MB90568	FE0000H	004000H	001100H
MB90F568	FE0000H	004000H	001100H
MB90V560	FE0000H*	004000H*	001100H

* : “V” products do not contain internal ROM. Treat this address as the ROM decode area used by the tools.

Memory map of MB90560/565 series

Notes : • When specified in the ROM mirror function register, the upper part of 00 bank (“004000H to 00FFFFH”) contains a mirror of the data in the upper part of FF bank (“FF4000H to FFFFFFH”) .
• See “10. ROM Mirror Function Selection Module” in the Peripheral Functions section for details of the ROM mirror function settings.

Remarks : • The ROM mirror function is provided so the C compiler’s small memory model can be used.
• The lower 16 bits of the FF bank and 00 bank addresses are the same. However, as the FF bank ROM area exceeds 48 KBytes, the entire ROM data area cannot be mirrored in 00 bank.
• When using the C compiler’s small memory model, locating data tables in the area “FF4000H to FFFFFFH” makes the image of the data visible in the “004000H to 00FFFFH” area. This means that data tables located in ROM can be referenced without needing to declare far pointers.

■ PERIPHERAL FUNCTIONS

1. I/O Ports

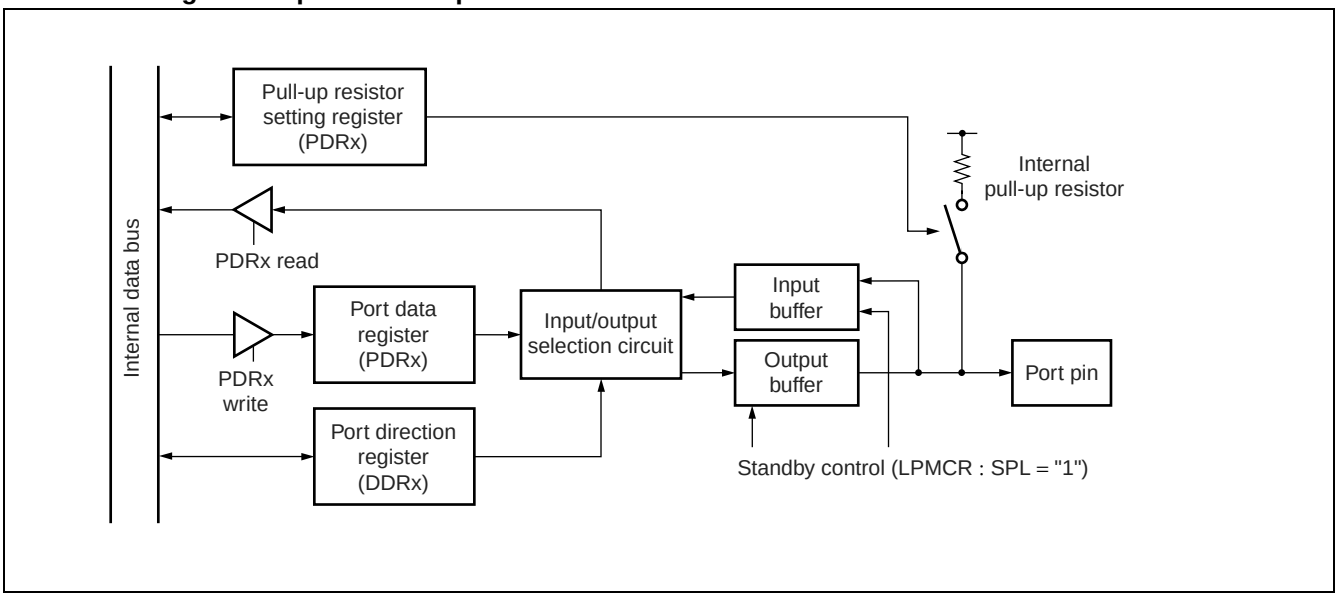
- The I/O ports can be used as general-purpose I/O ports (parallel I/O ports) . The MB90560/565 series have 7 ports (51 pins) . The ports share pins with the inputs and outputs of the peripheral functions.
- The port data registers (PDR) are used to output data to the I/O pins and read the data input from the I/O ports. Similarly, the port direction registers (DDR) set the I/O direction (input or output) for each individual port bit.
- The following table lists the I/O ports and the peripheral functions with which they share pins.

	Pin Name (Port)	Pin Name (Peripheral)	Peripheral Function that Shares Pin
Port 0	P00-P07	—	Not shared
Port 1	P10-P16	INT0-INT6	External interrupts
	P17	FRCK	Freerun timer external input
Port 2	P20-P23	TIN0, TO0, TIN1, TO1	16-bit reload timer 0 and 1
	P24-P27	IN0-IN3	Input capture 0 to 3
Port 3	P30-P35	RTO0-RTO5	Output compare
	P36, P37	SIN0, SOT0	UART0
Port 4	P40	SCK0	UART0
	P41-P46	PPG0-PPG5	8/16-bit PPG timer
Port 5	P50-P57	AN0-AN7	8/10-bit A/D converter
Port 6	P60-P62	SIN1, SOT1, SCK1	UART1
	P63	INT7	External interrupts
		DTTI	Waveform generator

Notes : • Pins P30 to P35 of port 3 can drive a maximum of I_{OL} = 12 mA.

• Port 5 shares pins with the analog inputs. When using port 5 pins as a general-purpose ports, ensure that the corresponding analog input enable register (ADER) bits are set to “0_B”. ADER is initialized to “FF_H” after a reset.

- **Block diagram for port 0 and 1 pins**



3. Watchdog Timer

- The watchdog timer is a timer/counter used to detect faults such as program runaway.
- The watchdog timer is a 2-bit counter that counts the clock signal from the timebase timer or watch timer.
- Once started, the watchdog timer must be cleared before the 2-bit counter overflows. If an overflow occurs, the CPU is reset.

- **Interval time for the watchdog timer**

HCLK : Oscillation Clock (4 MHz)		
Min.	**Max.**	**Clock Period**
Approx. 3.58 ms	Approx. 4.61 ms	$2^{14} \pm 2^{11}$ / HCLK
Approx. 14.33 ms	Approx. 18.30 ms	$2^{16} \pm 2^{13}$ / HCLK
Approx. 57.23 ms	Approx. 73.73 ms	$2^{18} \pm 2^{15}$ / HCLK
Approx. 458.75 ms	Approx. 589.82 ms	$2^{18} \pm 2^{15}$ / HCLK

Notes : • The difference between the maximum and minimum watchdog timer interval times is due to the timing when the counter is cleared.

• As the watchdog timer is a 2-bit counter that counts the carry-up signal from the timebase timer or watch timer, clearing the timebase timer (when operating on HCLK) or the watch timer (when operating on SCLK) lengthens the time until the watchdog timer reset is generated.

- **Watchdog timer count clock**

WTC : WDCS	HCLK : Oscillation clock PCLK : PLL clock
"0"	Prohibited setting
"1"	Count the timebase timer output.

- **Events that stop the watchdog timer**

1 : Stop due to a power-on reset

2 : Watchdog reset

- **Events that clear the watchdog timer**

1 : External reset input from the $\overline{\text{RST}}$ pin.

2 : Writing "0" to the software reset bit.

3 : Writing "0" to the watchdog control bit (second and subsequent times) .

4 : Changing to sleep mode (clears the watchdog timer and temporarily halts the count) .

5 : Changing to timebase timer mode (clears the watchdog timer and temporarily halts the count) .

6 : Changing to stop mode (clears the watchdog timer and temporarily halts the count) .

- An interrupt can be generated when an active edge is detected on the external signal (ICS01, ICS23 : ICE0 = “1”, ICE1 = “1”, ICE2 = “1”, ICE3 = “1”) .

- **8/16-bit PPG timer** (**8-bit** : **6 channels**, **16-bit** : **3 channels**)

The 8/16-bit PPG timer consists of an 8-bit down counter (PCNT) , PPG control registers (PPGC0 to PPGC 5) , PPG clock control registers (PCS01, PCS23, PCS45) , and PPG reload registers (PRLL0 to PRLL5, PRLH0 to PRLH5) .
When used as an 8/16-bit reload timer, the PPG operates as an event timer. The PPG can also be used to output pulses with specified frequency and duty ratio.

- 8-bit PPG mode
  Each channel operates as an independent 8-bit PPG.
- 8-bit prescaler + 8-bit PPG mode
  ch0 (ch2, ch4) operates as an 8-bit prescaler and ch1 (ch3, ch5) operates as a variable frequency PPG by counting up on the borrow output from ch0 (ch2, ch4) .
- 16-bit PPG mode
  ch0 (ch2, ch4) and ch1 (ch3, ch5) operate together as a 16-bit PPG.
- PPG operation
  Outputs pulses with the specified frequency and duty ratio (ratio of “H” level period and “L” level period), and can also be used as a D/A converter when combined with an external circuit.

- **Waveform generator**

The waveform generator consists of an 8-bit timer, 8-bit timer control registers (DTCR0 to DTCR2) , 8-bit reload registers (TMRR0 to TMRR2) , and waveform control register (SIGCR) .

The waveform generator can generate a DC chopper output or non-overlapping three-phase waveform output for inverter control using the realtime outputs (RT0 to RT5) and 8/16-bit PPG timer.

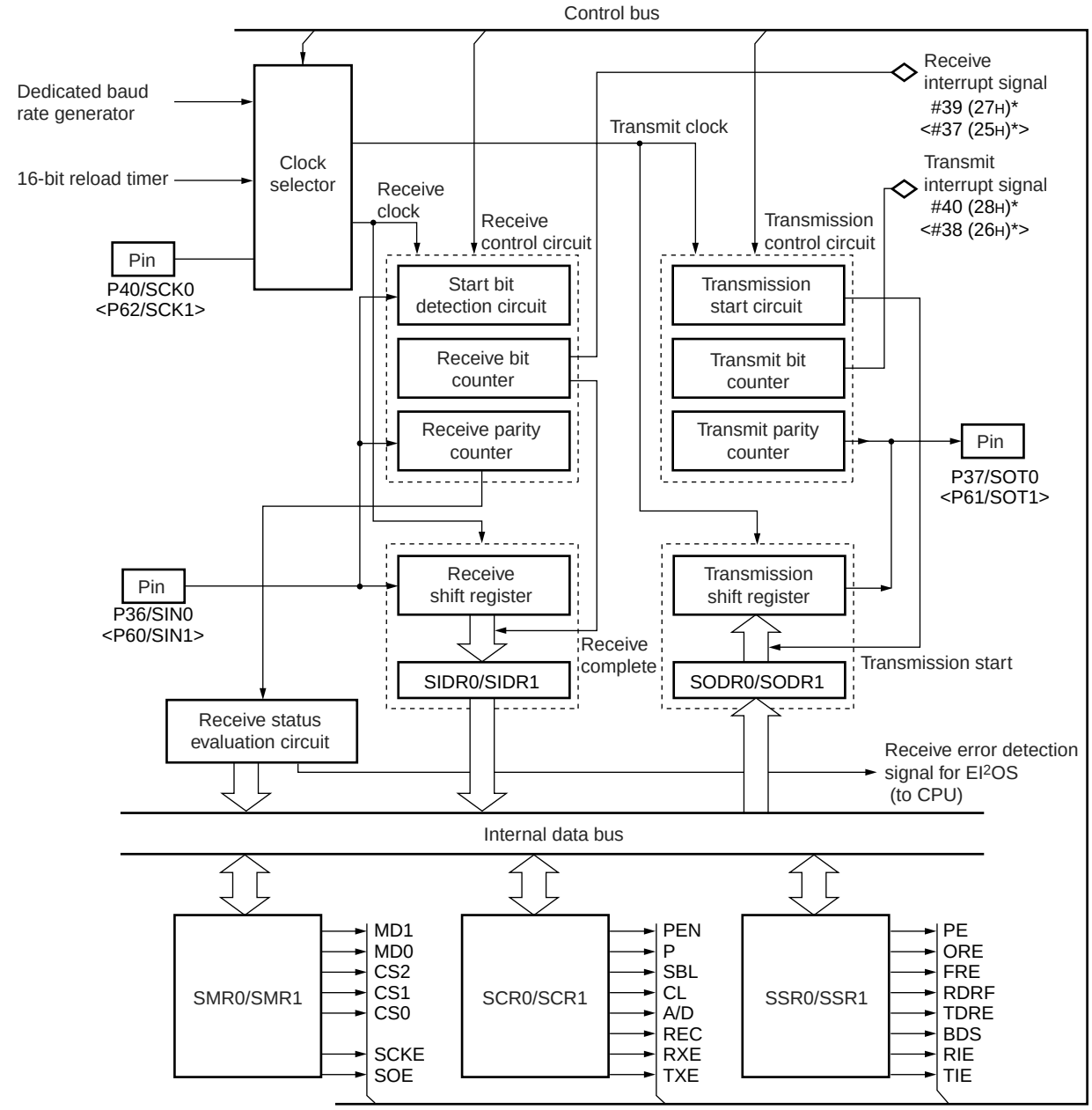
- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the PPG timer pulse output. (Deadtime timer function)
- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the realtime outputs (RT1, RT3, RT5) . (Deadtime timer function)
- A GATE signal can be generated when a match occurs between the count from the 16-bit freerun timer and compare register in the output compare (OCCP0 to OCCP5) (rising edge on realtime output (RT)) to control the PPG timer operation. (GATE function)
- Can control the RTO0 to RTO5 pin outputs using the DTTI pin input.
  By making the DTTI pin input clockless, the pins can be controlled externally even when the oscillation clock is halted. (The level for each pin can be set by the program.) However, the I/O ports (P30 to P35) must have been set beforehand as outputs and the output values set in the port 3 data register (PDR3) .

(2) UART structure

The UART consists of the following 11 blocks:

- Clock selector
- Receive control circuit
- Transmission control circuit
- Receive status evaluation circuit
- Receive shift register
- Transmission shift register
- Mode registers (SMR0, SMR1)
- Control registers (SCR0, SCR1)
- Status registers (SSR0, SSR1)
- Input data registers (SIDR0, SIDR1)
- Output data registers (SODR0, SODR1)

- **Block diagram**



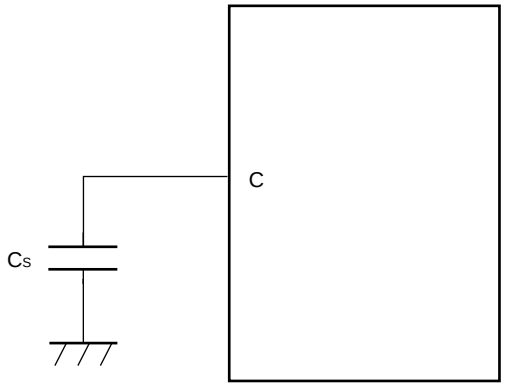
* : Interrupt number

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	5.5	V	Normal operation (MB90562A, MB90561A, and MB90V560)
		4.5	5.5	V	Normal operation (MB90F562B)
	V_{CC}	3.0	5.5	V	Maintaining state in stop mode
Input “H” voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD input pin
Smoothing capacitor	C_S	0.1	1.0	µF	Use a ceramic capacitor or other capacitor with equivalent frequency characteristics. The capacitance of the smoothing capacitor connected to the V_{CC} pin must be greater than C_S.
Operating temperature	T_A	–40	+85	°C	

• C pin diagram



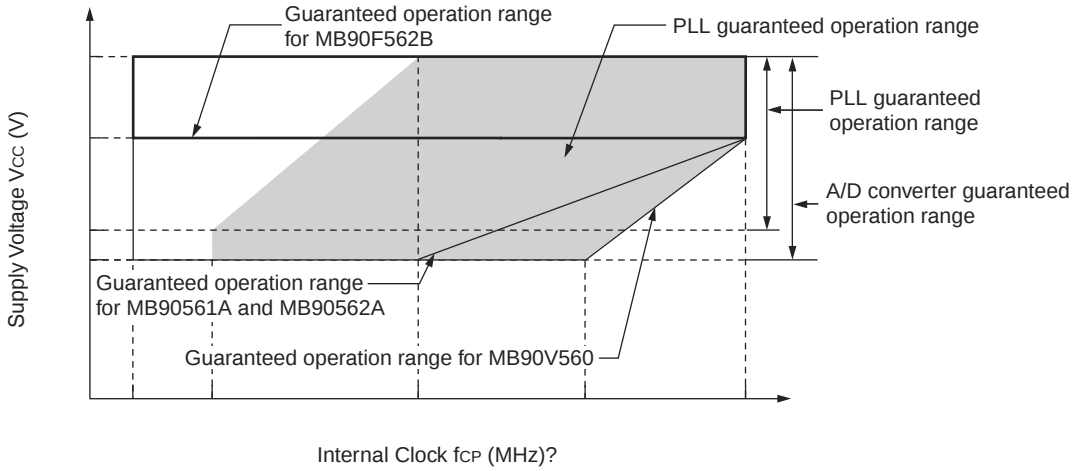
WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

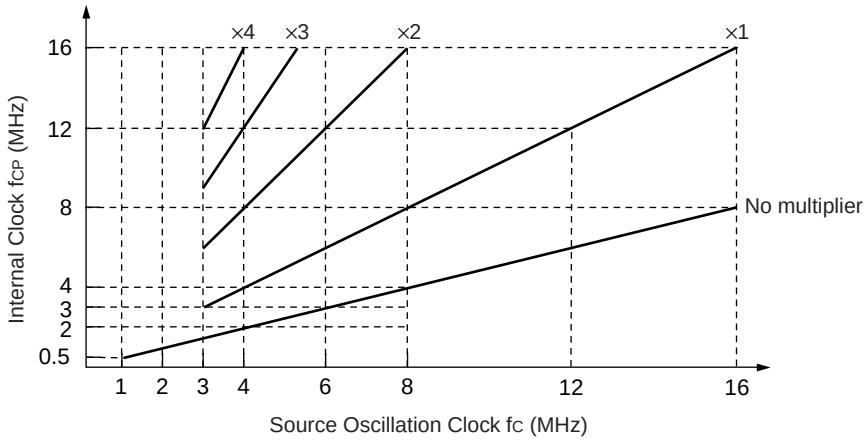
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

• **PLL guaranteed operation range**

Relationship between internal operating clock frequency and power supply voltage



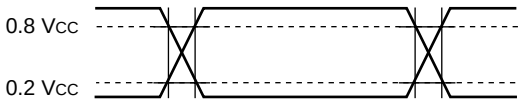
Relationship between oscillation frequency and internal operating clock frequency



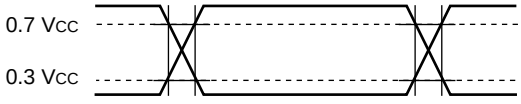
The AC ratings are specified for the following measurement reference voltages.

• **Input signal waveform**

Hysteresis input pin

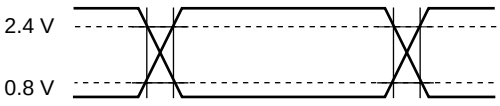


Pins other than hysteresis input or MD input pins



• **Output signal waveform**

Output pin



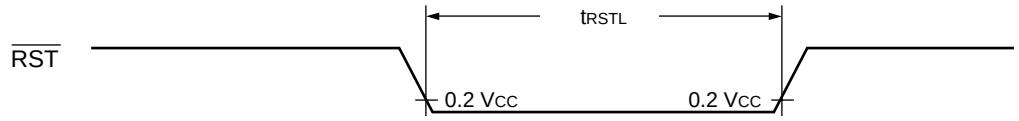
(2)Reset

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

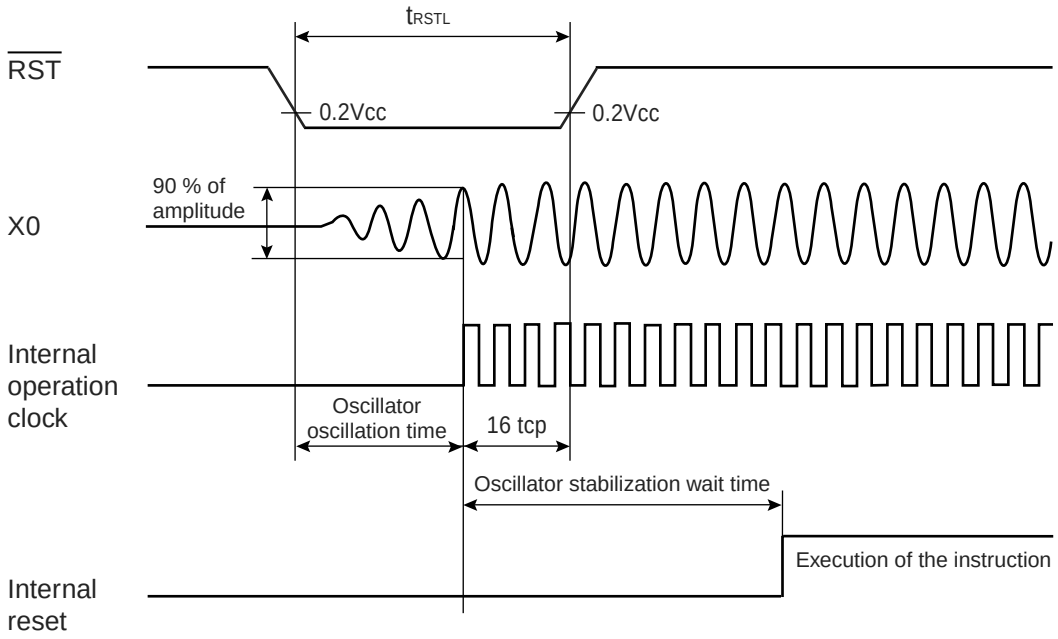
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Reset input time	t_{RSTH}	$\overline{RST}$	—	16 t_{CP}	—	ns	In normal operation
				Oscillator oscillation time* + 16 t_{CP}	—	ms	In stop mode

*: Oscillator oscillation time is the time to reach 90% amplitude. For a crystal oscillator, this is a few to several dozen ms; for a ceramic oscillator, this is several hundred µs to a few ms, and for an external clock this is 0 ms.

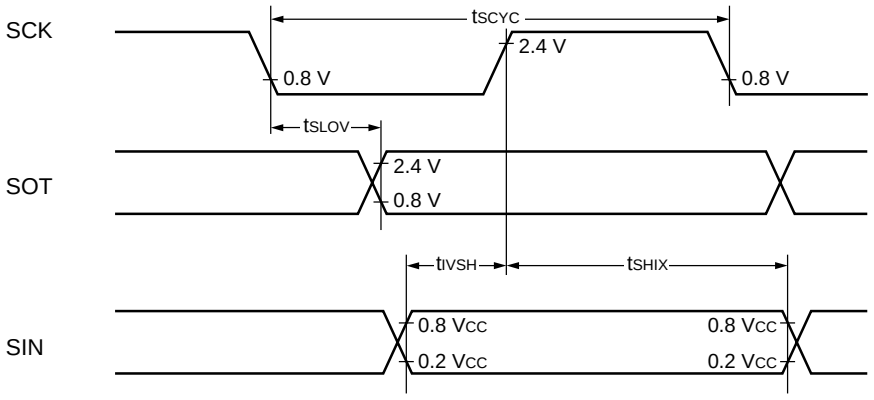
• In normal operation



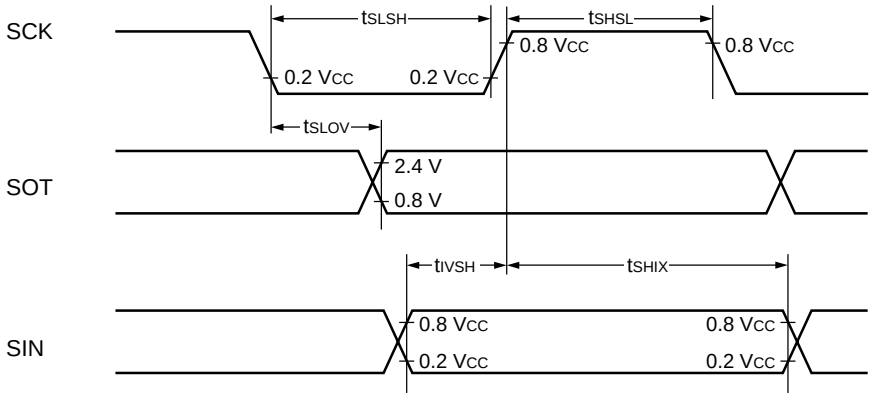
• In stop mode



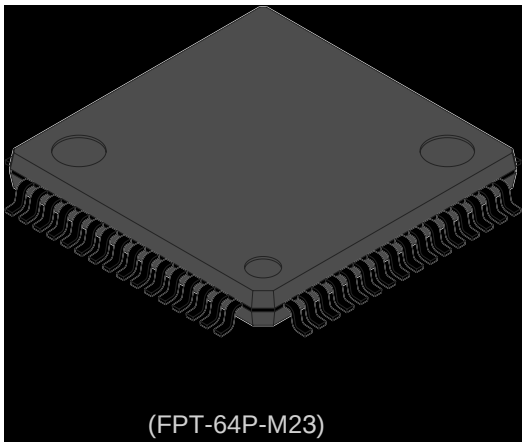
- **Internal shift clock mode**



- **External shift clock mode**



(Continued)



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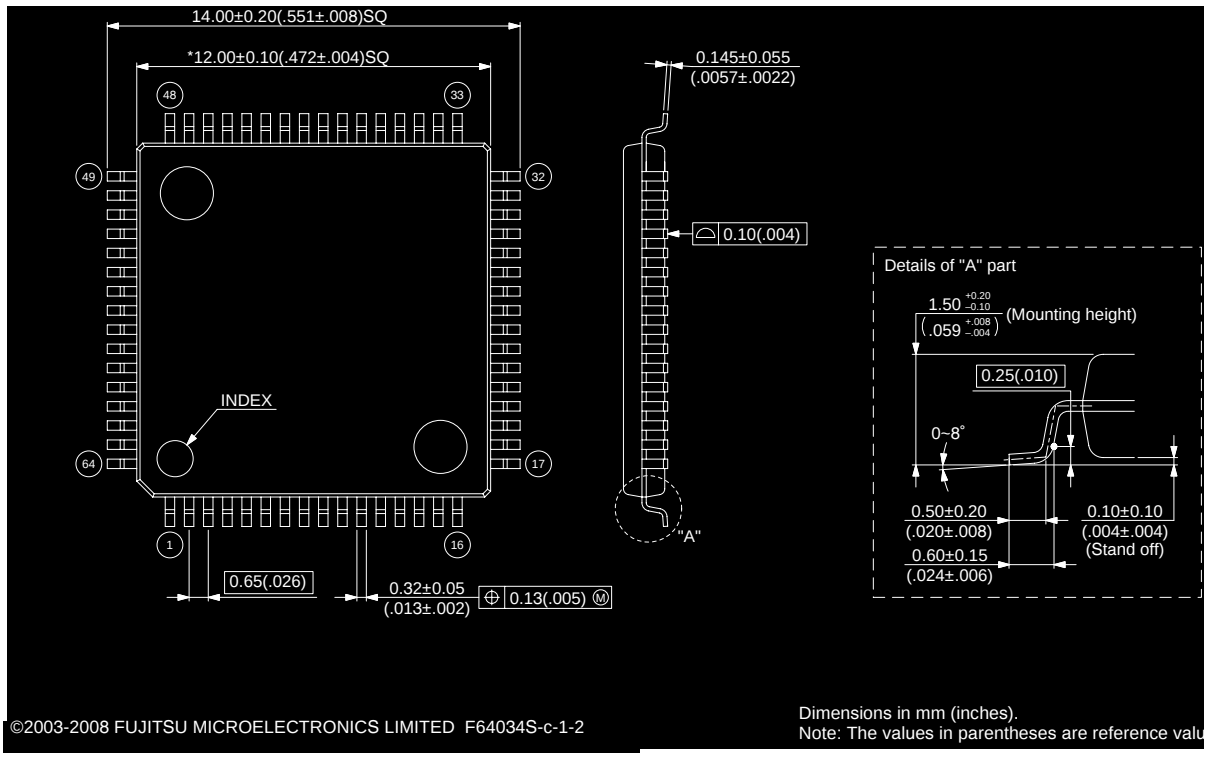

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