Infineon Technologies - MB90562APMC-GS-454E1 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	F²MC-16LX
Core Size	16-Bit
Speed	16MHz
Connectivity	UART/USART
Peripherals	POR, WDT
Number of I/O	51
Program Memory Size	64KB (64K x 8)
Program Memory Type	Mask ROM
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 8x8/10b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb90562apmc-gs-454e1

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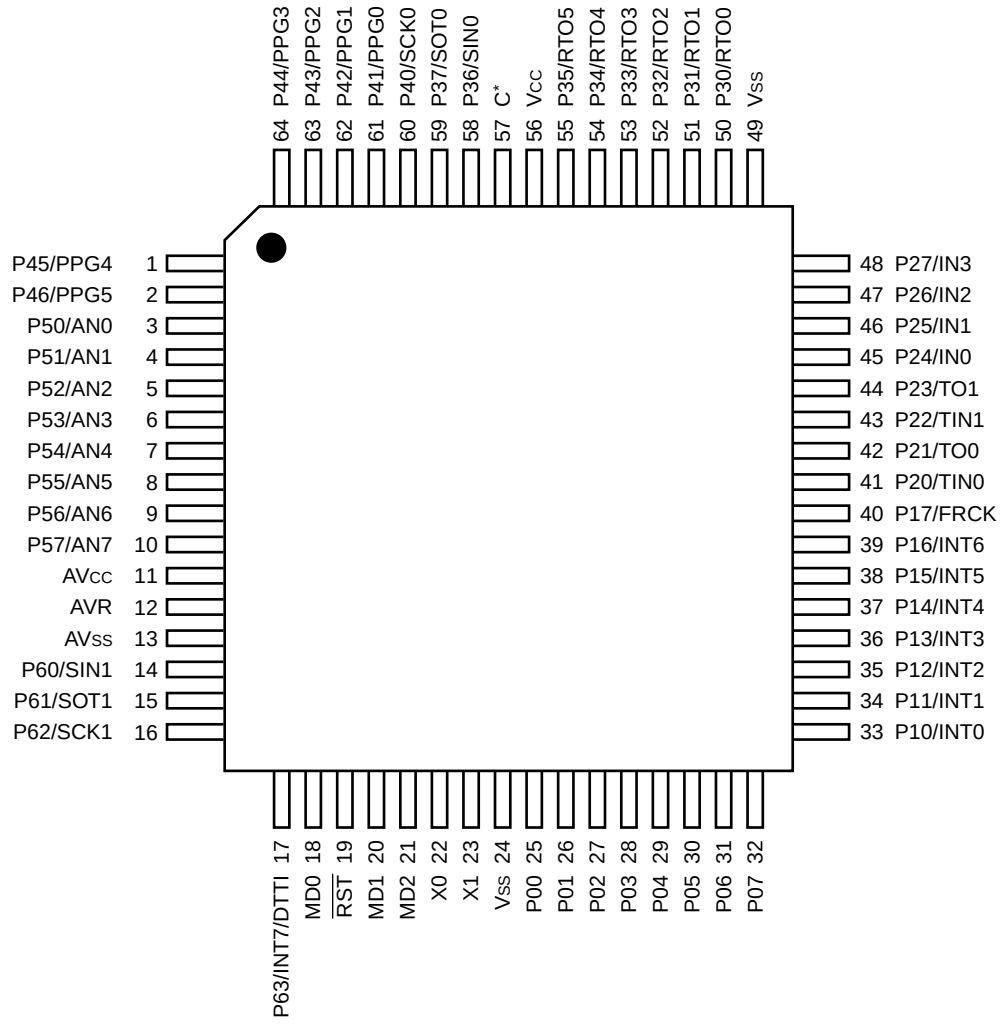
- **Instruction set**
  - Bit, byte, word, and long word data types
  - 23 different addressing modes
  - Enhanced calculation precision using a 32-bit accumulator
  - Enhanced signed multiplication and division instructions and RETI instruction
- **Instruction set designed for high level language (C) and multi-tasking**
  - Uses a system stack pointer
  - Symmetric instruction set and barrel shift instructions
- **Program patch function (2 address pointers) .**
- **4-byte instruction queue**
- **Interrupt function**
  - Priority levels are programmable
  - 32 interrupts
- **Data transfer function**
  - Extended intelligent I/O service function : Up to 16 channels
- **Low-power consumption modes**
  - Sleep mode (CPU operating clock stops.)
  - Timebase timer mode (Only oscillation clock and timebase timer continue to operate.)
  - Stop mode (Oscillation clock stops.)
  - CPU intermittent operation mode (The CPU operates intermittently at the specified interval.)
- **Package**
  - LQFP-64P (FTP-64P-M23 : 0.65 mm pin pitch)
  - QFP-64P (FTP-64P-M06 : 1.00 mm pin pitch)
  - SH-DIP (DIP-64P-M01 : 1.778 mm pin pitch)
- **Process : CMOS technology**

■ PERIPHERAL FUNCTIONS (RESOURCES)

- **I/O ports : 51 ports (max.)**
- **Timebase timer : 1 channel**
- **Watchdog timer : 1 channel**
- **16-bit reload timer : 2 channels**
- **Multi-function timer**
  - 16-bit free-run timer : 1 channel
  - Output compare : 6 channels
    Can output an interrupt request when a match occurs between the count in the 16-bit freerun timer and the value set in the compare register.
  - Input capture : 4 channels
    On detecting an active edge on the input signal from an external input pin, copies the count value of the 16-bit freerun timer to the input capture data register and generates an interrupt request.
  - 8/16-bit PPG timer (8-bit × 6 channels or 16-bit × 3 channels) The period and duty of the output pulse can be set by the program.
  - Waveform generator (8-bit timer : 3 channels)
- **UART** : **2 channels**
  - Full-duplex, double-buffered (8-bit)
  - Can be set to asynchronous or clock synchronous serial transfer (I/O expansion serial) operation
- **DTP/external interrupt circuit (8 channels)**
  - External interrupts can activate the extended intelligent I/O service.
  - Generates interrupts in response to external interrupt inputs.

(TOP VIEW)



(FPT-64P-M23)

* : N.C. on the MB90F568, MB90567, and MB90568.

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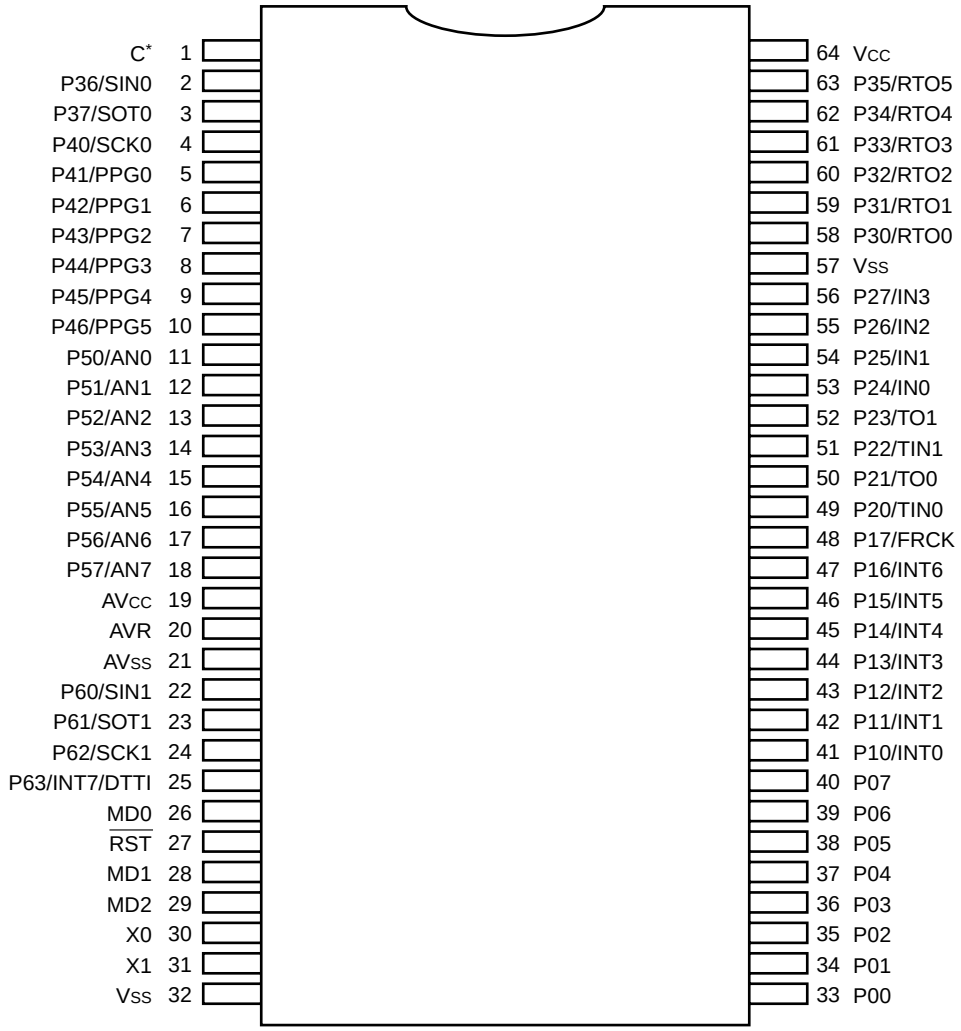
(TOP VIEW)



(DIP-64P-M01)
(Only support MB90F562B, MB90561A, and MB90562A.)

* : Not support on the MB90F568, MB90567, and MB90568.

Pin No.			Pin Name	Circuit Type*1	State/ Function at Reset	Description
QFP*3	LQFP*4	SDIP*5				
51 to 56	50 to 55	58 to 63	P30 to P35	E	Port inputs (Hi-Z)	I/O ports
			RTO0 to RTO5			Event output pins for the output compare and waveform generator output pins. The pins output the specified waveform generated by the waveform generator. If not using waveform generation, these terminals enable output compare event output to use as output compare outputs. When used as a port, set the corresponding bits in the analog input enable register (ADER) to “port”.
59	58	2	P36	D		I/O port
			SIN0			Serial data input pin for UART ch0. This pin is used continuously when input operation is enabled for UART ch0. In this case, do not use as a general input pin.
60	59	3	P37	D		I/O port
			SOT0			Serial data output pin for UART ch0. Output operates when UART ch0 output is enabled.
61	60	4	P40	D		I/O port
			SCK0			Serial clock I/O pin for UART ch0. Output operates when UART ch0 clock output is enabled.
62 to 64, 1 to 3	61 to 64, 1, 2	5 to 10	P41 to P46	D		I/O ports
			PPG0 to PPG5			Output pins for PPG ch0 to ch5. The outputs operate when output is enabled for PPG ch0 to ch5.
4 to 11	3 to 10	11 to 18	P50 to P57	F	Analog inputs	I/O ports
			AN0 to AN7			Analog input pins for the A/D converter. Input is available when the corresponding analog input enable register bits are set. (ADER : bit0 to bit7)
12	11	19	AV_{CC}	—	Power supply input	V_{CC} power supply input pin for A/D converter.
13	12	20	AVR	G	Reference voltage input	Reference voltage input pin for A/D converter. Ensure that the voltage does not exceed V_{CC}.
14	13	21	AV_{SS}	—	Power supply input	V_{SS} power supply input pin for A/D converter.

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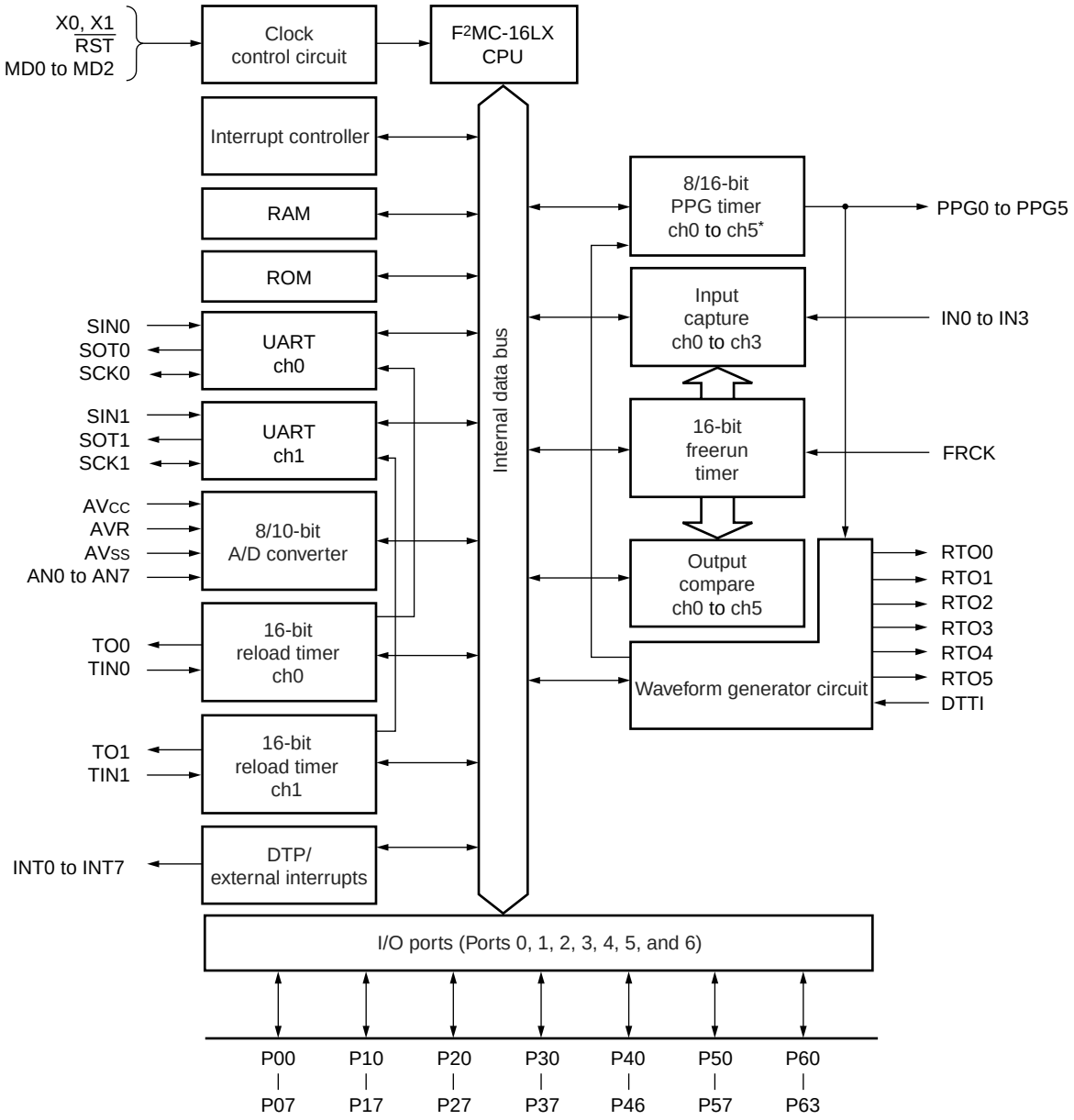
■ BLOCK DIAGRAM



* : Channel numbers when used as 8-bit timers. Three channels (ch1, ch3, and ch5) are available when used as 16-bit timers.

Note: The I/O ports share pins with the various peripheral functions (resources) .
See the Pin Assignment and Pin Description sections for details.
Note that, if a pin is used by a peripheral function (resource) , it may not be used as an I/O port.

- An interrupt can be generated when an active edge is detected on the external signal (ICS01, ICS23 : ICE0 = “1”, ICE1 = “1”, ICE2 = “1”, ICE3 = “1”) .

- **8/16-bit PPG timer** (**8-bit** : **6 channels**, **16-bit** : **3 channels**)

The 8/16-bit PPG timer consists of an 8-bit down counter (PCNT) , PPG control registers (PPGC0 to PPGC 5) , PPG clock control registers (PCS01, PCS23, PCS45) , and PPG reload registers (PRLL0 to PRLL5, PRLH0 to PRLH5) .
When used as an 8/16-bit reload timer, the PPG operates as an event timer. The PPG can also be used to output pulses with specified frequency and duty ratio.

- 8-bit PPG mode
  Each channel operates as an independent 8-bit PPG.
- 8-bit prescaler + 8-bit PPG mode
  ch0 (ch2, ch4) operates as an 8-bit prescaler and ch1 (ch3, ch5) operates as a variable frequency PPG by counting up on the borrow output from ch0 (ch2, ch4) .
- 16-bit PPG mode
  ch0 (ch2, ch4) and ch1 (ch3, ch5) operate together as a 16-bit PPG.
- PPG operation
  Outputs pulses with the specified frequency and duty ratio (ratio of “H” level period and “L” level period), and can also be used as a D/A converter when combined with an external circuit.

- **Waveform generator**

The waveform generator consists of an 8-bit timer, 8-bit timer control registers (DTCR0 to DTCR2) , 8-bit reload registers (TMRR0 to TMRR2) , and waveform control register (SIGCR) .

The waveform generator can generate a DC chopper output or non-overlapping three-phase waveform output for inverter control using the realtime outputs (RT0 to RT5) and 8/16-bit PPG timer.

- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the PPG timer pulse output. (Deadtime timer function)
- A non-overlapping waveform can be generated by using the 8-bit timer as a deadtime timer and adding a non-overlap time delay to the realtime outputs (RT1, RT3, RT5) . (Deadtime timer function)
- A GATE signal can be generated when a match occurs between the count from the 16-bit freerun timer and compare register in the output compare (OCCP0 to OCCP5) (rising edge on realtime output (RT)) to control the PPG timer operation. (GATE function)
- Can control the RTO0 to RTO5 pin outputs using the DTTI pin input.
  By making the DTTI pin input clockless, the pins can be controlled externally even when the oscillation clock is halted. (The level for each pin can be set by the program.) However, the I/O ports (P30 to P35) must have been set beforehand as outputs and the output values set in the port 3 data register (PDR3) .

6. UART

(1) Overview

- The UART is a general-purpose serial communications interface for performing synchronous or asynchronous (start-stop synchronization) communications with external devices.
- The interface provides both a bi-directional communication function (normal mode) and a master-slave communication function (multi-processor mode) .
- The UART can generate interrupt requests at receive complete, receive error detected, and transmit complete timings. Also the UART supports EI^{2}OS.

- **UART functions**

The UART is a general-purpose serial communications interface for sending serial data to and from other CPUs and peripheral devices.

	Function
Data buffer	Full-duplex double-buffered
Transmission modes	• Clock synchronous (no start and stop bits) • Clock asynchronous (start-stop synchronization)
Baud rate	• Max. 2 MHz (for a 16 MHz machine clock) • Baud rate generated by dedicated baud rate generator • Baud rate generated by external clock (clock input from SCK0 and SCK1 pins) • Baud rate generated by internal clock (clock supplied from 16-bit reload timer) • Eight different baud rate settings are available.
Number of data bits	• 7 bits (asynchronous normal mode only) • 8 bits
Signal format	Non return to zero (NRZ) format
Receive error detection	• Framing errors • Overrun errors • Parity errors (not available in multi-processor mode)
Interrupt requests	• Receive interrupt (Receive complete or receive error detected) • Transmit interrupt (Transmission complete) • Both transmit and receive support the extended intelligent I/O service (EI^{2}OS) .
Master/slave communication function (multi-processor mode)	Used for 1 (master) to n (slave) communications. (Can only be used as master)

Note : The UART does not add the start and stop bits in clock synchronous mode. In this case, only data is transmitted.

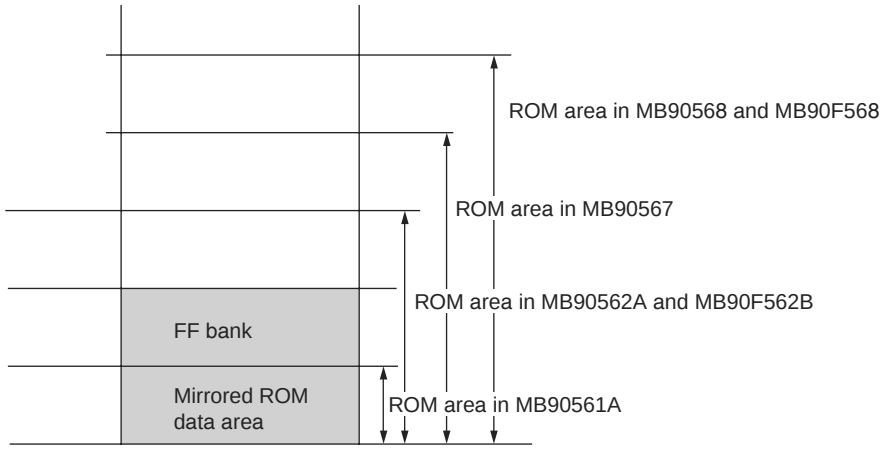
10. ROM Mirror Function Selection Module

- The ROM mirror function selection module enables ROM data in FF bank to be read by accessing 00 bank.

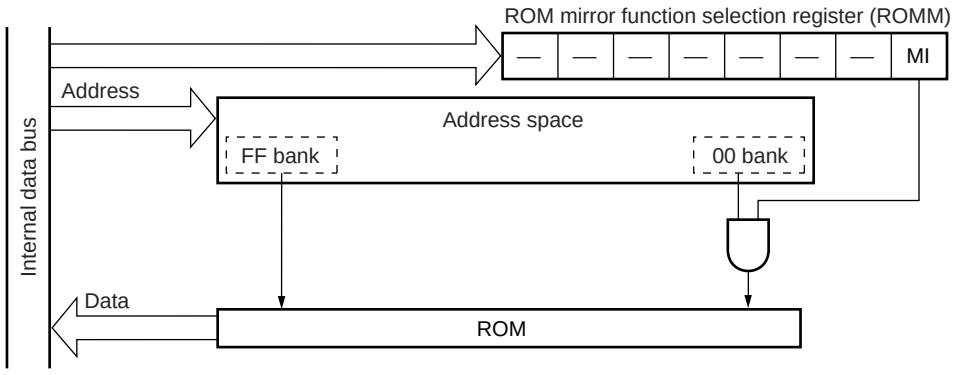
- **ROM mirror function selection module functions**

	Function
Mirror setting address	• Data in FFFFFF$_H$ to FF4000$_H$ in FF bank can be read from 00FFFF$_H$ to 004000$_H$ in 00 bank.
Interrupts	• None
EI^{2}OS support	• Not supported by the extended intelligent I/O service (EI^{2}OS) .

- **Relationship between addresses in the ROM mirror function**



- **Block diagram**



12. 512 Kbit Flash Memory

- This section describes the flash memory on the MB90F562B and does not apply to evaluation and mask ROM versions.
- The flash memory is located in bank FF in the CPU memory map.

- **Flash memory functions**

	Function
Memory size	• 512 Kbit (64 KBytes)
Memory configuration	• 64 KWords × 8 bits or 32 KWords × 16 bits
Sector configuration	• 16 KBytes + 8 KBytes + 8 KBytes + 32 KBytes
Sector protect function	• Selectable for each sector
Programming algorithm	• Automatic programming algorithm (Embedded Algorithm : Equivalent to MBM29F400TA)
Operation commands	• Compatible with JEDEC standard commands • Includes an erase pause and restart function • Write/erase completion detection by data polling or toggle bit • Erasing by sector available (sectors can be combined in any combination)
No. of write/erase cycles	• Min. 10,000 guaranteed
Memory write/erase method	• Can be written and erased using a parallel writer (Ando Denki AF9704, AF9705, AF9706, AF9708, and AF9709) • Can be written and erased using a dedicated serial writer (Yokogawa Digital Computer Corporation AF200, AF210, AF120, and AF110) • Can be written and erased by the program
Interrupts	• Write and erase completion interrupts
EI^{2}OS support	• Not supported by the extended intelligent I/O service (EI^{2}OS) .

- **Sector configuration of flash memory**

Flash memory	CPU address	Writer address*
SA1 (32 Kbyte)	FF0000H FF7FFFH	70000H 77FFFH
SA2 (8 Kbyte)	FF8000H FF9FFFH	78000H 79FFFH
SA3 (8 Kbyte)	FFA000H FFBFFFH	7A000H 7BFFFH
SA4 (16 Kbyte)	FFC000H FEFFFFH	7C000H 7FFFFH

* : The writer address is the address to be used instead of the CPU address when writing data from a parallel flash memory writer. Use the writer address when programming or erasing with a general-purpose parallel writer.

■ ELECTRICAL CHARACTERISTICS (MB90560 SERIES)

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 6.0	V	$V_{CC} \geq AV_{CC}$ *1
	AVR	V_{SS} – 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq AVR \geq 0$ V *1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 6.0	V	*2
"L" level maximum output current	I_{OL1}	—	15	mA	*3, *4
	I_{OL2}	—	20	mA	*3, *5
"L" level average output current	I_{OLAV1}	—	4	mA	Average value (operating current × operating ratio) *4
	I_{OLAV2}	—	12	mA	Average value (operating current × operating ratio) *5
"L" level total maximum output current	ΣI_{OL}	—	100	mA	
"L" level total average output current	ΣI_{OLAV}	—	50	mA	Average value (operating current × operating ratio)
"H" level maximum output current	I_{OH}	—	–15	mA	*3
"H" level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating ratio)
"H" level total maximum output current	ΣI_{OH}	—	–100	mA	
"H" level total average output current	ΣI_{OHAV}	—	–50	mA	Average value (operating current × operating ratio)
Power consumption	Pd	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : AV_{CC} and AVR must not exceed V_{CC}. Also, AVR must not exceed AV_{CC}.

*2 : V_I and V_O must not exceed V_{CC} + 0.3 V.

*3 : The maximum output current is the peak value for a single pin.

*4 : Pins other than P30/RTO0 to P35/RTO5

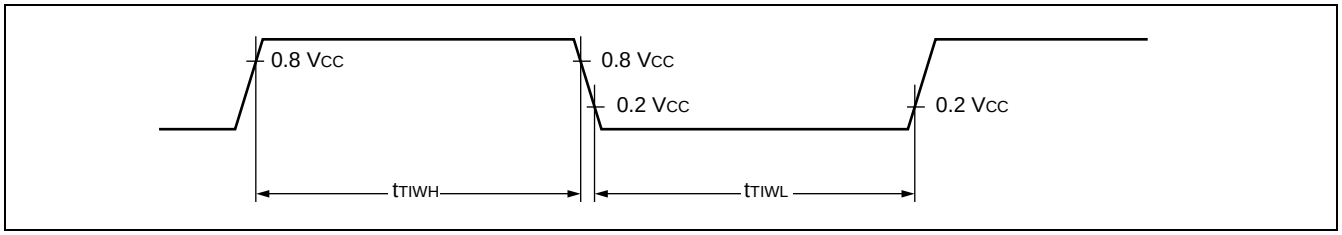
*5 : P30/RTO0 to P35/RTO5 pins

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

(5) Timer Input Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

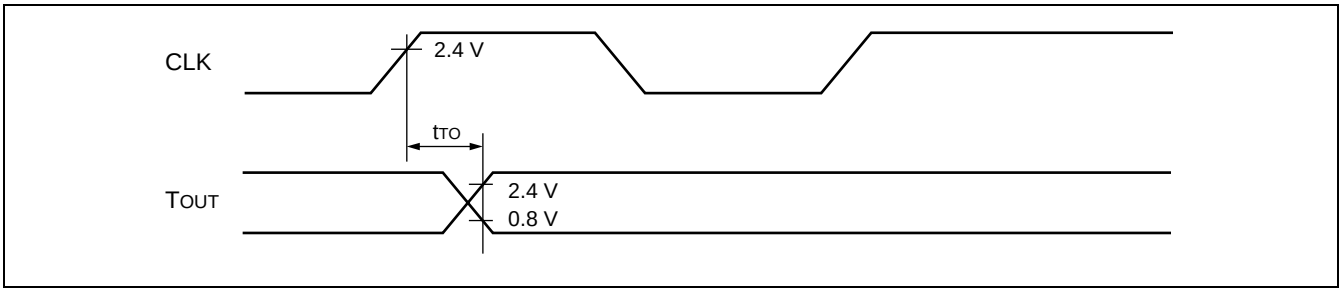
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TIWH}, t_{TIWL}	FRCK, IN0, IN1, TIN0, TIN1	—	4 t_{CP}	—	ns	



(6) Timer Output Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

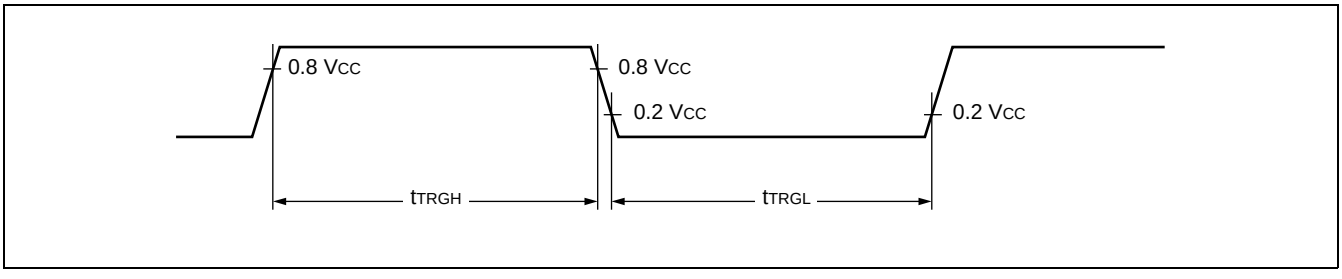
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
CLK ↑ → T_{OUT} change time	t_{TO}	RTO0 to RTO5, PPG0 to PPG5, TO0 to TO1	—	30	—	ns	



(7) Trigger Input Timings

(T_A = –40 °C to +85 °C, V_{CC} = 5.0 V ±10%, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Input pulse width	t_{TRGL}	INT0 to INT7, IN0 to IN3	—	5 t_{CP}	—	ns	In normal operation
				1	—	µs	In stop mode



■ ELECTRICAL CHARACTERISTICS (MB90565 SERIES)

1. Absolute Maximum Ratings

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Rating		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	
	AV_{CC}	V_{SS} – 0.3	V_{SS} + 4.0	V	$V_{CC} \geq AV_{CC}$ *1
	AVR	V_{SS} – 0.3	V_{SS} + 4.0	V	$AV_{CC} \geq AVR \geq 0$ V *1
Input voltage	V_I	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
Output voltage	V_O	V_{SS} – 0.3	V_{SS} + 4.0	V	*2
“L” level maximum output current	I_{OL}	—	15	mA	*3
“L” level average output current	I_{OLAV}	—	4	mA	Average value (operating current × operating ratio)
“L” level total maximum output current	ΣI_{OL}	—	100	mA	
“L” level total average output current	ΣI_{OLAV}	—	50	mA	Average value (operating current × operating ratio)
“H” level maximum output current	I_{OH}	—	–15	mA	*3
“H” level average output current	I_{OHAV}	—	–4	mA	Average value (operating current × operating ratio)
“H” level total maximum output current	ΣI_{OH}	—	–100	mA	
“H” level total average output current	ΣI_{OHAV}	—	–50	mA	Average value (operating current × operating ratio)
Power consumption	Pd	—	300	mW	
Operating temperature	T_A	–40	+85	°C	
Storage temperature	Tstg	–55	+150	°C	

*1 : AV_{CC} and AVR must not exceed V_{CC}. Also, AVR must not exceed AV_{CC}.

*2 : V_I and V_O must not exceed V_{CC} + 0.3 V.

*3 : The maximum output current is the peak value for a single pin.

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

(V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Value		Unit	Remarks
		Min.	Max.		
Power supply voltage	V_{CC}	3.0	3.6	V	Normal operation (MB90V560)
		2.7	3.6	V	Normal operation (MB90F568, MB90567 and MB90568)
		2.5	3.6	V	Maintaining state in stop mode
Input “H” voltage	V_{IH}	0.7 V_{CC}	V_{CC} + 0.3	V	CMOS input pin
	V_{IHS}	0.8 V_{CC}	V_{CC} + 0.3	V	CMOS hysteresis input pin
	V_{IHM}	V_{CC} – 0.3	V_{CC} + 0.3	V	MD input pin
Input “L” voltage	V_{IL}	V_{SS} – 0.3	0.3 V_{CC}	V	CMOS input pin
	V_{ILS}	V_{SS} – 0.3	0.2 V_{CC}	V	CMOS hysteresis input pin
	V_{ILM}	V_{SS} – 0.3	V_{SS} + 0.3	V	MD input pin
Operating temperature	T_A	–40	+85	°C	

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

3. DC Characteristics

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Output “H” voltage	V_{OH}	All output pins	V_{CC} = 3.0 V I_{OH} = –2.0 mA	V_{CC} – 0.5	V_{CC} – 0.3	—	V	
Output “L” voltage	V_{OL}	All output pins	V_{CC} = 3.0 V I_{OL} = 2.0 mA	—	0.2	0.4	V	
Input leak current	I_{IL}	All output pins	V_{CC} = 3.0 V V_{SS} < V_I < V_{CC}	–5	–1	5	µA	
Power supply current*	I_{CC}	V_{CC}	For V_{CC} = 3.3 V, internal frequency = 8 MHz, normal operation	—	14	22	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, normal operation	—	27	40	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 8 MHz, A/D operation in progress	—	18	27	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, A/D operation in progress	—	32	45	mA	MB90567/568
			For V_{CC} = 3.3 V, internal frequency = 8 MHz, normal operation	—	18	28	mA	MB90F568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, normal operation	—	36	45	mA	MB90F568
			For V_{CC} = 3.3 V, internal frequency = 8 MHz, A/D operation in progress	—	23	33	mA	MB90F568
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, A/D operation in progress	—	41	50	mA	MB90F568
			Flash write or erase	—	40	50	mA	MB90F568
	I_{CCS}		For V_{CC} = 3.3 V, internal frequency = 8 MHz, sleep mode	—	6	10	mA	MB90567/568 MB90F568*
			For V_{CC} = 3.3 V, internal frequency = 16 MHz, sleep mode	—	14	20	mA	MB90567/568 MB90F568*
	I_{CCH}		Stop mode, T_A = 25 °C	—	5	20	µA	

* : Value when low power mode bits (LPM0, 1) are set to “01” with an internal operating frequency of 8 MHz.

(Continued)

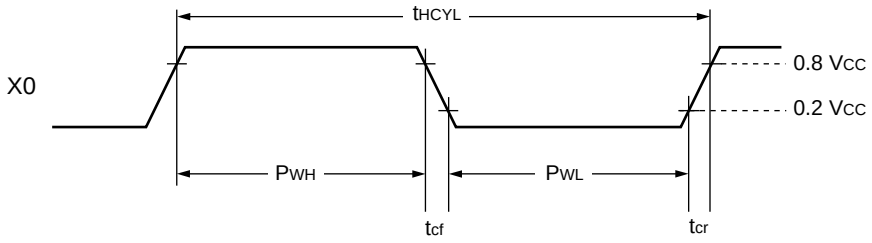
4. AC Characteristics

(1) Clock Timings

(MB90567/568/F568 : T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)
(MB90V560 : T_A = +25 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

Parameter	Symbol	Pin Name	Condition	Value			Unit	Remarks
				Min.	Typ.	Max.		
Clock frequency	f_C	X0, X1	—	3	—	12	MHz	MB90V560
				3	—	16	MHz	MB90567/568 MB90F568
Clock cycle time	t_{HCYL}	X0, X1		83.3	—	333	ns	MB90V560
				62.5	—	333	ns	MB90567/568 MB90F568
Input clock pulse width	P_{WH} P_{WL}	X0		10	—	—	ns	Recommended duty ratio = 30% to 70%
Input clock rise/fall time	tcr tcf	X0		—	—	5	ns	When using an external clock
Internal operating clock frequency	f_{CP}	—		1.5	—	12	MHz	MB90V560
				1.5	—	16	MHz	MB90567/568 MB90F568
Internal operating clock cycle time	t_{CP}	—		83.3	—	666	ns	MB90V560
				62.5	—	666	ns	MB90567/568 MB90F568

- **X0 and X1 clock timing**



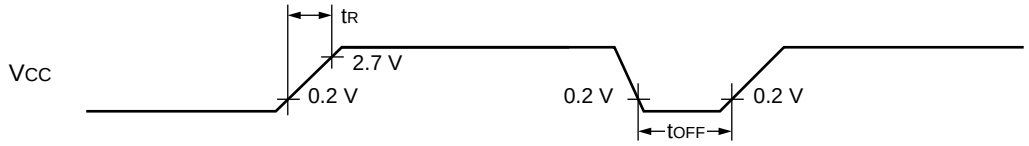
(3) Power-On Reset

(T_A = –40 °C to +85 °C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = AV_{SS} = 0.0 V)

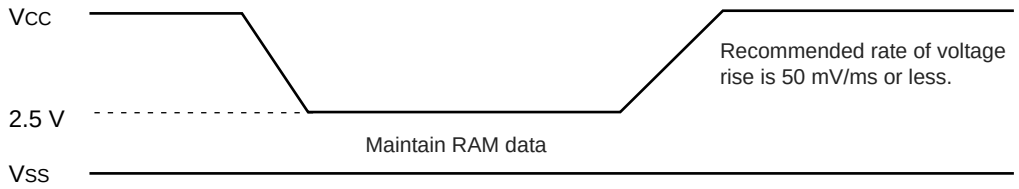
Parameter	Symbol	Pin Name	Condition	Value		Unit	Remarks
				Min.	Max.		
Power supply rise time	t_R	V_{CC}*	—	0.05	30	ms	
Power supply cutoff time	t_{OFF}	V_{CC}		4	—	ms	For repeated operation

* : V_{CC} must be less than 0.2 V before power-on.

Notes : • The above rating values are for generating a power-on reset.
• Some internal registers are only initialized by a power-on reset. Always apply the power supply in accordance with the above ratings if you wish to initialize these registers.



Sudden changes in the power supply voltage may cause a power-on reset.
The recommended practice if you wish to change the power supply voltage while the device is operating is to raise the voltage smoothly as shown below. Also, changes to the supply voltage should be performed when the PLL clock is not in use. The PLL clock may be used, however, if the rate of voltage change is 1 V/s or less.



■ ORDERING INFORMATION

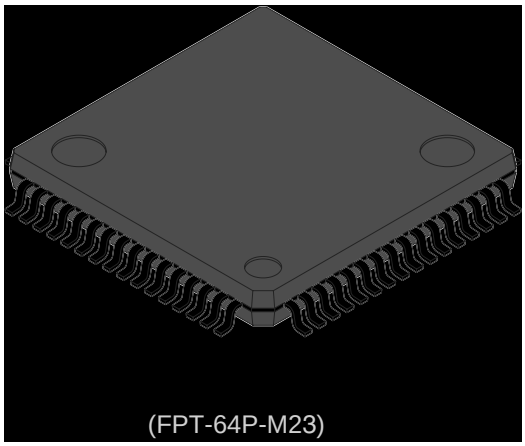
- **MB90560 series**

Part No.	Package	Remarks
MB90561AP MB90562AP MB90F562BP	64-pin plastic SH-DIP (DIP-64P-M01)	
MB90561APF MB90562APF MB90F562BPF	64-pin plastic QFP (FPT-64P-M06)	
MB90561APMC MB90562APMC MB90F562BPMC	64-pin plastic LQFP (FPT-64P-M23)	

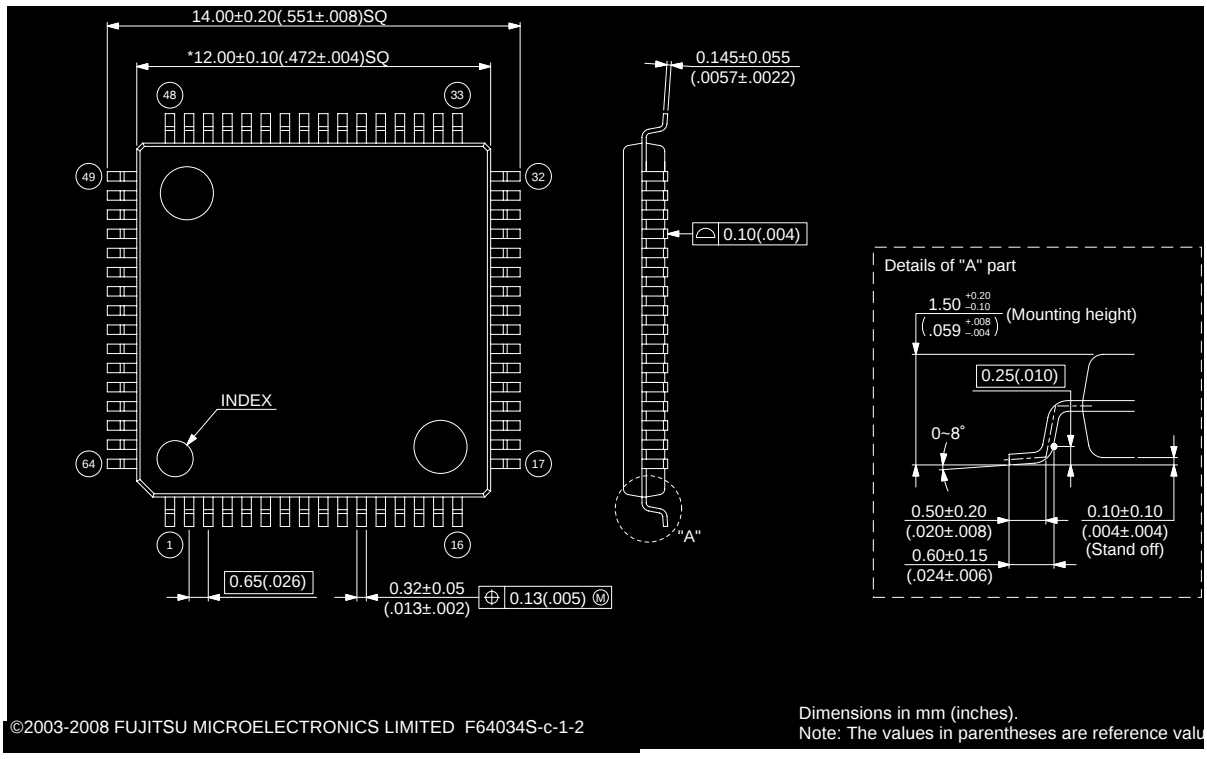
- **MB90565 series**

Part No.	Package	Remarks
MB90567PF MB90568PF MB90F568PF	64-pin plastic QFP (FPT-64P-M06)	
MB90567PMC MB90568PMC MB90F568PMC	64-pin plastic LQFP (FPT-64P-M23)	

(Continued)



(FPT-64P-M23)



Please confirm the latest Package dimension by following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
—	—	Deleted the description of old products MB90561, MB90562, and MB90F562.
—	—	The package code is changed. (FPT-64P-M09 → FPT-64P-M23)
34	■ PERIPHERAL FUNCTIONS 3. Watchdog Timer	The resource name of watch timer is collected. (clock timer → watch timer)
55	■ PERIPHERAL FUNCTIONS 13. 1 Mbit Flash Memory	Deleted "· Standard configuration for Fujitsu Microelectronics standard serial on-board programming".
66	■ ELECTRICAL CHARACTERISTICS (MB90560 SERIES) 5. Electrical Characteristics for the A/D Converter	Changed the items of "Zero transition voltage" and "Full-scale transition voltage".
79	■ ELECTRICAL CHARACTERISTICS (MB90565 SERIES) 5. Electrical Characteristics for the A/D Converter	Changed the items of "Zero transition voltage" and "Full-scale transition voltage".
85	■ ORDERING INFORMATION	Order informations are changed. (MB90561APFM → MB90561APMC MB90562APFM → MB90562APMC MB90F562BPFM → MB90F562BPMC MB90567PFM → MB90567PMC MB90568PFM → MB90568PMC MB90F568PFM → MB90F568PMC)
87	■ PACKAGE DIMENSIONS	The package figure is changed. (FPT-64P-M09 → FPT-64P-M23)

The vertical lines marked in the left side of the page show the changes.

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