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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	64MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-BQFP
Supplier Device Package	144-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f273-ceg-p-tr

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3 Functional description

The architecture of the ST10F273E combines advantages of both RISC and CISC processors and an advanced peripheral subsystem. The block diagram gives an overview of the different on-chip components and the high bandwidth internal bus structure of the ST10F273E.

Figure 3. Block diagram

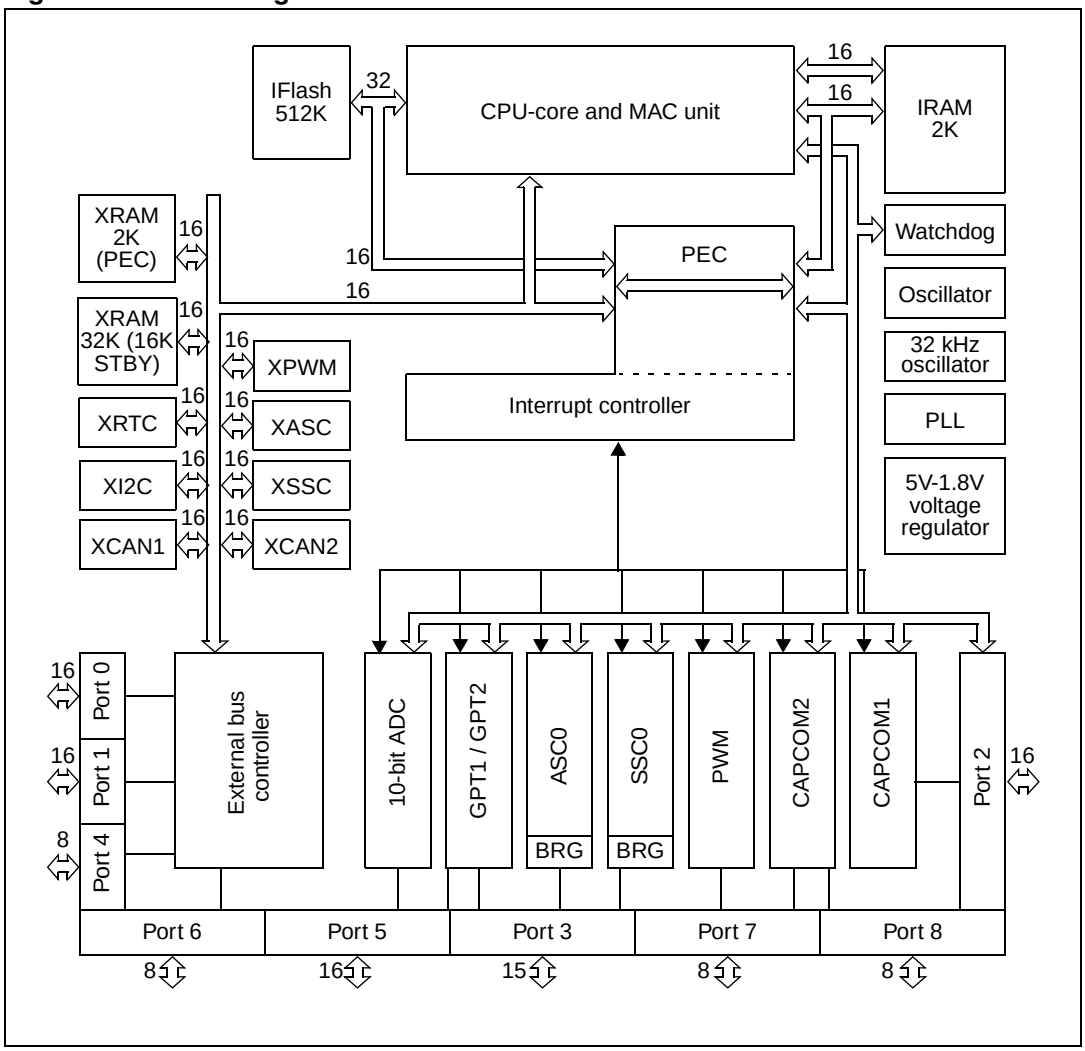


Table 8. Flash control register 0 high (continued)

Bit	Function
SUSP	Suspend This bit must be set to suspend the current Program (Word or Double Word) or Sector Erase operation in order to read data in one of the sectors of the bank under modification or to program data in another bank. The Suspend operation resets the Flash bank to normal read mode (automatically resetting bits BSYx). When in Program Suspend, the Flash module accepts only the following operations: Read and Program Resume. When in Erase Suspend the module accepts only the following operations: Read, Erase Resume and Program (Word or Double Word; Program operations cannot be suspended during Erase Suspend). To resume a suspended operation, the WMS bit must be set again, together with the selection bit corresponding to the operation to resume (WPG, DWPG, SER).(1)
WMS	Write mode start This bit must be set to start every write operation in the Flash module. At the end of the write operation or during a Suspend, this bit is automatically reset. To resume a suspended operation, this bit must be set again. It is forbidden to set this bit if bit ERR of FER is high (the operation is not accepted). It is also forbidden to start a new write (program or erase) operation (by setting WMS high) when bit SUSP of FCR0 is high. Resetting this bit by software has no effect.

1. It is forbidden to start a new Write operation with bit SUSP already set.

5.4.3 Flash control register 1 low

The Flash Control Register 1 Low (FCR1L), together with Flash Control Register 1 High (FCR1H), is used to select the sectors to Erase or, during any write operation, to monitor the status of each sector and bank.

FCR1L (0x0E 0004) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved						B0F9	B0F8	B0F7	B0F6	B0F5	B0F4	B0F3	B0F2	B0F1	B0F0
						RS	RS	RS	RS	RS	RS	RS	RS	RS	RS

Table 9. Flash control register 1 low

Bit	Function
B0F(9:0)	Bank 0 IFlash sector 9:0 status These bits must be set during a Sector Erase operation to select the sectors to erase in Bank 0. Besides, during any erase operation, these bits are automatically set and give the status of the 10 sectors of Bank 0 (B0F9-B0F0). The meaning of B0Fy bit for Sector y of Bank 0 is given by the next *Table 11* Banks (BxS) and Sectors (BxFy) Status bits meaning. These bits are automatically reset at the end of a Write operation if no errors are detected.

5.4.7 Flash data register 1 low

FDR1L (0x0E 000C) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN15	DIN14	DIN13	DIN12	DIN11	DIN10	DIN9	DIN8	DIN7	DIN6	DIN5	DIN4	DIN3	DIN2	DIN1	DIN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 14. Flash data register 1 low

Bit	Function
DIN(15:0)	Data input 15:0 These bits must be written with the Data to program the Flash with the following operations: Word Program (32-bit), Double Word Program (64-bit) and Set Protection.

5.4.8 Flash data register 1 high

FDR1H (0x0E 000E) FCR Reset value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
DIN31	DIN30	DIN29	DIN28	DIN27	DIN26	DIN25	DIN24	DIN23	DIN22	DIN21	DIN20	DIN19	DIN18	DIN17	DIN16
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 15. Flash data register 1 high

Bit	Function
DIN(31:16)	Data input 31:16 These bits must be written with the Data to program the Flash with the following operations: Word Program (32-bit), Double Word Program (64-bit) and Set Protection.

5.4.9 Flash address register low

FARL (0x0E 0010) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADD15	ADD14	ADD13	ADD12	ADD11	ADD10	ADD9	ADD8	ADD7	ADD6	ADD5	ADD4	ADD3	ADD2	reserved	
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW		

Table 16. Flash address register low

Bit	Function
ADD(15:2)	Address 15:2 These bits must be written with the Address of the Flash location to program in the following operations: Word Program (32-bit) and Double Word Program (64-bit). In Double Word Program bit ADD2 must be written to ‘0’.

5.5.5 Flash non volatile access protection register 1 low

FNVAPR1L (0x0E DFBC) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PDS15	PDS14	PDS13	PDS12	PDS11	PDS10	PDS9	PDS8	PDS7	PDS6	PDS5	PDS4	PDS3	PDS2	PDS1	PDS0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 22. Flash non volatile access protection register 1 low

Bit	Function
PDS(15:0)	Protections disable 15-0 If bit PDSx is programmed at 0 and bit PENx is erased at 1, the action of bit ACCP is disabled. Bit PDS0 can be programmed at 0 only if both bits DBGP and ACCP have already been programmed at 0. Bit PDSx can be programmed at 0 only if bit PENx-1 has already been programmed at 0.

5.5.6 Flash non volatile access protection register 1 high

FNVAPR1H (0x0E DFBE) NVR Delivery value: FFFFh

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PEN15	PEN14	PEN13	PEN12	PEN11	PEN10	PEN9	PEN8	PEN7	PEN6	PEN5	PEN4	PEN3	PEN2	PEN1	PEN0
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

Table 23. Flash non volatile access protection register 1 high

Bit	Function
PEN15-0	Protections enable 15-0 If bit PENx is programmed at 0 and bit PDSx+1 is erased at 1, the action of bit ACCP is enabled again. Bit PENx can be programmed at 0 only if bit PDSx has already been programmed at 0.

5.5.7 Access protection

The I-Flash module has one level of access protection (access to data both in Reading and Writing): if bit ACCP of FNVAPR0 is programmed at 0, the I-Flash module becomes access protected: data in the I-Flash module can be read only if the current execution is from the I-Flash module itself.

Protection can be permanently disabled by programming bit PDS0 of FNVAPR1H, in order to analyze rejects. Protection can be permanently enabled again by programming bit PEN0 of FNVAPR1L. The action to disable and enable again Access Protections in a permanent way can be executed a maximum of 16 times.

Trying to write into the access protected Flash from internal RAM or external memories will be unsuccessful. Trying to read into the access protected Flash from internal RAM or external memories will output a dummy data (software trap 0x009Bh).

When the Flash module is protected in access, also the data access through PEC of a peripheral is forbidden. To read/write data in PEC mode from/to a protected bank, first it is necessary to temporarily unprotect the Flash module.

In the following table a summary of all levels of possible Access protection is reported: in particular, supposing to enable all possible access protections, when fetching from a

7.2 Instruction set summary

The *Table 27* lists the instructions of the ST10F273E. The detailed description of each instruction can be found in the “ST10 Family Programming Manual”.

Table 27. Standard instruction set summary

Mnemonic	Description	Bytes
ADD(B)	Add word (byte) operands	2 / 4
ADDC(B)	Add word (byte) operands with Carry	2 / 4
SUB(B)	Subtract word (byte) operands	2 / 4
SUBC(B)	Subtract word (byte) operands with Carry	2 / 4
MUL(U)	(Un)Signed multiply direct GPR by direct GPR (16-16-bit)	2
DIV(U)	(Un)Signed divide register MDL by direct GPR (16-/16-bit)	2
DIVL(U)	(Un)Signed long divide reg. MD by direct GPR (32-/16-bit)	2
CPL(B)	Complement direct word (byte) GPR	2
NEG(B)	Negate direct word (byte) GPR	2
AND(B)	Bit-wise AND, (word/byte operands)	2 / 4
OR(B)	Bit-wise OR, (word/byte operands)	2 / 4
XOR(B)	Bit-wise XOR, (word/byte operands)	2 / 4
BCLR	Clear direct bit	2
BSET	Set direct bit	2
BMOV(N)	Move (negated) direct bit to direct bit	4
BAND, BOR, BXOR	AND/OR/XOR direct bit with direct bit	4
BCMP	Compare direct bit to direct bit	4
BFLDH/L	Bit-wise modify masked high/low byte of bit-addressable direct word memory with immediate data	4
CMP(B)	Compare word (byte) operands	2 / 4
CMPD1/2	Compare word data to GPR and decrement GPR by 1/2	2 / 4
CMPI1/2	Compare word data to GPR and increment GPR by 1/2	2 / 4
PRIOR	Determine number of shift cycles to normalize direct word GPR and store result in direct word GPR	2
SHL / SHR	Shift left/right direct word GPR	2
ROL / ROR	Rotate left/right direct word GPR	2
ASHR	Arithmetic (sign bit) shift right direct word GPR	2
MOV(B)	Move word (byte) data	2 / 4
MOVBS	Move byte operand to word operand with sign extension	2 / 4
MOVBZ	Move byte operand to word operand with zero extension	2 / 4
JMPA, JMPI, JMPR	Jump absolute/indirect/relative if condition is met	4
JMPS	Jump absolute to a code segment	4

Table 29. Interrupt sources (continued)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h
CAPCOM register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 timer 5	T5IR	T5IE	T5INT	00'0094h	25h

20.2 Asynchronous reset

An asynchronous reset is triggered when $\overline{\text{RSTIN}}$ pin is pulled low while RPD pin is at low level. Then the ST10F273E is immediately (after the input filter delay) forced in reset default state. It pulls low $\overline{\text{RSTOUT}}$ pin, it cancels pending internal hold states if any, it aborts all internal/external bus cycles, it switches buses (data, address and control signals) and I/O pin drivers to high-impedance, it pulls high Port0 pins.

Note: If an asynchronous reset occurs during a read or write phase in internal memories, the content of the memory itself could be corrupted: to avoid this, synchronous reset usage is strongly recommended.

Power-on reset

The asynchronous reset must be used during the power-on of the device. Depending on crystal or resonator frequency, the on-chip oscillator needs about 1ms to 10ms to stabilize (Refer to Electrical Characteristics Section), with an already stable V_{DD}. The logic of the ST10F273E does not need a stabilized clock signal to detect an asynchronous reset, so it is suitable for power-on conditions. To ensure a proper reset sequence, the $\overline{\text{RSTIN}}$ pin and the RPD pin must be held at low level until the device clock signal is stabilized and the system configuration value on Port0 is settled.

At Power-on it is important to respect some additional constraints introduced by the start-up phase of the different embedded modules.

In particular the on-chip voltage regulator needs at least 1ms to stabilize the internal 1.8V for the core logic: this time is computed from when the external reference (V_{DD}) becomes stable (inside specification range, that is at least 4.5V). This is a constraint for the application hardware (external voltage regulator): the $\overline{\text{RSTIN}}$ pin assertion shall be extended to guarantee the voltage regulator stabilization.

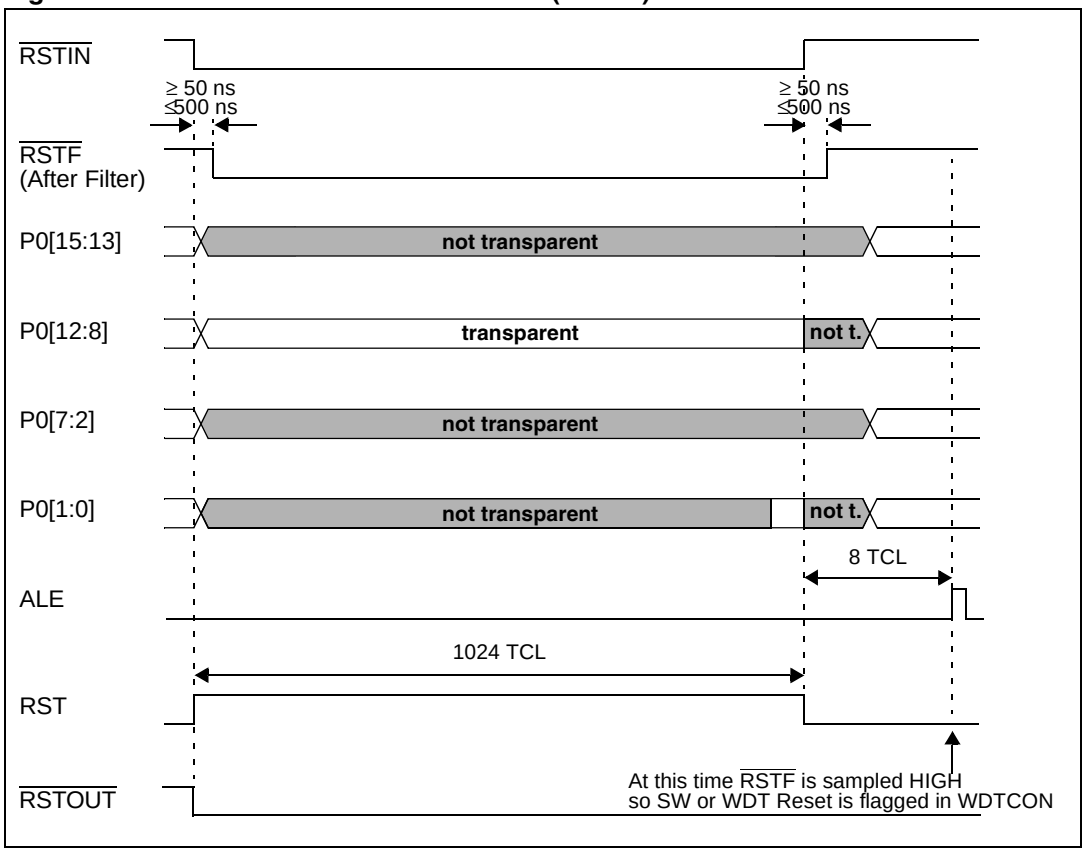
A second constraint is imposed by the embedded FLASH. When booting from internal memory, starting from $\overline{\text{RSTIN}}$ releasing, it needs a maximum of 1ms for its initialization: before that, the internal reset (RST signal) is not released, so the CPU does not start code execution in internal memory.

Note: This is not true if external memory is used (pin $\overline{EA}$ held low during reset phase). In this case, once $\overline{RSTIN}$ pin is released, and after few CPU clock (Filter delay plus 3...8 TCL), the internal reset signal RST is released as well, so the code execution can start immediately after. Obviously, an eventual access to the data in internal Flash is forbidden before its initialization phase is completed: an eventual access during starting phase will return FFFFh (just at the beginning), while later 009Bh (an illegal opcode trap can be generated).

At Power-on, the $\overline{\text{RSTIN}}$ pin shall be tied low for a minimum time that includes also the start-up time of the main oscillator (t_{STUP} = 1ms for resonator, 10ms for crystal) and PLL synchronization time (t_{PSUP} = 200µs): this means that if the internal FLASH is used, the $\overline{\text{RSTIN}}$ pin could be released before the main oscillator and PLL are stable to recover some time in the start-up phase (FLASH initialization only needs stable V_{18}, but does not need stable system clock since an internal dedicated oscillator is used).

Warning: It is recommended to provide the external hardware with a current limitation circuitry. This is necessary to avoid permanent damages of the device during the power-on transient, when the capacitance on V_{18} pin is charged. For the on-chip voltage regulator functionality 10nF are

Figure 26. SW / WDT bidirectional RESET ($\overline{EA}$ = 0)



21.3.4 Power reduction modes summary

In the following *Table 52: Power reduction modes summary*, a summary of the different Power reduction modes is reported.

Table 52. Power reduction modes summary

Mode	V_{DD}	V_{STBY}	CPU	Peripherals	RTC	Main OSC	32 kHz OSC	STBY XRAM	XRAM
Idle	on	on	off	on	off	run	off	biased	biased
	on	on	off	on	on	run	on	biased	biased
Power down	on	on	off	off	off	off	off	biased	biased
	on	on	off	off	on	on	off	biased	biased
	on	on	off	off	on	off	on	biased	biased
Stand-by	off	on	off	off	off	off	off	biased	off
	off	on	off	off	on	off	on	biased	off

Table 53. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
T1	FE52h	29h	CAPCOM timer 1 register	0000h
T1IC **b**	FF9Eh	CFh	CAPCOM timer 1 interrupt control register	- - 00h
T1REL	FE56h	2Bh	CAPCOM timer 1 reload register	0000h
T2	FE40h	20h	GPT1 timer 2 register	0000h
T2CON **b**	FF40h	A0h	GPT1 timer 2 control register	0000h
T2IC **b**	FF60h	B0h	GPT1 timer 2 interrupt control register	- - 00h
T3	FE42h	21h	GPT1 timer 3 register	0000h
T3CON **b**	FF42h	A1h	GPT1 timer 3 control register	0000h
T3IC **b**	FF62h	B1h	GPT1 timer 3 interrupt control register	- - 00h
T4	FE44h	22h	GPT1 timer 4 register	0000h
T4CON **b**	FF44h	A2h	GPT1 timer 4 control register	0000h
T4IC **b**	FF64h	B2h	GPT1 timer 4 interrupt control register	- - 00h
T5	FE46h	23h	GPT2 timer 5 register	0000h
T5CON **b**	FF46h	A3h	GPT2 timer 5 control register	0000h
T5IC **b**	FF66h	B3h	GPT2 timer 5 interrupt control register	- - 00h
T6	FE48h	24h	GPT2 timer 6 register	0000h
T6CON **b**	FF48h	A4h	GPT2 timer 6 control register	0000h
T6IC **b**	FF68h	B4h	GPT2 timer 6 interrupt control register	- - 00h
T7	F050h **E**	28h	CAPCOM timer 7 register	0000h
T78CON **b**	FF20h	90h	CAPCOM timer 7 and 8 control register	0000h
T7IC **b**	F17Ah **E**	BDh	CAPCOM timer 7 interrupt control register	- - 00h
T7REL	F054h **E**	2Ah	CAPCOM timer 7 reload register	0000h
T8	F052h **E**	29h	CAPCOM timer 8 register	0000h
T8IC **b**	F17Ch **E**	BEh	CAPCOM timer 8 interrupt control register	- - 00h
T8REL	F056h **E**	2Bh	CAPCOM timer 8 reload register	0000h
TFR **b**	FFACh	D6h	Trap Flag register	0000h
WDT	FEAEh	57h	Watchdog timer register (read only)	0000h
WDTCON **b**	FFAEh	D7h	Watchdog timer control register	00xxh [2]
XADRS3	F01Ch **E**	0Eh	XPER address select register 3	800Bh
XP0IC **b**	F186h **E**	C3h	See *Section 9.1*	- - 00h [3]
XP1IC **b**	F18Eh **E**	C7h	See *Section 9.1*	- - 00h [3]
XP2IC **b**	F196h **E**	CBh	See *Section 9.1*	- - 00h [3]
XP3IC **b**	F19Eh **E**	CFh	See *Section 9.1*	- - 00h [3]

Table 54. List of XBus registers (continued)

Name	Physical address	Description	Reset value
RTCDL	ED0Ah	RTC divider counter low byte	XXXXh
RTCH	ED10h	RTC programmable counter high byte	XXXXh
RTCL	ED0Eh	RTC programmable counter low byte	XXXXh
RTCPH	ED08h	RTC prescaler register high byte	XXXXh
RTCPL	ED06h	RTC prescaler register low byte	XXXXh
XCLKOUTDIV	EB02h	CLKOUT divider control register	- - 00h
XEMU0	EB76h	XBUS emulation register 0 (write only)	XXXXh
XEMU1	EB78h	XBUS emulation register 1 (write only)	XXXXh
XEMU2	EB7Ah	XBUS emulation register 2 (write only)	XXXXh
XEMU3	EB7Ch	XBUS emulation register 3 (write only)	XXXXh
XIR0CLR	EB14h	X-Interrupt 0 clear register (write only)	0000h
XIR0SEL	EB10h	X-Interrupt 0 selection register	0000h
XIR0SET	EB12h	X-Interrupt 0 set register (write only)	0000h
XIR1CLR	EB24h	X-Interrupt 1 clear register (write only)	0000h
XIR1SEL	EB20h	X-Interrupt 1 selection register	0000h
XIR1SET	EB22h	X-Interrupt 1 set register (write only)	0000h
XIR2CLR	EB34h	X-Interrupt 2 clear register (write only)	0000h
XIR2SEL	EB30h	X-Interrupt 2 selection register	0000h
XIR2SET	EB32h	X-Interrupt 2 set register (write only)	0000h
XIR3CLR	EB44h	X-Interrupt 3 clear selection register (write only)	0000h
XIR3SEL	EB40h	X-Interrupt 3 selection register	0000h
XIR3SET	EB42h	X-Interrupt 3 set selection register (write only)	0000h
XMISC	EB46h	XBUS miscellaneous features register	0000h
XP1DIDIS	EB36h	Port 1 digital disable register	0000h
XPEREMU	EB7Eh	XPERCON copy for emulation (write only)	XXXXh
XPICON	EB26h	Extended port input threshold control register	- - 00h
XPOLAR	EC04h	XPWM module channel polarity register	0000h
XPP0	EC20h	XPWM module period register 0	0000h
XPP1	EC22h	XPWM module period register 1	0000h
XPP2	EC24h	XPWM module period register 2	0000h
XPP3	EC26h	XPWM module period register 3	0000h
XPT0	EC10h	XPWM module up/down counter 0	0000h
XPT1	EC12h	XPWM module up/down counter 1	0000h
XPT2	EC14h	XPWM module up/down counter 2	0000h

23.3 Flash registers ordered by name

The following table lists all Flash Control Registers which are implemented in the ST10F273E ordered by their name. These registers are physically mapped on the IBus, except for XFVTAUR0, which is mapped on XBus. Note that these registers are not bit-addressable.

Table 55. List of flash registers

Name	Physical address	Description	Reset value
FARH	0x000E 0012	Flash address register - high	0000h
FARL	0x000E 0010	Flash address register - low	0000h
FCR0H	0x000E 0002	Flash control register 0 - high	0000h
FCR0L	0x000E 0000	Flash control register 0 - low	0000h
FCR1H	0x000E 0006	Flash control register 1 - high	0000h
FCR1L	0x000E 0004	Flash control register 1 - low	0000h
FDR0H	0x000E 000A	Flash data register 0 - high	FFFFh
FDR0L	0x000E 0008	Flash data register 0 - low	FFFFh
FDR1H	0x000E 000E	Flash data register 1 - high	FFFFh
FDR1L	0x000E 000C	Flash data register 1 - low	FFFFh
FER	0x000E 0014	Flash error register	0000h
FNVAPR0	0x000E DFB8	Flash non volatile access protection reg.0	ACFFh
FNVAPR1H	0x000E DFBE	Flash non volatile access protection reg.1 - high	FFFFh
FNVAPR1L	0x000E DFBC	Flash non volatile access protection reg.1 - low	FFFFh
FNVWPIRH	0x000E DFB6	Flash non volatile protection i register high	FFFFh
FNVWPIRL	0x000E DFB4	Flash non volatile protection i register low	FFFFh

23.4 Identification registers

The ST10F273E have four Identification registers, mapped in ESFR space. These registers contain:

- A manufacturer identifier
- A chip identifier with its revision
- A internal Flash and size identifier
- Programming voltage description

Note: The ST10F273E device is a commercial version based on the ST10F276E silicon, the identification registers provide the values corresponding to the ST10F276E device.

IDPROG (F078h / 3Ch) ESFR Reset Value: 0040h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PROGVPP								PROGVDD							
R								R							

Table 59. IDPROG

Bit	Function
PROGVDD	Programming V_{DD} voltage V_{DD} voltage when programming EPROM or FLASH devices is calculated using the following formula: V_{DD} = 20 x [PROGVDD] / 256 (volts) - 40h for ST10F273E (5V).
PROGVPP	Programming V_{PP} voltage (no need of external V_{PP}) - 00h

Note: All identification words are read only registers.

The values written inside different Identification Register bits are valid only after the Flash initialization phase is completed. When code execution is started from internal memory (pin $\overline{EA}$ held high during reset), the Flash has certainly completed its initialization, so the bits of Identification Registers are immediately ready to be read out. On the contrary, when code execution is started from external memory (pin $\overline{EA}$ held low during reset), the Flash initialization is not yet completed, so the bits of Identification Registers are not ready. The user can poll bits 15 and 14 of IDMEM register: when both bits are read low, the Flash initialization is complete, so all Identification Register bits are correct.

Before Flash initialization completion, the default setting of the different Identification Registers are the following:

- IDMANUF 0403h
- IDCHIP 114xh (x = silicon revision)
- IDMEM F0D0h
- IDPROG 0040h

Table 64. DC characteristics (continued)

Symbol	Parameter	Test Condition	Limit Values		Unit
			Min.	Max.	
V_{OH1} **CC**	Output high voltage (1) (P0[15:0], P1[15:0], P2[15:0], P3[15,13:0], P4[7:0], P7[7:0], P8[7:0])	I_{OH1} = – 4 mA I_{OH1} = – 0.5 mA	V_{DD} – 0.8 V_{DD} – 0.08	–	V
V_{OH2} **CC**	Output high voltage RPD	I_{OH2} = – 2 mA I_{OH2} = – 750 µA I_{OH2} = – 150 µA	0 0.3 V_{DD} 0.5 V_{DD}	–	V
$\lvert I_{OZ1} \rvert$ **CC**	Input leakage current (P5[15:0]) (2)	–	–	±0.2	µA
$\lvert I_{OZ2} \rvert$ **CC**	Input leakage current (all except P5[15:0], P2[0], RPD, P3[12], P3[15])	–	–	±0.5	µA
$\lvert I_{OZ3} \rvert$ **CC**	Input leakage current (P2[0]) (3)	–	–	+1.0 –0.5	µA
$\lvert I_{OZ4} \rvert$ **CC**	Input leakage current (RPD)	–	–	±3.0	µA
$\lvert I_{OZ5} \rvert$ **CC**	Input leakage current (P3[12], P3[15])	–	–	±1.0	µA
$\lvert I_{OV1} \rvert$ **SR**	Overload current (all except P2[0])	3) 4)	–	±5	mA
$\lvert I_{OV2} \rvert$ **SR**	Overload current (P2[0]) (3)	3) 4)	–	+5 –1	mA
R_{RST} **CC**	$\overline{\text{RSTIN}}$ pull-up resistor	100 kΩ nominal	50	250	kΩ
I_{RWH}	Read/Write inactive current (4) (5)	V_{OUT} = 2.4 V	–	–40	µA
I_{RWL}	Read/Write active current (4) 7)	V_{OUT} = 0.4V	–500	–	µA
I_{ALEL}	ALE inactive current (4) (5)	V_{OUT} = 0.4V	20	–	µA
I_{ALEH}	ALE active current (4) 7)	V_{OUT} = 2.4 V	–	300	µA
I_{P6H}	Port 6 inactive current (P6[4:0])(4) (5)	V_{OUT} = 2.4 V	–	–40	µA
I_{P6L}	Port 6 active current (P6[4:0]) (4) (6)	V_{OUT} = 0.4V	–500	–	µA
I_{P0H} 6)	PORT0 configuration current (4)	V_{IN} = 2.0V	–	–10	µA
I_{P0L} 7)		V_{IN} = 0.8V	–100	–	µA
C_{IO} **CC**	Pin capacitance (Digital inputs / outputs)	(3) (5)	–	10	pF
I_{CC1}	Run mode power supply current (7) (execution from internal RAM)	–	–	20 + 2 f_{CPU}	mA
I_{CC2}	Run mode power supply current (8)(9) (execution from internal Flash)	–	–	20 + 1.8 f_{CPU}	mA
I_{ID}	Idle mode supply current (10)	–	–	20 + 0.6 f_{CPU}	mA
I_{PD1}	Power down supply current(11) *(RTC off, oscillators off, main voltage regulator off)*	T_A = 25°C	–	1	mA

above, it is simple to derive the following relation between the ideal and real sampled voltage on C_S:

$$\frac{V_A}{V_{A2}} = \frac{C_{P1} + C_{P2} + C_F}{C_{P1} + C_{P2} + C_F + C_S}$$

From this formula, in the worst case (when V_A is maximum, that is for instance 5V), assuming to accept a maximum error of half a count (~2.44mV), it is immediately evident a constraints on C_F value:

$$C_F > 2048 \cdot C_S$$

In the next section an example of how to design the external network is provided, assuming some reasonable values for the internal parameters and making hypothesis on the characteristics of the analog signal to be sampled.

24.7.4.1 Example of external network sizing

The following hypothesis are formulated in order to proceed in designing the external network on A/D Converter input pins:

- Analog Signal Source Bandwidth (f_0): 10 kHz
- Conversion Rate (f_C): 25 kHz
- Sampling Time (T_S): 1µs
- Pin Input Capacitance (C_{P1}): 5pF
- Pin Input Routing Capacitance (C_{P2}): 1pF
- Sampling Capacitance (C_S): 4pF
- Maximum Input Current Injection (I_{INJ}): 3mA
- Maximum Analog Source Voltage ($V_{AM)}$:12V
- Analog Source Impedance (R_S): 100Ω
- Channel Switch Resistance (R_{SW}): 500Ω
- Sampling Switch Resistance (R_{AD}): 200Ω

Warning: Direct driving on XTAL3 pin is not supported. Always use a 32 kHz crystal oscillator.

24.8.13 External clock drive XTAL1

When Direct Drive configuration is selected during reset, it is possible to drive the CPU clock directly from the XTAL1 pin, without particular restrictions on the maximum frequency, since the on-chip oscillator amplifier is bypassed. The speed limit is imposed by internal logic that targets a maximum CPU frequency of 64 MHz.

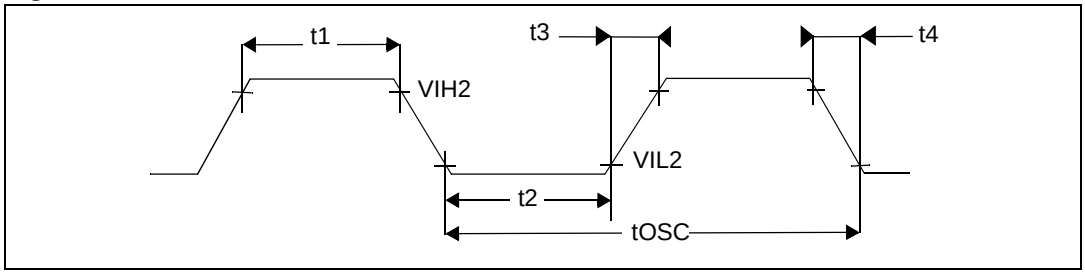
In all other clock configurations (Direct Drive with Prescaler or PLL usage) the on-chip oscillator amplifier is not bypassed, so it determines the input clock speed limit. Then, when the on-chip oscillator is enabled it is forbidden to use any external clock source different from crystal or ceramic resonator.

Table 76. External clock drive XTAL1 timing

Parameter	Symbol		Direct drive $f_{CPU} = f_{XTAL}$		Direct drive with prescaler $f_{CPU} = f_{XTAL} / 2$		PLL usage $f_{CPU} = f_{XTAL} \times F$		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
XTAL1 period [1, 2]	t_{OSC}	SR	15.625	–	83.3	250	83.3	250	ns
High time [3]	t_1	SR	6	–	3	–	6	–	
Low time [3]	t_2	SR	6	–	3	–	6	–	
Rise time [3]	t_3	SR	–	2	–	2	–	2	
Fall time [3]	t_4	SR	–	2	–	2	–	2	

1. The minimum value for the XTAL1 signal period shall be considered as the theoretical minimum. The real minimum value depends on the duty cycle of the input clock signal.
2. 4 to 8 MHz is the input frequency range when using an external clock source. 64 MHz can be applied with an external clock source only when Direct Drive mode is selected: in this case, the oscillator amplifier is bypassed so it does not limit the input frequency.
3. The input clock signal must reach the defined levels V_{IL2} and V_{IH2}.

Figure 47. External clock drive XTAL1



Note: When Direct Drive is selected, an external clock source can be used to drive XTAL1. The maximum frequency of the external clock source depends on the duty cycle: when 64 MHz is used, 50% duty cycle shall be granted (low phase = high phase = 7.8ns); when for instance 32 MHz is used, a 25% duty cycle can be accepted (minimum phase, high or low, again equal to 7.8ns).

Figure 51. External memory cycle: Multiplexed bus, with/without r/w delay, extended ALE, r/w CS

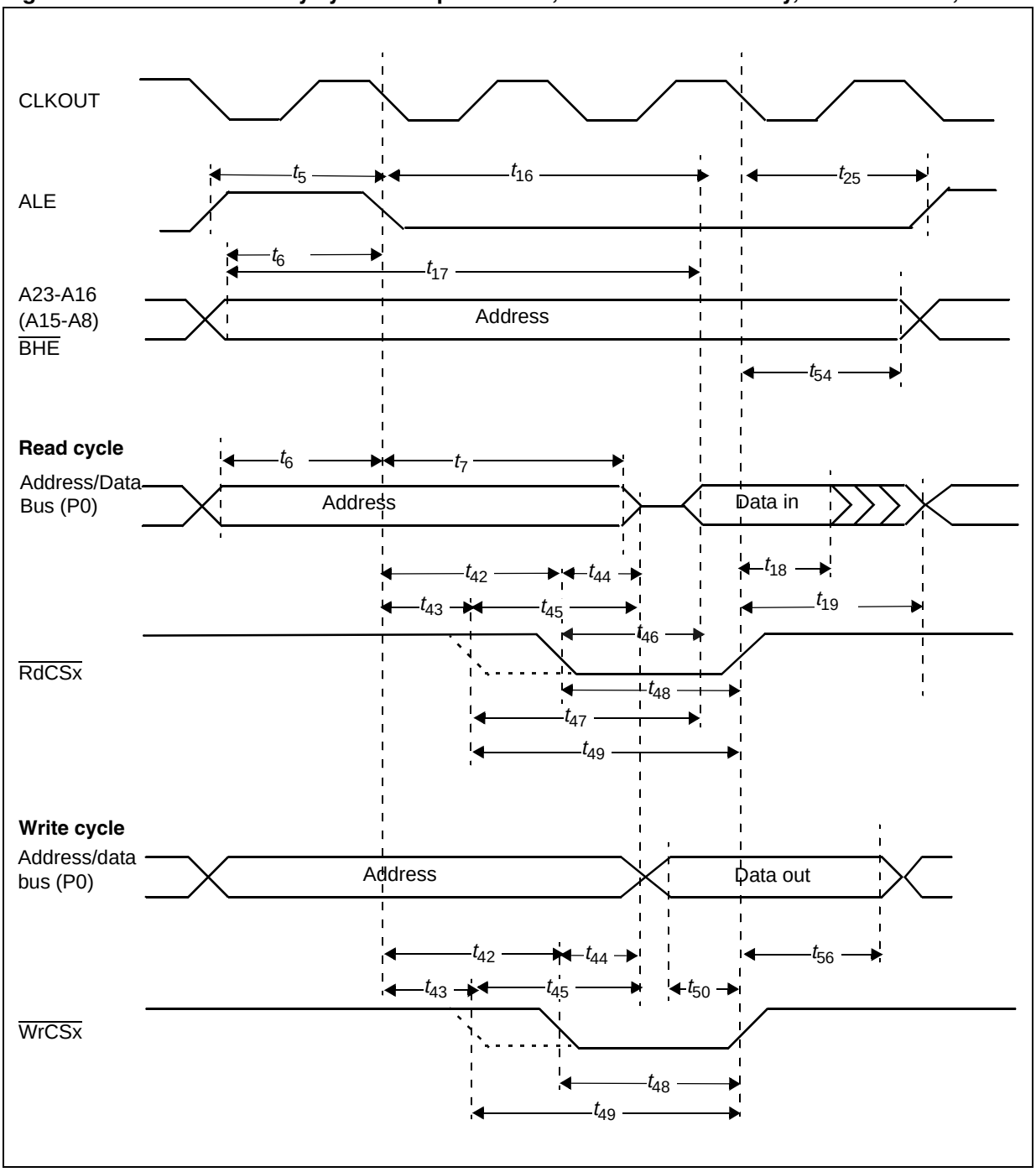


Figure 54. External memory cycle: Demultipl. bus, with/without r/w delay, normal ALE, r/w CS