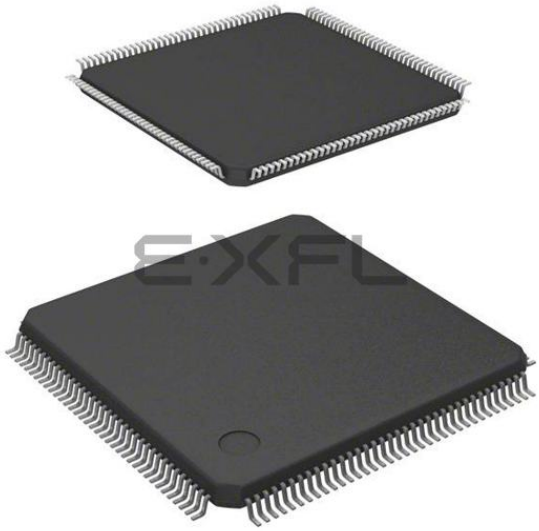

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	48MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f273-ceg-t-tr

Table 1. Pin description (continued)

Symbol	Pin	Type	Function
$\overline{EA}$ / V_{STBY}	99	I	External access enable pin. A low level applied to this pin during and after Reset forces the ST10F273E to start the program from the external memory space. A high level forces ST10F273E to start in the internal memory space. This pin is also used (when Stand-by mode is entered, that is ST10F273E under reset and main V_{DD} turned off) to bias the 32 kHz oscillator amplifier circuit and to provide a reference voltage for the low-power embedded voltage regulator which generates the internal 1.8V supply for the RTC module (when not disabled) and to retain data inside the Stand-by portion of the XRAM (16Kbyte). It can range from 4.5 to 5.5V (6V for a reduced amount of time during the device life, 4.0V when RTC and 32 kHz on-chip oscillator amplifier are turned off). In running mode, this pin can be tied low during reset without affecting 32 kHz oscillator, RTC and XRAM activities, since the presence of a stable V_{DD} guarantees the proper biasing of all those modules.
P0L.0 -P0L.7, P0H.0 P0H.1 - P0H.7	100-107, 108, 111-117	I/O	Two 8-bit bidirectional I/O ports P0L and P0H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. The input threshold of Port 0 is selectable (TTL or CMOS). In case of an external bus configuration, PORT0 serves as the address (A) and as the address / data (AD) bus in multiplexed bus modes and as the data (D) bus in demultiplexed bus modes. Demultiplexed bus modes Data path width 8-bit 16-bi P0L.0 – P0L.7: D0 – D7 D0 - D7 P0H.0 – P0H.7: I/O D8 - D15 Multiplexed bus modes Data path width 8-bit 16-bi P0L.0 – P0L.7: AD0 – AD7 AD0 - AD7 P0H.0 – P0H.7: A8 – A15 AD8 - AD15
P1L.0 - P1L.7 P1H.0 - P1H.7	118-125 128-135	I/O	Two 8-bit bidirectional I/O ports P1L and P1H, bit-wise programmable for input or output via direction bit. Programming an I/O pin as input forces the corresponding output driver to high impedance state. PORT1 is used as the 16-bit address bus (A) in demultiplexed bus modes: if at least BUSCONx is configured such the demultiplexed mode is selected, the pis of PORT1 are not available for general purpose I/O function. The input threshold of Port 1 is selectable (TTL or CMOS). The pins of P1L also serve as the additional (up to 8) analog input channels for the A/D converter, where P1L.x equals ANy (Analog input channel y, where y = x + 16). This additional function have higher priority on demultiplexed bus function. The following PORT1 pins have alternate functions:
	132	I	P1H.4 CC24IO CAPCOM2: CC24 capture input
	133	I	P1H.5 CC25IO CAPCOM2: CC25 capture input
	134	I	P1H.6 CC26IO CAPCOM2: CC26 capture input
	135	I	P1H.7 CC27IO CAPCOM2: CC27 capture input

Power supply drop

If, during a write operation, the internal low voltage supply drops below a certain internal voltage threshold, any write operation running is suddenly interrupted and the module is reset to Read mode. At following Power-on, the interrupted Flash write operation must be repeated.

5.4 Registers description

5.4.1 Flash control register 0 low

The Flash Control Register 0 Low (FCR0L), together with the Flash Control Register 0 High (FCR0H), is used to enable and to monitor all the write operations on the IFlash. The user has no access in write mode to the Test-Flash (B0TF). Besides, Test-Flash block is seen by the user in Bootstrap mode only.

FCR0L (0x0E 0000) FCR Reset Value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved									BSY1	BSY0	LOCK	res.	res.	res.	res.
									R	R	R				

Table 7. Flash control register 0 low

Bit	Function
BSY(1:0)	Bank 0:1 Busy (IFlash) These bits indicate that a write operation is running on Bank 0 or Bank 1(IFlash). They are automatically set when bit WMS is set. Setting Protection operation sets bits BSYx (since protection registers are in this Block). When this bits are set, every read access to the corresponding bank will output invalid data (software trap 009Bh), while every write access to the bank will be ignored. At the end of the write operation or during a Program or Erase Suspend these bits are automatically reset and the bank returns to read mode. After a Program or Erase Resume these bits is automatically set again.
LOCK	Flash registers access locked When this bit is set, it means that the access to the Flash Control Registers FCR0H/-FCR1H/L, FDR0H/L-FDR1H/L, FARH/L and FER is locked by the FPEC: any read access to the registers will output invalid data (software trap 009Bh) and any write access will be ineffective. LOCK bit is automatically set when the Flash bit WMS is set. This is the only bit the user can always access to detect the status of the Flash: once it is found low, the rest of FCR0L and all the other Flash registers are accessible by the user as well. Note that FER content can be read when LOCK is low, but its content is updated only when also BSYx bits are reset.

Set Protection

Example 1: Enable Write Protection of sectors B0F3-0 of Bank 0.

```
FCR0H  |= 0x0100;       /*Set SPR in FCR0H*/
FARL    = 0xDFB4;       /*Load Add of register FNVWPIR in FARL*/
FARH    = 0x000E;       /*Load Add of register FNVWPIR in FARH*/
FDR0L   = 0xFFF0;       /*Load Data in FDR0L*/
FDR0H   = 0xFFFF;       /*Load Data in FDR0H*/
FCR0H  |= 0x8000;       /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Example 2: Enable Access and Debug Protection.

```
FCR0H  |= 0x0100;       /*Set SPR in FCR0H*/
FARL    = 0xDFB8;       /*Load Add of register FNVAPR0 in FARL*/
FARH    = 0x000E;       /*Load Add of register FNVAPR0 in FARH*/
FDR0L   = 0xFFFC;       /*Load Data in FDR0L*/
FCR0H  |= 0x8000;       /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Example 3: Disable in a permanent way Access and Debug Protection.

```
FCR0H    |= 0x0100;    /*Set SPR in FCR0H*/
FARL      = 0xDFBC;    /*Load Add of register FNVAPR1L in FARL*/
FARH      = 0x000E;    /*Load Add of register FNVAPR1L in FARH*/
FDR0L     = 0xFFFE;    /*Load Data in FDR0L for clearing PDS0*/
FCR0H    |= 0x8000;    /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Example 4: Enable again in a permanent way Access and Debug Protection, after having disabled them.

```
FCR0H    |= 0x0100;      /*Set SPR in FCR0H*/
FARL      = 0xDFBC;      /*Load Add register FNVAPR1H in FARL*/
FARH      = 0x000E;      /*Load Add register FNVAPR1H in FARH*/
FDR0H     = 0xFFFE;      /*Load Data in FDR0H for clearing
PEN0*/
FCR0H    |= 0x8000;      /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Disable and re-enable of Access and Debug Protection in a permanent way (as shown by examples 3 and 4) can be done for a maximum of 16 times.

5.7 Write operation summary

In general, each write operation is started through a sequence of 3 steps:

1. The first instruction is used to select the desired operation by setting its corresponding selection bit in the Flash Control Register 0.
2. The second step is the definition of the Address and Data for programming or the sectors or banks to erase, SMOD must be always set except for writing in Flash Non Volatile Protection registers.
3. The last instruction is used to start the write operation, by setting the start bit WMS in the FCR0.

Once selected, but not yet started, one operation can be canceled by resetting the operation selection bit.

A summary of the available Flash Module Write Operations are shown in the following *Table 25*.

Table 25. Flash write operations

Operation	Select bit	Address and data	Start bit
Word program (32-bit)	WPG	FARL/FARH FDR0L/FDR0H	WMS
Double word program (64-bit)	DWPG	FARL/FARH FDR0L/FDR0H FDR1L/FDR1H	WMS
Sector erase	SER	FCR1L/FCR1H	WMS
Set protection	SPR	FDR0L/FDR0H	WMS
Program/Erase suspend	SUSP	None	None

Table 29. Interrupt sources (continued)

Source of Interrupt or PEC Service Request	Request Flag	Enable Flag	Interrupt Vector	Vector Location	Trap Number
CAPCOM register 6	CC6IR	CC6IE	CC6INT	00'0058h	16h
CAPCOM register 7	CC7IR	CC7IE	CC7INT	00'005Ch	17h
CAPCOM register 8	CC8IR	CC8IE	CC8INT	00'0060h	18h
CAPCOM register 9	CC9IR	CC9IE	CC9INT	00'0064h	19h
CAPCOM register 10	CC10IR	CC10IE	CC10INT	00'0068h	1Ah
CAPCOM register 11	CC11IR	CC11IE	CC11INT	00'006Ch	1Bh
CAPCOM register 12	CC12IR	CC12IE	CC12INT	00'0070h	1Ch
CAPCOM register 13	CC13IR	CC13IE	CC13INT	00'0074h	1Dh
CAPCOM register 14	CC14IR	CC14IE	CC14INT	00'0078h	1Eh
CAPCOM register 15	CC15IR	CC15IE	CC15INT	00'007Ch	1Fh
CAPCOM register 16	CC16IR	CC16IE	CC16INT	00'00C0h	30h
CAPCOM register 17	CC17IR	CC17IE	CC17INT	00'00C4h	31h
CAPCOM register 18	CC18IR	CC18IE	CC18INT	00'00C8h	32h
CAPCOM register 19	CC19IR	CC19IE	CC19INT	00'00CCh	33h
CAPCOM register 20	CC20IR	CC20IE	CC20INT	00'00D0h	34h
CAPCOM register 21	CC21IR	CC21IE	CC21INT	00'00D4h	35h
CAPCOM register 22	CC22IR	CC22IE	CC22INT	00'00D8h	36h
CAPCOM register 23	CC23IR	CC23IE	CC23INT	00'00DCh	37h
CAPCOM register 24	CC24IR	CC24IE	CC24INT	00'00E0h	38h
CAPCOM register 25	CC25IR	CC25IE	CC25INT	00'00E4h	39h
CAPCOM register 26	CC26IR	CC26IE	CC26INT	00'00E8h	3Ah
CAPCOM register 27	CC27IR	CC27IE	CC27INT	00'00ECh	3Bh
CAPCOM register 28	CC28IR	CC28IE	CC28INT	00'00F0h	3Ch
CAPCOM register 29	CC29IR	CC29IE	CC29INT	00'0110h	44h
CAPCOM register 30	CC30IR	CC30IE	CC30INT	00'0114h	45h
CAPCOM register 31	CC31IR	CC31IE	CC31INT	00'0118h	46h
CAPCOM timer 0	T0IR	T0IE	T0INT	00'0080h	20h
CAPCOM timer 1	T1IR	T1IE	T1INT	00'0084h	21h
CAPCOM timer 7	T7IR	T7IE	T7INT	00'00F4h	3Dh
CAPCOM timer 8	T8IR	T8IE	T8INT	00'00F8h	3Eh
GPT1 timer 2	T2IR	T2IE	T2INT	00'0088h	22h
GPT1 timer 3	T3IR	T3IE	T3INT	00'008Ch	23h
GPT1 timer 4	T4IR	T4IE	T4INT	00'0090h	24h
GPT2 timer 5	T5IR	T5IE	T5INT	00'0094h	25h

10 Capture / compare (CAPCOM) units

The ST10F273E has two 16-channel CAPCOM units which support generation and control of timing sequences on up to 32 channels with a maximum resolution of 125ns at 64 MHz CPU clock.

The CAPCOM units are typically used to handle high speed I/O tasks such as pulse and waveform generation, pulse width modulation (PMW), Digital to Analog (D/A) conversion, software timing, or time recording relative to external events.

Four 16-bit timers (T0/T1, T7/T8) with reload registers provide two independent time bases for the capture/compare register array.

The input clock for the timers is programmable to several prescaled values of the internal system clock, or may be derived from an overflow/underflow of timer T6 in module GPT2.

This provides a wide range of variation for the timer period and resolution and allows precise adjustments to application specific requirements. In addition, external count inputs for CAPCOM timers T0 and T7 allow event scheduling for the capture/compare registers relative to external events.

Each of the two capture/compare register arrays contain 16 dual purpose capture/compare registers, each of which may be individually allocated to either CAPCOM timer T0 or T1 (T7 or T8, respectively), and programmed for capture or compare functions. Each of the 32 registers has one associated port pin which serves as an input pin for triggering the capture function, or as an output pin to indicate the occurrence of a compare event.

When a capture/compare register has been selected for capture mode, the current contents of the allocated timer will be latched (captured) into the capture/compare register in response to an external event at the port pin which is associated with this register. In addition, a specific interrupt request for this capture/compare register is generated.

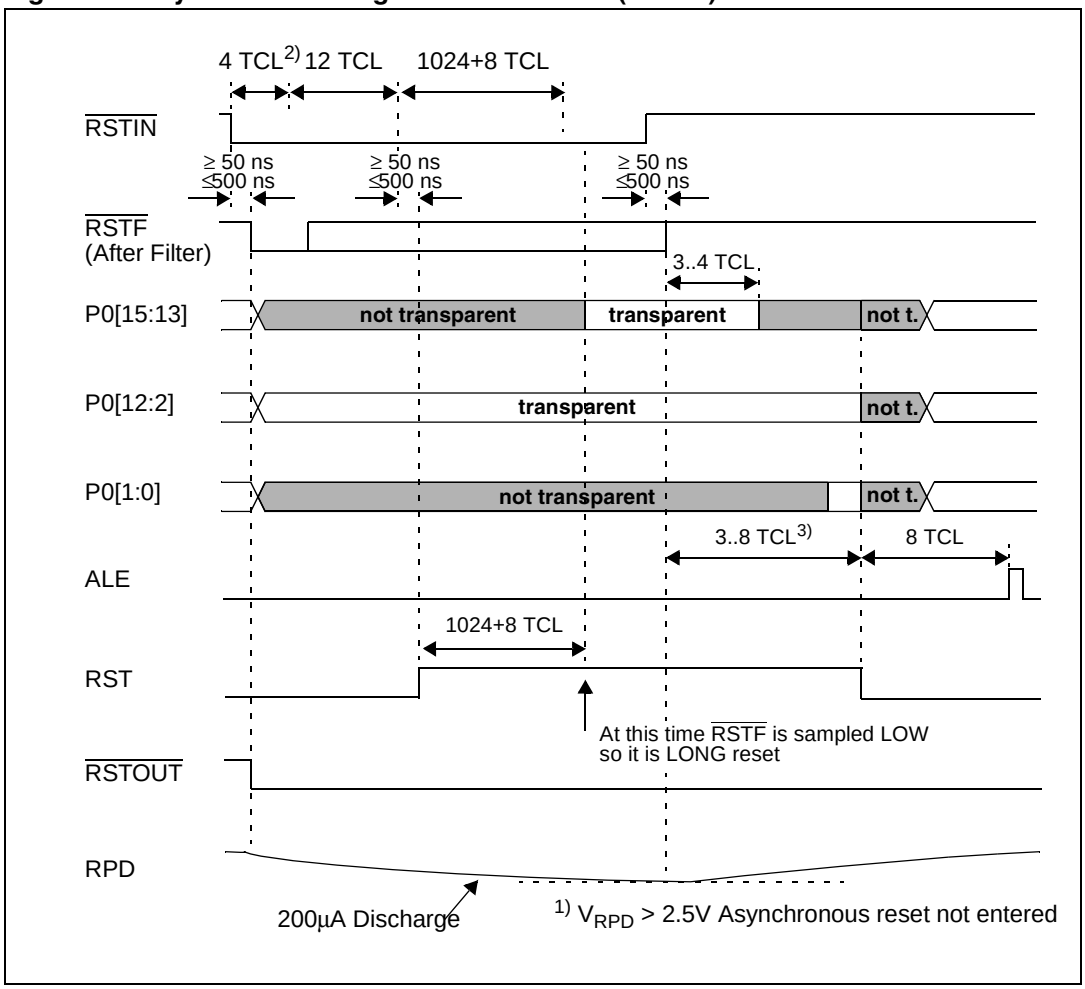
Either a positive, a negative, or both a positive and a negative external signal transition at the pin can be selected as the triggering event. The contents of all registers which have been selected for one of the five compare modes are continuously compared with the contents of the allocated timers.

When a match occurs between the timer value and the value in a capture / compare register, specific actions will be taken based on the selected compare mode.

The input frequencies f_{Tx}, for the timer input selector Tx, are determined as a function of the CPU clocks. The timer input frequencies, resolution and periods which result from the selected pre-scaler option in TxI when using a 40 MHz and 64 MHz CPU clock are listed in the *Table 33* and *Table 34* respectively.

The numbers for the timer periods are based on a reload value of 0000h. Note that some numbers may be rounded to 3 significant figures.

Figure 22. Synchronous long hardware RESET ($\overline{EA}$ = 0)



1) If during the reset condition ($\overline{RSTIN}$ low), RPD voltage drops below the threshold voltage (about 2.5V for 5V operation), the asynchronous reset is then immediately entered.

2) Minimum $\overline{RSTIN}$ low pulse duration shall also be longer than 500ns to guarantee the pulse is not masked by the internal filter (refer to Section 21.1).

3) 3 to 8 TCL depending on clock source selection.

20.4 Software reset

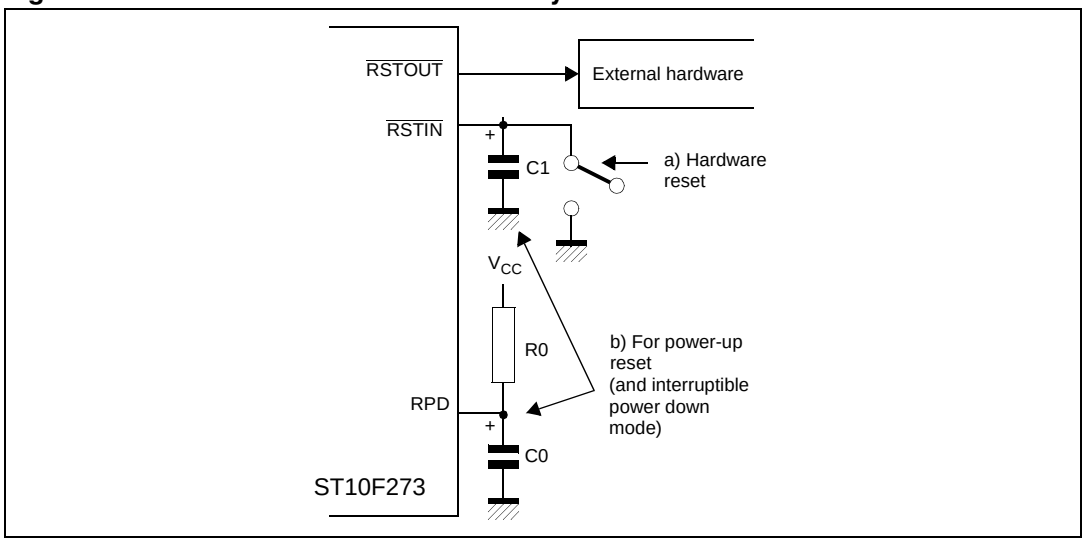
A software reset sequence can be triggered at any time by the protected SRST (software reset) instruction. This instruction can be deliberately executed within a program, e.g. to leave bootstrap loader mode, or on a hardware trap that reveals system failure.

On execution of the SRST instruction, the internal reset sequence is started. The microcontroller behavior is the same as for a synchronous short reset, except that only bits P0.12...P0.8 are latched at the end of the reset sequence, while previously latched, bits P0.7...P0.2 are cleared (that is written at ‘1’).

A Software reset is always taken as synchronous: there is no influence on Software Reset behavior with RPD status. In case Bidirectional Reset is selected, a Software Reset event pulls $\overline{RSTIN}$ pin low: this occurs only if RPD is high; if RPD is low, $\overline{RSTIN}$ pin is not pulled low even though Bidirectional Reset is selected.

To ensure correct power-up reset with controlled supply current consumption, specially if clock signal requires a long period of time to stabilize, an asynchronous hardware reset is required during power-up. For this reason, it is recommended to connect the external R0-C0 circuit shown in Figure 28 to the RPD pin. On power-up, the logical low level on RPD pin forces an asynchronous hardware reset when $\overline{\text{RSTIN}}$ is asserted low. The external pull-up R0 will then charge the capacitor C0. Note that an internal pull-down device on RPD pin is turned on when $\overline{\text{RSTIN}}$ pin is low, and causes the external capacitor (C0) to begin discharging at a typical rate of 100-200µA. With this mechanism, after power-up reset, short low pulses applied on $\overline{\text{RSTIN}}$ produce synchronous hardware reset. If $\overline{\text{RSTIN}}$ is asserted longer than the time needed for C0 to be discharged by the internal pull-down device, then the device is forced in an asynchronous reset. This mechanism insures recovery from very catastrophic failure.

Figure 28. Minimum external reset circuitry



The minimum reset circuit of *Figure 28* is not adequate when the $\overline{\text{RSTIN}}$ pin is driven from the ST10F273E itself during software or watchdog triggered resets, because of the capacitor C1 that will keep the voltage on $\overline{\text{RSTIN}}$ pin above V_{IL} after the end of the internal reset sequence, and thus will trigger an asynchronous reset sequence.

Figure 29 shows an example of a reset circuit. In this example, R1-C1 external circuit is only used to generate power-up or manual reset, and R0-C0 circuit on RPD is used for power-up reset and to exit from Power down mode. Diode D1 creates a wired-OR gate connection to the reset pin and may be replaced by open-collector Schmitt trigger buffer. Diode D2 provides a faster cycle time for repetitive power-on resets.

R2 is an optional pull-up for faster recovery and correct biasing of TTL Open Collector drivers.

Warning: **During power-off phase, it is important that the external hardware maintains a stable ground level on $\overline{\text{RSTIN}}$ pin, without any glitch, in order to avoid spurious exiting from reset status with unstable power supply.**

21.3.2 Exiting stand-by mode

After the system has entered the Stand-by mode, the procedure to exit this mode consists of a standard Power-on sequence, with the only difference that the RAM is already powered through V_{18SB} internal reference (derived from V_{STBY} pin external voltage).

It is recommended to held the device under RESET ($\overline{\text{RSTIN}}$ pin forced low) until external V_{DD} voltage pin is stable. Even though, at the very beginning of the power-on phase, the device is maintained under reset by the internal low voltage detector circuit (implemented inside the main voltage regulator) till the internal V_{18} becomes higher than about 1.0V, **there is no warranty that the device stays under reset status if $\overline{\text{RSTIN}}$ is at high level during power ramp up. So, it is important the external hardware is able to guarantee a stable ground level on $\overline{\text{RSTIN}}$ along the power-on phase, without any temporary glitch.**

The external hardware shall be responsible to drive low the $\overline{\text{RSTIN}}$ pin until the V_{DD} is stable, even though the internal LVD is active.

Once the internal Reset signal goes low, the RAM (still frozen) power supply is switched to the main V_{18}.

At this time, everything becomes stable, and the execution of the initialization routines can start: XRAM2EN bit can be set, enabling the RAM.

21.3.3 Real time clock and stand-by mode

When Stand-by mode is entered (turning off the main supply V_{DD}), the Real Time Clock counting can be maintained running in case the on-chip 32 kHz oscillator is used to provide the reference to the counter. This is not possible if the main oscillator is used as reference for the counter: Being the main oscillator powered by V_{DD}, once this is switched off, the oscillator is stopped.

Table 53. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
PW1	FE32h	19h	PWM module pulse width register 1	0000h
PW2	FE34h	1Ah	PWM module pulse width register 2	0000h
PW3	FE36h	1Bh	PWM module pulse width register 3	0000h
PWMCON0 **b**	FF30h	98h	PWM module control register 0	0000h
PWMCON1 **b**	FF32h	99h	PWM module control register 1	0000h
PWMIC **b**	F17Eh **E**	BFh	PWM module interrupt control register	- - 00h
QR0	F004h **E**	02h	MAC unit offset register r0	0000h
QR1	F006h **E**	03h	MAC unit offset register R1	0000h
QX0	F000h **E**	00h	MAC unit offset register X0	0000h
QX1	F002h **E**	01h	MAC unit offset register X1	0000h
RP0H **b**	F108h **E**	84h	System start-up configuration register (read only)	- - XXh
S0BG	FEB4h	5Ah	Serial channel 0 baud rate generator reload register	0000h
S0CON **b**	FFB0h	D8h	Serial channel 0 control register	0000h
S0EIC **b**	FF70h	B8h	Serial channel 0 error interrupt control register	- - 00h
S0RBUF	FEB2h	59h	Serial channel 0 receive buffer register (read only)	- - XXh
S0RIC **b**	FF6Eh	B7h	Serial channel 0 receive interrupt control register	- - 00h
S0TBIC **b**	F19Ch **E**	CEh	Serial channel 0 transmit buffer interrupt control reg.	- - 00h
S0TBUF	FEB0h	58h	Serial channel 0 transmit buffer register (write only)	0000h
S0TIC **b**	FF6Ch	B6h	Serial channel 0 transmit interrupt control register	- - 00h
SP	FE12h	09h	CPU system stack pointer register	FC00h
SSCBR	F0B4h **E**	5Ah	SSC Baud rate register	0000h
SSCCON **b**	FFB2h	D9h	SSC control register	0000h
SSCEIC **b**	FF76h	BBh	SSC error interrupt control register	- - 00h
SSCRB	F0B2h **E**	59h	SSC receive buffer (read only)	XXXXh
SSCRIC **b**	FF74h	BAh	SSC receive interrupt control register	- - 00h
SSCTB	F0B0h **E**	58h	SSC transmit buffer (write only)	0000h
SSCTIC **b**	FF72h	B9h	SSC transmit interrupt control register	- - 00h
STKOV	FE14h	0Ah	CPU stack overflow pointer register	FA00h
STKUN	FE16h	0Bh	CPU stack underflow pointer register	FC00h
SYSCON **b**	FF12h	89h	CPU system configuration register	0xx0h [1]
T0	FE50h	28h	CAPCOM timer 0 register	0000h
T01CON **b**	FF50h	A8h	CAPCOM timer 0 and timer 1 control register	0000h
T0IC **b**	FF9Ch	CEh	CAPCOM timer 0 interrupt control register	- - 00h
T0REL	FE54h	2Ah	CAPCOM timer 0 reload register	0000h

Table 53. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
XPERCON **b**	F024h **E**	12h	XPER configuration register	- - 05h
ZEROS **b**	FF1Ch	8Eh	Constant value 0's register (read only)	0000h

Note: 1. The system configuration is selected during reset. SYSCON reset value is 0000 0xx0 x000 0000b.

2. Reset Value depends on different triggered reset event.

3. The XPnIC Interrupt Control Registers control interrupt requests from integrated X-Bus peripherals. Some software controlled interrupt requests may be generated by setting the XPnIR bits (of XPnIC register) of the unused X-Peripheral nodes.

23.2 X-registers

The following table lists all X-Bus registers which are implemented in the ST10F273E ordered by their name. The FLASH control registers are listed in a separate section, in spite of they also are physically mapped on X-Bus memory space. Note that all X-Registers are not bit-addressable.

Table 54. List of XBus registers

Name	Physical address	Description	Reset value
CAN1BRPER	EF0Ch	CAN1: BRP extension register	0000h
CAN1BTR	EF06h	CAN1: Bit timing register	2301h
CAN1CR	EF00h	CAN1: CAN control register	0001h
CAN1EC	EF04h	CAN1: error counter	0000h
CAN1IF1A1	EF18h	CAN1: IF1 arbitration 1	0000h
CAN1IF1A2	EF1Ah	CAN1: IF1 arbitration 2	0000h
CAN1IF1CM	EF12h	CAN1: IF1 command mask	0000h
CAN1IF1CR	EF10h	CAN1: IF1 command request	0001h
CAN1IF1DA1	EF1Eh	CAN1: IF1 data A 1	0000h
CAN1IF1DA2	EF20h	CAN1: IF1 data A 2	0000h
CAN1IF1DB1	EF22h	CAN1: IF1 data B 1	0000h
CAN1IF1DB2	EF24h	CAN1: IF1 data B 2	0000h
CAN1IF1M1	EF14h	CAN1: IF1 mask 1	FFFFh
CAN1IF1M2	EF16h	CAN1: IF1 mask 2	FFFFh
CAN1IF1MC	EF1Ch	CAN1: IF1 message control	0000h
CAN1IF2A1	EF48h	CAN1: IF2 arbitration 1	0000h
CAN1IF2A2	EF4Ah	CAN1: IF2 arbitration 2	0000h
CAN1IF2CM	EF42h	CAN1: IF2 command mask	0000h

Table 54. List of XBus registers (continued)

Name	Physical address	Description	Reset value
RTCDL	ED0Ah	RTC divider counter low byte	XXXXh
RTCH	ED10h	RTC programmable counter high byte	XXXXh
RTCL	ED0Eh	RTC programmable counter low byte	XXXXh
RTCPH	ED08h	RTC prescaler register high byte	XXXXh
RTCPL	ED06h	RTC prescaler register low byte	XXXXh
XCLKOUTDIV	EB02h	CLKOUT divider control register	- - 00h
XEMU0	EB76h	XBUS emulation register 0 (write only)	XXXXh
XEMU1	EB78h	XBUS emulation register 1 (write only)	XXXXh
XEMU2	EB7Ah	XBUS emulation register 2 (write only)	XXXXh
XEMU3	EB7Ch	XBUS emulation register 3 (write only)	XXXXh
XIR0CLR	EB14h	X-Interrupt 0 clear register (write only)	0000h
XIR0SEL	EB10h	X-Interrupt 0 selection register	0000h
XIR0SET	EB12h	X-Interrupt 0 set register (write only)	0000h
XIR1CLR	EB24h	X-Interrupt 1 clear register (write only)	0000h
XIR1SEL	EB20h	X-Interrupt 1 selection register	0000h
XIR1SET	EB22h	X-Interrupt 1 set register (write only)	0000h
XIR2CLR	EB34h	X-Interrupt 2 clear register (write only)	0000h
XIR2SEL	EB30h	X-Interrupt 2 selection register	0000h
XIR2SET	EB32h	X-Interrupt 2 set register (write only)	0000h
XIR3CLR	EB44h	X-Interrupt 3 clear selection register (write only)	0000h
XIR3SEL	EB40h	X-Interrupt 3 selection register	0000h
XIR3SET	EB42h	X-Interrupt 3 set selection register (write only)	0000h
XMISC	EB46h	XBUS miscellaneous features register	0000h
XP1DIDIS	EB36h	Port 1 digital disable register	0000h
XPEREMU	EB7Eh	XPERCON copy for emulation (write only)	XXXXh
XPICON	EB26h	Extended port input threshold control register	- - 00h
XPOLAR	EC04h	XPWM module channel polarity register	0000h
XPP0	EC20h	XPWM module period register 0	0000h
XPP1	EC22h	XPWM module period register 1	0000h
XPP2	EC24h	XPWM module period register 2	0000h
XPP3	EC26h	XPWM module period register 3	0000h
XPT0	EC10h	XPWM module up/down counter 0	0000h
XPT1	EC12h	XPWM module up/down counter 1	0000h
XPT2	EC14h	XPWM module up/down counter 2	0000h

Table 54. List of XBus registers (continued)

Name	Physical address	Description	Reset value
XPT3	EC16h	XPWM module up/down counter 3	0000h
XPW0	EC30h	XPWM module pulse width register 0	0000h
XPW1	EC32h	XPWM module pulse width register 1	0000h
XPW2	EC34h	XPWM module pulse width register 2	0000h
XPW3	EC36h	XPWM module pulse width register 3	0000h
XPWMCON0	EC00h	XPWM module control register 0	0000h
XPWMCON0CLR	EC08h	XPWM module clear control reg. 0 (write only)	0000h
XPWMCON0SET	EC06h	XPWM module set control register 0 (write only)	0000h
XPWMCON1	EC02h	XPWM module control register 1	0000h
XPWMCON1CLR	EC0Ch	XPWM module clear control reg. 0 (write only)	0000h
XPWMCON1SET	EC0Ah	XPWM module set control register 0 (write only)	0000h
XPWMPORT	EC80h	XPWM module port control register	0000h
XS1BG	E906h	XASC Baud rate generator reload register	0000h
XS1CON	E900h	XASC control register	0000h
XS1CONCLR	E904h	XASC clear control register (write only)	0000h
XS1CONSET	E902h	XASC set control register (write only)	0000h
XS1PORT	E980h	XASC port control register	0000h
XS1RBUF	E90Ah	XASC receive buffer register	0000h
XS1TBUF	E908h	XASC transmit buffer register	0000h
XSSCBR	E80Ah	XSSC Baud rate register	0000h
XSSCCON	E800h	XSSC control register	0000h
XSSCCONCLR	E804h	XSSC clear control register (write only)	0000h
XSSCCONSET	E802h	XSSC set control register (write only)	0000h
XSSCPORT	E880h	XSSC port control register	0000h
XSSCRB	E808h	XSSC receive buffer	XXXXh
XSSCTB	E806h	XSSC transmit buffer	0000h

23.3 Flash registers ordered by name

The following table lists all Flash Control Registers which are implemented in the ST10F273E ordered by their name. These registers are physically mapped on the IBus, except for XFVTAUR0, which is mapped on XBus. Note that these registers are not bit-addressable.

Table 55. List of flash registers

Name	Physical address	Description	Reset value
FARH	0x000E 0012	Flash address register - high	0000h
FARL	0x000E 0010	Flash address register - low	0000h
FCR0H	0x000E 0002	Flash control register 0 - high	0000h
FCR0L	0x000E 0000	Flash control register 0 - low	0000h
FCR1H	0x000E 0006	Flash control register 1 - high	0000h
FCR1L	0x000E 0004	Flash control register 1 - low	0000h
FDR0H	0x000E 000A	Flash data register 0 - high	FFFFh
FDR0L	0x000E 0008	Flash data register 0 - low	FFFFh
FDR1H	0x000E 000E	Flash data register 1 - high	FFFFh
FDR1L	0x000E 000C	Flash data register 1 - low	FFFFh
FER	0x000E 0014	Flash error register	0000h
FNVAPR0	0x000E DFB8	Flash non volatile access protection reg.0	ACFFh
FNVAPR1H	0x000E DFBE	Flash non volatile access protection reg.1 - high	FFFFh
FNVAPR1L	0x000E DFBC	Flash non volatile access protection reg.1 - low	FFFFh
FNVWPIRH	0x000E DFB6	Flash non volatile protection i register high	FFFFh
FNVWPIRL	0x000E DFB4	Flash non volatile protection i register low	FFFFh

23.4 Identification registers

The ST10F273E have four Identification registers, mapped in ESFR space. These registers contain:

- A manufacturer identifier
- A chip identifier with its revision
- A internal Flash and size identifier
- Programming voltage description

Note: The ST10F273E device is a commercial version based on the ST10F276E silicon, the identification registers provide the values corresponding to the ST10F276E device.

Table 62. Thermal characteristics

Symbol	Description	Value (typical)	Unit
Θ_{JA}	Thermal resistance junction-ambient PQFP 144 - 28 x 28 x 3.4 mm / 0.65 mm pitch TQFP 144 - 20 x 20 mm / 0.5 mm pitch TQFP 144 - 20 x 20 mm / 0.5 mm pitch on four layer FR4 board (2 layers signals / 2 layers power)	 30 40 35	°C/W

Based on thermal characteristics of the package and with reference to the power consumption figures provided in next tables and diagrams, the following product classification can be proposed. Anyhow, the exact power consumption of the device inside the application must be computed according to different working conditions, thermal profiles, real thermal resistance of the system (including printed circuit board or other substrata), I/O activity, and so on.

Table 63. Product classification

Package	Ambient temperature range	CPU frequency range
Die	–40°C to +125°C	1 to 64 MHz
PQFP 144	–40°C to +125°C	1 to 64 MHz
TQFP 144	–40°C to +125°C	1 to 40 MHz
	–40°C to +105°C	1 to 48 MHz

24.4 Parameter interpretation

The parameters listed in the following tables represent the characteristics of the ST10F273E and its demands on the system.

Where the ST10F273E logic provides signals with their respective timing characteristics, the symbol “CC” for Controller Characteristics, is included in the “Symbol” column. Where the external system must provide signals with their respective timing characteristics to the ST10F273E, the symbol “SR” for System Requirement, is included in the “Symbol” column.

10. The Idle mode supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the Figure 35 below. These parameters are tested and at maximum CPU clock with all outputs disconnected and all inputs at V_{IL} or V_{IH}, $\overline{\text{RSTIN}}$ pin at V_{IH1Min}.
11. This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{AREF} = 0 V, all outputs (including pins configured as outputs) disconnected. Besides, the Main Voltage Regulator is assumed off: in case it is not, additional 1mA shall be assumed. The value for this parameter shall be considered as “Target Value” to be confirmed by silicon characterization.
12. Overload conditions occur if the standard operating conditions are exceeded, i.e. the voltage on any pin exceeds the specified range (i.e. $V_{OV} > V_{DD}$ + 0.3 V or $V_{OV} < –0.3$ V). The absolute sum of input overload currents on all port pins may not exceed 50mA. The supply voltage must remain within the specified limits.
13. This parameter is tested including leakage currents. All inputs (including pins configured as inputs) at 0 V to 0.1 V or at V_{DD} – 0.1 V to V_{DD}, V_{AREF} = 0 V, all outputs (including pins configured as outputs) disconnected. Besides, the Main Voltage Regulator is assumed off: in case it is not, additional 1mA shall be assumed. The value for this parameter shall be considered as “Target Value” to be confirmed by silicon characterization.

Figure 35. Port2 test mode structure

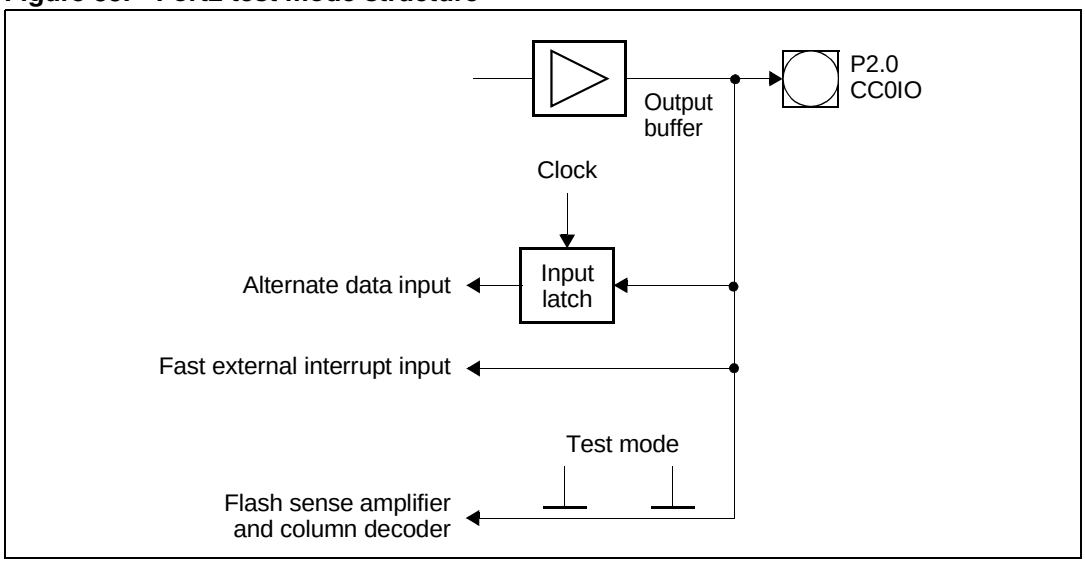
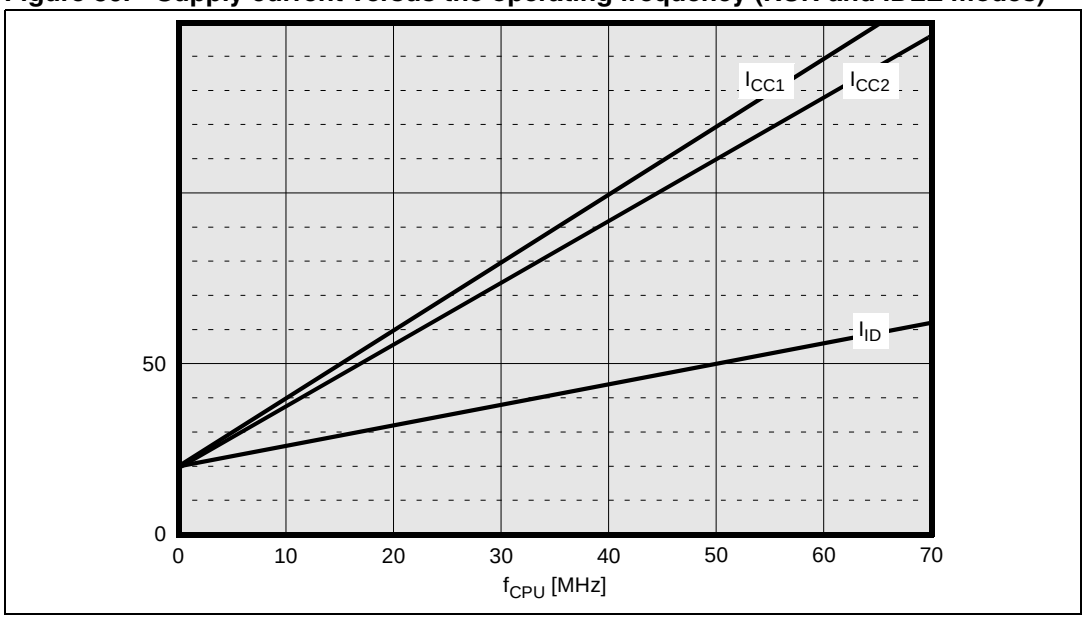


Figure 36. Supply current versus the operating frequency (RUN and IDLE modes)



24.8.2 Definition of internal timing

The internal operation of the ST10F273E is controlled by the internal CPU clock f_{CPU}. Both edges of the CPU clock can trigger internal (for example pipeline) or external (for example bus cycles) operations.

The specification of the external timing (AC Characteristics) therefore depends on the time between two consecutive edges of the CPU clock, called “TCL”.

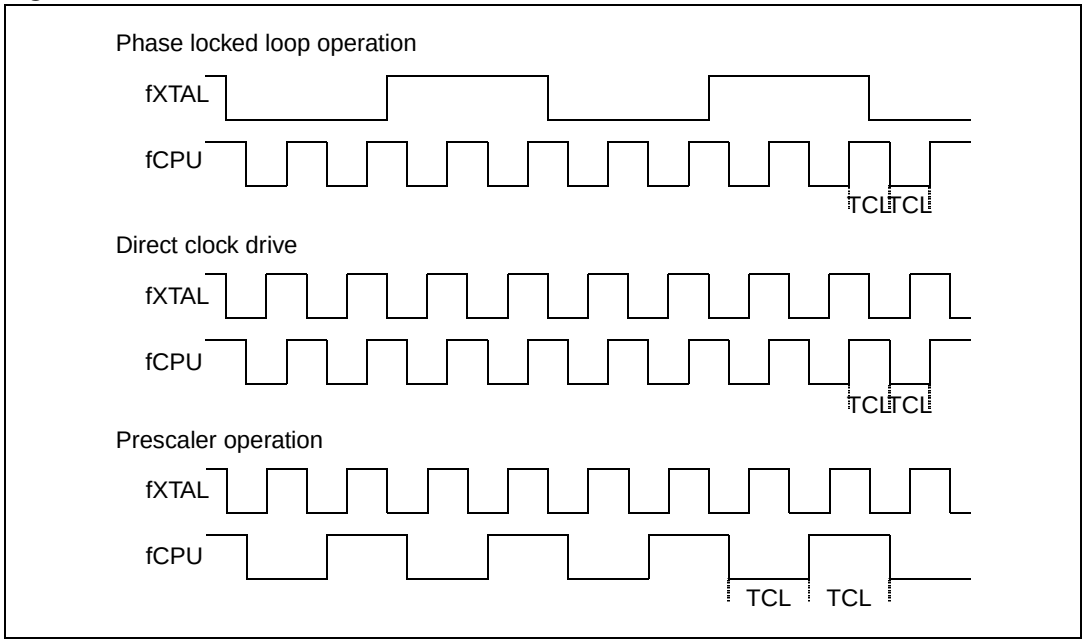
The CPU clock signal can be generated by different mechanisms. The duration of TCL and its variation (and also the derived external timing) depends on the mechanism used to generate f_{CPU}.

This influence must be regarded when calculating the timings for the ST10F273E.

The example for PLL operation shown in *Figure 43* refers to a PLL factor of 4.

The mechanism used to generate the CPU clock is selected during reset by the logic levels on pins P0.15-13 (P0H.7-5).

Figure 43. Generation mechanisms for the CPU clock



24.8.19 External bus arbitration

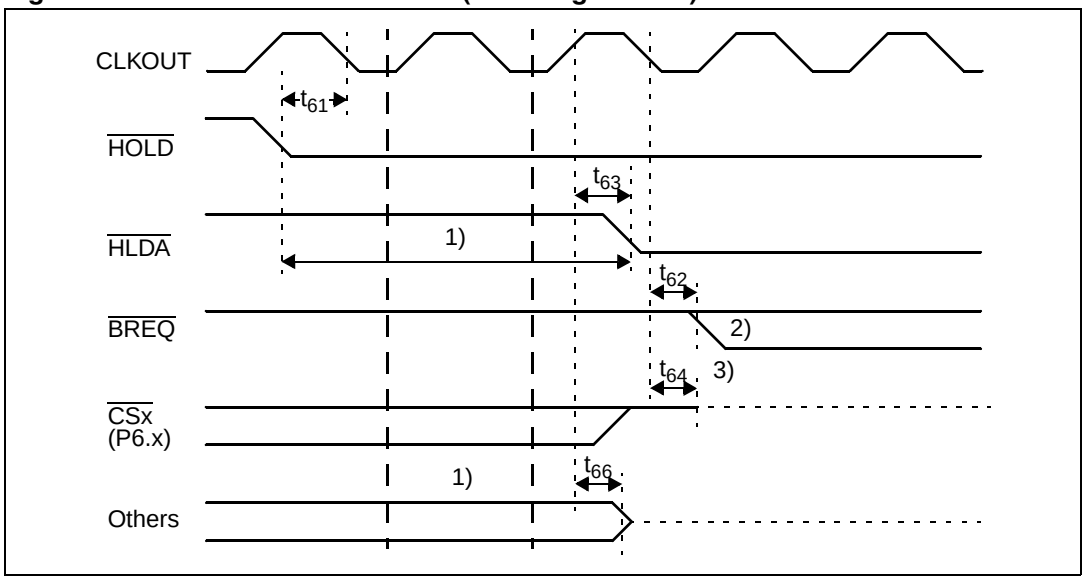
V_{DD} = 5V ± 10%, V_{SS} = 0V, T_A = -40°C to +125°C, C_L = 50pF

Table 80. External bus arbitration timings

Symbol		Parameter	F_{CPU} = 40 MHz TCL = 12.5 ns		Variable CPU Clock 1/2 TCL = 1 to 64 MHz		Unit
			Min.	Max.	Min.	Max.	
t_{61}	SR	$\overline{HOLD}$ input setup time to CLKOUT	18.5	–	18.5	–	ns
t_{62}	CC	CLKOUT to $\overline{HLDA}$ high or $\overline{BREQ}$ low delay	–	12.5	–	12.5	
t_{63}	CC	CLKOUT to $\overline{HLDA}$ low or $\overline{BREQ}$ high delay	–	12.5	–	12.5	
t_{64}	CC	$\overline{CSx}$ release(1)	–	20	–	20	
t_{65}	CC	$\overline{CSx}$ drive	– 4	15	– 4	15	
t_{66}	CC	Other signals release(1)	–	20	–	20	
t_{67}	CC	Other signals drive	– 4	15	– 4	15	

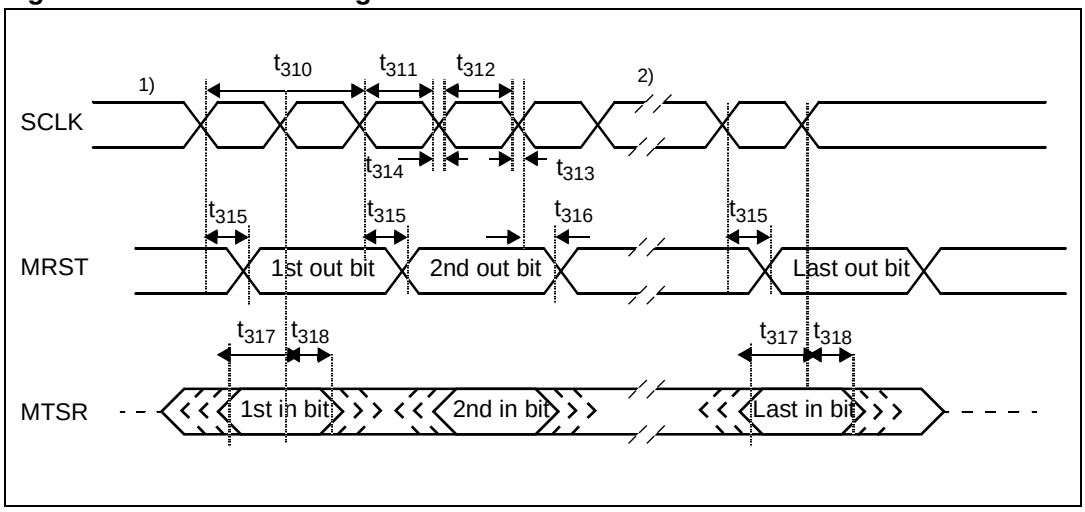
1. Partially tested, guaranteed by design characterization

Figure 57. External bus arbitration (releasing the bus)



1. The ST10F273E will complete the currently running bus cycle before granting bus access.
2. This is the first possibility for $\overline{BREQ}$ to become active.
3. The $\overline{CS}$ outputs will be resistive high (pull-up) after t_{64}.

Figure 60. SSC slave timing



1. The phase and polarity of shift and latch edge of SCLK is programmable. This figure uses the leading clock edge as shift edge (drawn in bold), with latch on trailing edge (SSCPH = 0b), Idle clock line is low, leading clock edge is low-to-high transition (SSCPO = 0b).
2. The bit timing is repeated for all bits to be transmitted or received.