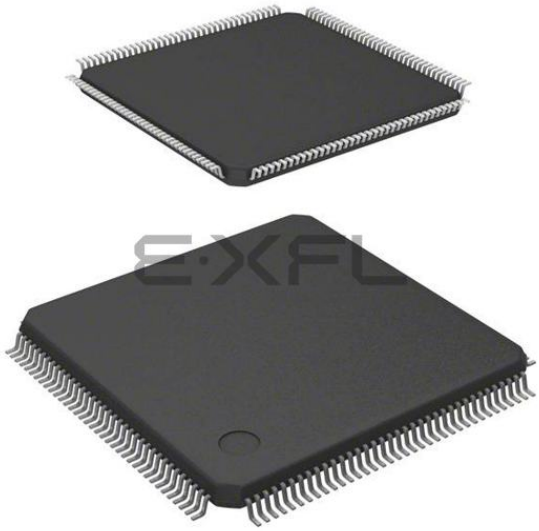

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST10
Core Size	16-Bit
Speed	40MHz
Connectivity	ASC, CANbus, EBI/EMI, I²C, SSC, UART/USART
Peripherals	POR, PWM, WDT
Number of I/O	111
Program Memory Size	512KB (512K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	36K x 8
Voltage - Supply (Vcc/Vdd)	4.5V ~ 5.5V
Data Converters	A/D 24x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	144-LQFP
Supplier Device Package	144-LQFP (20x20)
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/f273-ceg-t

5.4.4 Flash control register 1 high

The Flash Control Register 1 High (FCR1H), together with Flash Control Register 1 Low (FCR1L), is used to select the sectors to Erase or, during any write operation, to monitor the status of each sector and bank.

FCR1H (0x0E 0006) FCR Reset value: 0000h

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
reserved						B1S	B0S	reserved						B1F1	B1F0
						RS	RS							RS	RS

Table 10. Flash control register 1 high

Bit	Function
B1F(1:0)	Bank 1 IFlash sector 1:0 status These bits must be set during a Sector Erase operation to select the sectors to erase in Bank 1. Besides, during any erase operation, these bits are automatically set and give the status of the two sectors of Bank 1 (B1F1-B1F0). The meaning of B1Fy bit for Sector y of Bank 0 is given by the next *Table 11* Banks (BxS) and Sectors (BxFy) Status bits meaning. These bits are automatically reset at the end of a Write operation if no errors are detected.
B0S	Bank 0 status During any erase operation, this bit is automatically modified and gives the status of the Bank 0. The meaning of B0S bit is given in the next *Table 11* Banks (BxS) and Sectors (BxFy) Status bits meaning. This bit is automatically reset at the end of a erase operation if no errors are detected.
B1S	Bank 1 status During any erase operation, this bit is automatically modified and gives the status of the Bank 1. The meaning of B1S bit is given in the next *Table 11* Banks (BxS) and Sectors (BxFy) Status bits meaning. This bit is automatically reset at the end of a erase operation if no errors are detected.

Table 11. Banks (BxS) and sectors (BxFy) status bits meaning

ERR	SUSP	BxS = 1 meaning	BxFy = 1 meaning
1	-	Erase error in bank x	Erase error in sector y of bank x
0	1	Erase suspended in bank x	Erase suspended in sector y of bank x
0	0	Don't care	Don't care

Set Protection

Example 1: Enable Write Protection of sectors B0F3-0 of Bank 0.

```
FCR0H  |= 0x0100;       /*Set SPR in FCR0H*/
FARL    = 0xDFB4;       /*Load Add of register FNVWPIR in FARL*/
FARH    = 0x000E;       /*Load Add of register FNVWPIR in FARH*/
FDR0L   = 0xFFF0;       /*Load Data in FDR0L*/
FDR0H   = 0xFFFF;       /*Load Data in FDR0H*/
FCR0H  |= 0x8000;       /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Example 2: Enable Access and Debug Protection.

```
FCR0H  |= 0x0100;       /*Set SPR in FCR0H*/
FARL    = 0xDFB8;       /*Load Add of register FNVAPR0 in FARL*/
FARH    = 0x000E;       /*Load Add of register FNVAPR0 in FARH*/
FDR0L   = 0xFFFC;       /*Load Data in FDR0L*/
FCR0H  |= 0x8000;       /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Example 3: Disable in a permanent way Access and Debug Protection.

```
FCR0H    |= 0x0100;    /*Set SPR in FCR0H*/
FARL      = 0xDFBC;    /*Load Add of register FNVAPR1L in FARL*/
FARH      = 0x000E;    /*Load Add of register FNVAPR1L in FARH*/
FDR0L     = 0xFFFE;    /*Load Data in FDR0L for clearing PDS0*/
FCR0H    |= 0x8000;    /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Example 4: Enable again in a permanent way Access and Debug Protection, after having disabled them.

```
FCR0H    |= 0x0100;      /*Set SPR in FCR0H*/
FARL      = 0xDFBC;      /*Load Add register FNVAPR1H in FARL*/
FARH      = 0x000E;      /*Load Add register FNVAPR1H in FARH*/
FDR0H     = 0xFFFE;      /*Load Data in FDR0H for clearing
PEN0*/
FCR0H    |= 0x8000;      /*Operation start*/
```

Notice that SMOD bit of FCR0H must NOT be set.

Disable and re-enable of Access and Debug Protection in a permanent way (as shown by examples 3 and 4) can be done for a maximum of 16 times.

5.7 Write operation summary

In general, each write operation is started through a sequence of 3 steps:

1. The first instruction is used to select the desired operation by setting its corresponding selection bit in the Flash Control Register 0.
2. The second step is the definition of the Address and Data for programming or the sectors or banks to erase, SMOD must be always set except for writing in Flash Non Volatile Protection registers.
3. The last instruction is used to start the write operation, by setting the start bit WMS in the FCR0.

Once selected, but not yet started, one operation can be canceled by resetting the operation selection bit.

A summary of the available Flash Module Write Operations are shown in the following *Table 25*.

Table 25. Flash write operations

Operation	Select bit	Address and data	Start bit
Word program (32-bit)	WPG	FARL/FARH FDR0L/FDR0H	WMS
Double word program (64-bit)	DWPG	FARL/FARH FDR0L/FDR0H FDR1L/FDR1H	WMS
Sector erase	SER	FCR1L/FCR1H	WMS
Set protection	SPR	FDR0L/FDR0H	WMS
Program/Erase suspend	SUSP	None	None

7.3 MAC coprocessor specific instructions

The *Table 28* lists the MAC instructions of the ST10F273E. The detailed description of each instruction can be found in the “ST10 Family Programming Manual”. Note that all MAC instructions are encoded on 4 bytes.

Table 28. MAC instruction set summary

Mnemonic	Description
CoABS	Absolute value of the accumulator
CoADD(2)	Addition
CoASHR(rnd)	Accumulator arithmetic shift right & optional round
CoCMP	Compare accumulator with operands
CoLOAD(-,2)	Load accumulator with operands
CoMAC(R,u,s,-,rnd)	(Un)signed/(Un)Signed Multiply-Accumulate & Optional Round
CoMACM(R)(u,s,-,rnd)	(Un)Signed/(Un)signed multiply-accumulate with parallel data move & optional round
CoMAX / CoMIN	maximum / minimum of operands and accumulator
CoMOV	Memory to memory move
CoMUL(u,s,-,rnd)	(Un)signed/(Un)signed multiply & optional round
CoNEG(rnd)	Negate accumulator & optional round
CoNOP	No-operation
CoRND	Round accumulator
CoSHL / CoSHR	Accumulator logical shift left / right
CoSTORE	Store a MAC unit register
CoSUB(2,R)	Substraction

8 External bus controller

All of the external memory accesses are performed by the on-chip external bus controller.

The EBC can be programmed to single chip mode when no external memory is required, or to one of four different external memory access modes:

- 16- / 18- / 20- / 24-bit addresses and 16-bit data, demultiplexed
- 16- / 18- / 20- / 24-bit addresses and 16-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, multiplexed
- 16- / 18- / 20- / 24-bit addresses and 8-bit data, demultiplexed

In demultiplexed bus modes addresses are output on PORT1 and data is input / output on PORT0 or P0L, respectively. In the multiplexed bus modes both addresses and data use PORT0 for input / output.

Timing characteristics of the external bus interface (memory cycle time, memory tri-state time, length of ALE and read / write delay) are programmable giving the choice of a wide range of memories and external peripherals.

Up to four independent address windows may be defined (using register pairs ADDRSELx / BUSCONx) to access different resources and bus characteristics.

These address windows are arranged hierarchically where BUSCON4 overrides BUSCON3 and BUSCON2 overrides BUSCON1.

All accesses to locations not covered by these four address windows are controlled by BUSCON0. Up to five external $\overline{CS}$ signals (four windows plus default) can be generated in order to save external glue logic. Access to very slow memories is supported by a ‘Ready’ function.

A $\overline{HOLD}$ / $\overline{HLDA}$ protocol is available for bus arbitration which shares external resources with other bus masters.

The bus arbitration is enabled by setting bit HLDEN in register PSW. After setting HLDEN once, pins P6.7...P6.5 ($\overline{BREQ}$, $\overline{HLDA}$, $\overline{HOLD}$) are automatically controlled by the EBC. In master mode (default after reset) the $\overline{HLDA}$ pin is an output. By setting bit DP6.7 to’1’ the slave mode is selected where pin $\overline{HLDA}$ is switched to input. This directly connects the slave controller to another master controller without glue logic.

For applications which require less external memory space, the address space can be restricted to 1 Mbyte, 256 Kbytes or to 64 Kbytes. Port 4 outputs all eight address lines if an address space of 16M Bytes is used, otherwise four, two or no address lines.

Chip select timing can be made programmable. By default (after reset), the $\overline{CSx}$ lines change half a CPU clock cycle after the rising edge of ALE. With the CSCFG bit set in the SYSCON register the $\overline{CSx}$ lines change with the rising edge of ALE.

The active level of the READY pin can be set by bit RDYPOL in the BUSCONx registers. When the READY function is enabled for a specific address window, each bus cycle within the window must be terminated with the active level defined by bit RDYPOL in the associated BUSCON register.

12 PWM modules

Two pulse width modulation modules are available on ST10F273E: standard PWM0 and XBUS PWM1. They can generate up to four PWM output signals each, using edge-aligned or centre-aligned PWM. In addition, the PWM modules can generate PWM burst signals and single shot outputs. The *Table 39* and *Table 40* show the PWM frequencies for different resolutions. The level of the output signals is selectable and the PWM modules can generate interrupt requests.

Figure 10. Block diagram of PWM module

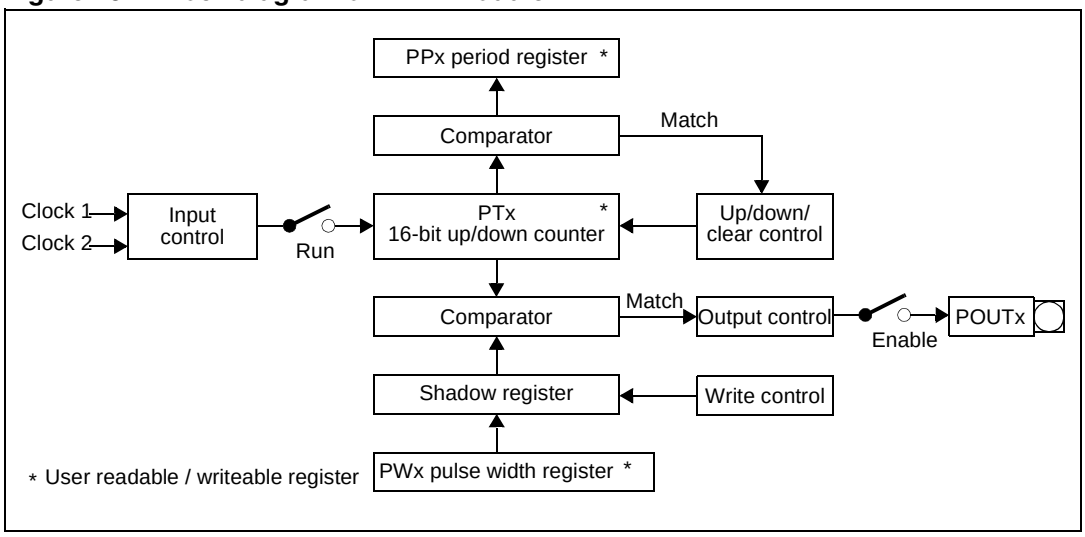


Table 39. PWM unit frequencies and resolutions at 40 MHz CPU clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU Clock/1	25ns	156.25 kHz	39.1 kHz	9.77 kHz	2.44Hz	610Hz
CPU Clock/64	1.6µs	2.44 kHz	610Hz	152.6Hz	38.15Hz	9.54Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPUclock/1	25ns	78.12 kHz	19.53 kHz	4.88 kHz	1.22 kHz	305.2Hz
CPU clock/64	1.6µs	1.22 kHz	305.17Hz	76.29Hz	19.07Hz	4.77Hz

Table 40. PWM unit frequencies and resolutions at 64 MHz CPU clock

Mode 0	Resolution	8-bit	10-bit	12-bit	14-bit	16-bit
CPU clock/1	15.6ns	250 kHz	62.5 kHz	15.63 kHz	3.91Hz	977Hz
CPU clock/64	1.0µs	3.91 kHz	976.6Hz	244.1Hz	61.01Hz	15.26Hz
Mode 1	**Resolution**	**8-bit**	**10-bit**	**12-bit**	**14-bit**	**16-bit**
CPU clock/1	15.6ns	125 kHz	31.25 kHz	7.81 kHz	1.95 kHz	488.3Hz
CPU clock/64	1.0µs	1.95 kHz	488.28Hz	122.07Hz	30.52Hz	7.63Hz

13 Parallel ports

13.1 Introduction

The ST10F273E MCU provides up to 111 I/O lines with programmable features. These capabilities bring very flexible adaptation of this MCU to wide range of applications.

ST10F273E has nine groups of I/O lines gathered as follows:

- Port 0 is a two time 8-bit port named P0L (Low as less significant byte) and P0H (high as most significant byte)
- Port 1 is a two time 8-bit port named P1L and P1H
- Port 2 is a 16-bit port
- Port 3 is a 15-bit port (P3.14 line is not implemented)
- Port 4 is a 8-bit port
- Port 5 is a 16-bit port input only
- Port 6, Port 7 and Port 8 are 8-bit ports

These ports may be used as general purpose bidirectional input or output, software controlled with dedicated registers.

For example, the output drivers of six of the ports (2, 3, 4, 6, 7, 8) can be configured (bit-wise) for push-pull or open drain operation using ODPx registers.

The input threshold levels are programmable (TTL/CMOS) for all the ports. The logic level of a pin is clocked into the input latch once per state time, regardless whether the port is configured for input or output. The threshold is selected with PICON and XPICON registers control bits.

A write operation to a port pin configured as an input causes the value to be written into the port output latch, while a read operation returns the latched state of the pin itself. A read-modify-write operation reads the value of the pin, modifies it, and writes it back to the output latch.

Writing to a pin configured as an output (DPx.y=‘1’) causes the output latch and the pin to have the written value, since the output buffer is enabled. Reading this pin returns the value of the output latch. A read-modify-write operation reads the value of the output latch, modifies it, and writes it back to the output latch, thus also modifying the level at the pin.

I/O lines support an alternate function which is detailed in the following description of each port.

15 Serial channels

Serial communication with other microcontrollers, microprocessors, terminals or external peripheral components is provided by up to four serial interfaces: two asynchronous / synchronous serial channels (ASC0 and ASC1) and two high-speed synchronous serial channel (SSC0 and SSC1). Dedicated Baud rate generators set up all standard Baud rates without the requirement of oscillator tuning. For transmission, reception and erroneous reception, separate interrupt vectors are provided for ASC0 and SSC0 serial channel. A more complex mechanism of interrupt sources multiplexing is implemented for ASC1 and SSC1 (XBUS mapped).

15.1 Asynchronous / synchronous serial interfaces

The asynchronous / synchronous serial interfaces (ASC0 and ASC1) provides serial communication between the ST10F273E and other microcontrollers, microprocessors or external peripherals.

15.2 ASCx in asynchronous mode

In asynchronous mode, 8- or 9-bit data transfer, parity generation and the number of stop bits can be selected. Parity framing and overrun error detection is provided to increase the reliability of data transfers. Transmission and reception of data is double-buffered. Full-duplex communication up to 2M Bauds (at 64 MHz of f_{CPU}) is supported in this mode.

Table 41. ASC asynchronous baud rates by reload value and deviation errors (f_{CPU} = 40 MHz)

S0BRS = '0', f_{CPU} = 40 MHz			S0BRS = '1', f_{CPU} = 40 MHz		
Baud Rate (Baud)	**Deviation Error**	**Reload Value (hex)**	**Baud Rate (Baud)**	**Deviation Error**	**Reload Value (hex)**
1 250 000	0.0% / 0.0%	0000 / 0000	833 333	0.0% / 0.0%	0000 / 0000
112 000	+1.5% / -7.0%	000A / 000B	112 000	+6.3% / -7.0%	0006 / 0007
56 000	+1.5% / -3.0%	0015 / 0016	56 000	+6.3% / -0.8%	000D / 000E
38 400	+1.7% / -1.4%	001F / 0020	38 400	+3.3% / -1.4%	0014 / 0015
19 200	+0.2% / -1.4%	0040 / 0041	19 200	+0.9% / -1.4%	002A / 002B
9 600	+0.2% / -0.6%	0081 / 0082	9 600	+0.9% / -0.2%	0055 / 0056
4 800	+0.2% / -0.2%	0103 / 0104	4 800	+0.4% / -0.2%	00AC / 00AD
2 400	+0.2% / 0.0%	0207 / 0208	2 400	+0.1% / -0.2%	015A / 015B
1 200	0.1% / 0.0%	0410 / 0411	1 200	+0.1% / -0.1%	02B5 / 02B6
600	0.0% / 0.0%	0822 / 0823	600	+0.1% / 0.0%	056B / 056C
300	0.0% / 0.0%	1045 / 1046	300	0.0% / 0.0%	0AD8 / 0AD9
153	0.0% / 0.0%	1FE8 / 1FE9	102	0.0% / 0.0%	1FE8 / 1FE9

17 CAN modules

The two integrated CAN modules (CAN1 and CAN2) are identical and handle the completely autonomous transmission and reception of CAN frames according to the CAN specification V2.0 part B (active). It is based on the C-CAN specification.

Each on-chip CAN module can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers.

Because of duplication of the CAN controllers, the following adjustments are to be considered:

- Same internal register addresses of both CAN controllers, but with base addresses differing in address bit A8; separate chip select for each CAN module. Refer to *Chapter 4: Memory organization on page 22*.
- The CAN1 transmit line (CAN1_TxD) is the alternate function of the Port P4.6 pin and the receive line (CAN1_RxD) is the alternate function of the Port P4.5 pin.
- The CAN2 transmit line (CAN2_TxD) is the alternate function of the Port P4.7 pin and the receive line (CAN2_RxD) is the alternate function of the Port P4.4 pin.
- Interrupt request lines of the CAN1 and CAN2 modules are connected to the XBUS interrupt lines together with other X-Peripherals sharing the four vectors.
- The CAN modules must be selected with corresponding CANxEN bit of XPERCON register before the bit XPEN of SYSCON register is set.
- The reset default configuration is: CAN1 enabled, CAN2 disabled.

Note: If one or both CAN modules is used, Port 4 cannot be programmed to output all 8 segment address lines. Thus, only four segment address lines can be used, reducing the external memory space to 5 Mbytes (1 Mbyte per $\overline{CS}$ line).

17.1 Configuration support

It is possible that both CAN controllers are working on the same CAN bus, supporting together up to 64 message objects. In this configuration, both receive signals and both transmit signals are linked together when using the same CAN transceiver. This configuration is especially supported by providing open drain outputs for the CAN1_Txd and CAN2_TxD signals. The open drain function is controlled with the ODP4 register for port P4: in this way it is possible to connect together P4.4 with P4.5 (receive lines) and P4.6 with P4.7 (transmit lines configured to be configured as Open-Drain).

The user is also allowed to map internally both CAN modules on the same pins P4.5 and P4.6. In this way, P4.4 and P4.7 may be used either as general purpose I/O lines, or used for I^2C interface. This is possible by setting bit CANPAR of XMISC register. To access this register it is necessary to set bit XMISCEN of XPERCON register and bit XPEN of SYSCON register.

sufficient: anyway, a maximum of 100nF on V_{18} pin should not generate problems of over-current (higher value is allowed if current is limited by the external hardware). External current limitation is anyway recommended also to avoid risks of damage in case of temporary short between V_{18} and ground: the internal 1.8V drivers are sized to drive currents of several tens of Ampere, so the current shall be limited by the external hardware. The limit of current is imposed by power dissipation considerations (Refer to Electrical Characteristics Section).

In next Figures *15* and *16* Asynchronous Power-on timing diagrams are reported, respectively with boot from internal or external memory, highlighting the reset phase extension introduced by the embedded FLASH module when selected.

Note: Never power the device without keeping $\overline{RSTIN}$ pin grounded: the device could enter in unpredictable states, risking also permanent damages.

fact that it can degenerate into Long Reset: the two figures show the behavior when booting from internal or external memory respectively. Figures *21* and *22* reports the timing of a typical synchronous Long Reset, again when booting from internal or external memory.

Synchronous reset and RPD pin

Whenever the $\overline{\text{RSTIN}}$ pin is pulled low (by external hardware or as a consequence of a Bidirectional reset), the RPD internal weak pull-down is activated. The external capacitance (if any) on RPD pin is slowly discharged through the internal weak pull-down. If the voltage level on RPD pin reaches the input low threshold (around 2.5V), the reset event becomes immediately asynchronous. In case of hardware reset (short or long) the situation goes immediately to the one illustrated in *Figure 17*. There is no effect if RPD comes again above the input threshold: the asynchronous reset is completed coherently. To grant the normal completion of a synchronous reset, the value of the capacitance shall be big enough to maintain the voltage on RPD pin sufficient high along the duration of the internal reset sequence.

For a Software or Watchdog reset events, an active synchronous reset is completed regardless of the RPD status.

It is important to highlight that the signal that makes RPD status transparent under reset is the internal $\overline{\text{RSTF}}$ (after the noise filter).

or Watchdog Reset become a Short Hardware Reset. On the contrary, if $\overline{RSTF}$ remains low for less than 4 TCL, the device simply exits reset state.

The Bidirectional reset is not effective in case RPD is held low, when a Software or Watchdog reset event occurs. On the contrary, if a Software or Watchdog Bidirectional reset event is active and RPD becomes low, the $\overline{RSTIN}$ pin is immediately released, while the internal reset sequence is completed regardless of RPD status change (1024 TCL).

Note: The bidirectional reset function is disabled by any reset sequence (bit BDRSTEN of SYSCON is cleared). To be activated again it must be enabled during the initialization routine.

WDTCON flags

Similarly to what already highlighted in the previous section when discussing about Short reset and the degeneration into Long reset, similar situations may occur when Bidirectional reset is enabled. The presence of the internal filter on $\overline{RSTIN}$ pin introduces a delay: when $\overline{RSTIN}$ is released, the internal signal after the filter (see $\overline{RSTF}$ in the drawings) is delayed, so it remains still active (low) for a while. It means that depending on the internal clock speed, a short reset may be recognized as a long reset: the WDTCON flags are set accordingly.

Besides, when either Software or Watchdog bidirectional reset events occur, again when the $\overline{RSTIN}$ pin is released (at the end of the internal reset sequence), the $\overline{RSTF}$ internal signal (after the filter) remains low for a while, and depending on the clock frequency it is recognized high or low: 8TCL after the completion of the internal sequence, the level of $\overline{RSTF}$ signal is sampled, and if recognized still low a Hardware reset sequence starts, and WDTCON will flag this last event, masking the previous one (Software or Watchdog reset). Typically, a Short Hardware reset is recognized, unless the $\overline{RSTIN}$ pin (and consequently internal signal $\overline{RSTF}$) is sufficiently held low by the external hardware to inject a Long Hardware reset. After this occurrence, the initialization routine is not able to recognize a Software or Watchdog bidirectional reset event, since a different source is flagged inside WDTCON register. This phenomenon does not occur when internal FLASH is selected during reset ($\overline{EA}$ = 1), since the initialization of the FLASH itself extend the internal reset duration well beyond the filter delay.

Next Figures *25*, *26* and *27* summarize the timing for Software and Watchdog Timer Bidirectional reset events: In particular *Figure 27* shows the degeneration into Hardware reset.

In normal running mode (that is when main V_{DD} is on) the V_{STBY} pin can be tied to V_{SS} during reset to exercise the $\overline{EA}$ functionality associated with the same pin: the voltage supply for the circuitries which are usually biased with V_{STBY} (see in particular the 32 kHz oscillator used in conjunction with Real Time Clock module), is granted by the active main V_{DD}.

It must be noted that Stand-by mode can generate problems associated with the usage of different power supplies in CMOS systems; particular attention must be paid when the ST10F273E I/O lines are interfaced with other external CMOS integrated circuits: if V_{DD} of ST10F273E becomes (for example in Stand-by mode) lower than the output level forced by the I/O lines of these external integrated circuits, the ST10F273E could be directly powered through the inherent diode existing on ST10F273E output driver circuitry. The same is valid for ST10F273E interfaced to active/inactive communication buses during Stand-by mode: current injection can be generated through the inherent diode.
Furthermore, the sequence of turning on/off of the different voltage could be critical for the system (not only for the ST10F273E device). The device Stand-by mode current (I_{STBY}) may vary while V_{DD} to V_{STBY} (and vice versa) transition occurs: some current flows between V_{DD} and V_{STBY} pins. System noise on both V_{DD} and V_{STBY} can contribute to increase this phenomenon.

21.3.1 Entering stand-by mode

As already said, to enter Stand-by mode XRAM2EN bit in the XPERCON Register must be cleared: this allows to freeze immediately the RAM interface, avoiding any data corruption. As a consequence of a RESET event, the RAM Power Supply is switched to the internal low-voltage supply V_{18SB} (derived from V_{STBY} through the low-power voltage regulator). The RAM interface will remain frozen until the bit XRAM2EN is set again by software initialization routine (at next exit from main V_{DD} power-on reset sequence).

Since V_{18} is falling down (as a consequence of V_{DD} turning off), it can happen that the XRAM2EN bit is no longer able to guarantee its content (logic “0”), being the XPERCON Register powered by internal V_{18}. This does not generate any problem, because the Stand-by mode switching dedicated circuit continues to confirm the RAM interface freezing, irrespective the XRAM2EN bit content; XRAM2EN bit status is considered again when internal V_{18} comes back over internal stand-by reference V_{18SB}.

If internal V_{18} becomes lower than internal stand-by reference (V_{18SB}) of about 0.3 to 0.45V with bit XRAM2EN set, the RAM Supply switching circuit is not active: in case of a temporary drop on internal V_{18} voltage versus internal V_{18SB} during normal code execution, no spurious Stand-by mode switching can occur (the RAM is not frozen and can still be accessed).

The ST10F273E Core module, generating the RAM control signals, is powered by internal V_{18} supply; during turning off transient these control signals follow the V_{18}, while RAM is switched to V_{18SB} internal reference. It could happen that a high level of RAM write strobe from ST10F273E Core (active low signal) is low enough to be recognized as a logic “0” by the RAM interface (due to V_{18} lower than V_{18SB}): The bus status could contain a valid address for the RAM and an unwanted data corruption could occur. For this reason, an extra interface, powered by the switched supply, is used to prevent the RAM from this kind of potential corruption mechanism.

Table 53. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
DP0H **b**	F102h **E**	81h	P0h direction control register	- - 00h
DP1L **b**	F104h **E**	82h	P1L direction control register	- - 00h
DP1H **b**	F106h **E**	83h	P1h direction control register	- - 00h
DP2 **b**	FFC2h	E1h	Port 2 direction control register	0000h
DP3 **b**	FFC6h	E3h	Port 3 direction control register	0000h
DP4 **b**	FFCAh	E5h	Port 4 direction control register	- - 00h
DP6 **b**	FFCEh	E7h	Port 6 direction control register	- - 00h
DP7 **b**	FFD2h	E9h	Port 7 direction control register	- - 00h
DP8 **b**	FFD6h	EBh	Port 8 direction control register	- - 00h
DPP0	FE00h	00h	CPU data page pointer 0 register (10-bit)	0000h
DPP1	FE02h	01h	CPU data page pointer 1 register (10-bit)	0001h
DPP2	FE04h	02h	CPU data page pointer 2 register (10-bit)	0002h
DPP3	FE06h	03h	CPU data page pointer 3 register (10-bit)	0003h
EMUCON	FE0Ah	05h	Emulation control register	- - XXh
EXICON **b**	F1C0h **E**	E0h	External interrupt control register	0000h
EXISEL **b**	F1DAh **E**	EDh	External interrupt source selection register	0000h
IDCHIP	F07Ch **E**	3Eh	Device identifier register (n is the device revision)	114nh
IDMANUF	F07Eh **E**	3Fh	Manufacturer identifier register	0403h
IDMEM	F07Ah **E**	3Dh	On-chip memory identifier register	30D0h
IDPROG	F078h **E**	3Ch	Programming voltage identifier register	0040h
IDX0 **b**	FF08h	84h	MAC unit address pointer 0	0000h
IDX1 **b**	FF0Ah	85h	MAC unit address pointer 1	0000h
MAH	FE5Eh	2Fh	MAC unit accumulator - high word	0000h
MAL	FE5Ch	2Eh	MAC unit accumulator - low word	0000h
MCW **b**	FFDCh	EEh	MAC unit control word	0000h
MDC **b**	FF0Eh	87h	CPU multiply divide control register	0000h
MDH	FE0Ch	06h	CPU multiply divide register – high word	0000h
MDL	FE0Eh	07h	CPU multiply divide register – low word	0000h
MRW **b**	FFDAh	EDh	MAC unit repeat word	0000h
MSW **b**	FFDEh	EFh	MAC unit status word	0200h
ODP2 **b**	F1C2h **E**	E1h	Port 2 open drain control register	0000h
ODP3 **b**	F1C6h **E**	E3h	Port 3 open drain control register	0000h
ODP4 **b**	F1CAh **E**	E5h	Port 4 open drain control register	- - 00h
ODP6 **b**	F1CEh **E**	E7h	Port 6 open drain control register	- - 00h

Table 53. List of special function registers (continued)

Name	Physical address	8-bit address	Description	Reset value
XPERCON **b**	F024h **E**	12h	XPER configuration register	- - 05h
ZEROS **b**	FF1Ch	8Eh	Constant value 0's register (read only)	0000h

Note: 1. The system configuration is selected during reset. SYSCON reset value is 0000 0xx0 x000 0000b.

2. Reset Value depends on different triggered reset event.

3. The XPnIC Interrupt Control Registers control interrupt requests from integrated X-Bus peripherals. Some software controlled interrupt requests may be generated by setting the XPnIR bits (of XPnIC register) of the unused X-Peripheral nodes.

23.2 X-registers

The following table lists all X-Bus registers which are implemented in the ST10F273E ordered by their name. The FLASH control registers are listed in a separate section, in spite of they also are physically mapped on X-Bus memory space. Note that all X-Registers are not bit-addressable.

Table 54. List of XBus registers

Name	Physical address	Description	Reset value
CAN1BRPER	EF0Ch	CAN1: BRP extension register	0000h
CAN1BTR	EF06h	CAN1: Bit timing register	2301h
CAN1CR	EF00h	CAN1: CAN control register	0001h
CAN1EC	EF04h	CAN1: error counter	0000h
CAN1IF1A1	EF18h	CAN1: IF1 arbitration 1	0000h
CAN1IF1A2	EF1Ah	CAN1: IF1 arbitration 2	0000h
CAN1IF1CM	EF12h	CAN1: IF1 command mask	0000h
CAN1IF1CR	EF10h	CAN1: IF1 command request	0001h
CAN1IF1DA1	EF1Eh	CAN1: IF1 data A 1	0000h
CAN1IF1DA2	EF20h	CAN1: IF1 data A 2	0000h
CAN1IF1DB1	EF22h	CAN1: IF1 data B 1	0000h
CAN1IF1DB2	EF24h	CAN1: IF1 data B 2	0000h
CAN1IF1M1	EF14h	CAN1: IF1 mask 1	FFFFh
CAN1IF1M2	EF16h	CAN1: IF1 mask 2	FFFFh
CAN1IF1MC	EF1Ch	CAN1: IF1 message control	0000h
CAN1IF2A1	EF48h	CAN1: IF2 arbitration 1	0000h
CAN1IF2A2	EF4Ah	CAN1: IF2 arbitration 2	0000h
CAN1IF2CM	EF42h	CAN1: IF2 command mask	0000h

Table 54. List of XBus registers (continued)

Name	Physical address	Description	Reset value
CAN1IF2CR	EF40h	CAN1: IF2 command request	0001h
CAN1IF2DA1	EF4Eh	CAN1: IF2 data A 1	0000h
CAN1IF2DA2	EF50h	CAN1: IF2 data A 2	0000h
CAN1IF2DB1	EF52h	CAN1: IF2 data B 1	0000h
CAN1IF2DB2	EF54h	CAN1: IF2 data B 2	0000h
CAN1IF2M1	EF44h	CAN1: IF2 Mask 1	FFFFh
CAN1IF2M2	EF46h	CAN1: IF2 mask 2	FFFFh
CAN1IF2MC	EF4Ch	CAN1: IF2 message control	0000h
CAN1IP1	EFA0h	CAN1: interrupt pending 1	0000h
CAN1IP2	EFA2h	CAN1: interrupt pending 2	0000h
CAN1IR	EF08h	CAN1: interrupt register	0000h
CAN1MV1	EFB0h	CAN1: message valid 1	0000h
CAN1MV2	EFB2h	CAN1: message valid 2	0000h
CAN1ND1	EF90h	CAN1: new data 1	0000h
CAN1ND2	EF92h	CAN1: new data 2	0000h
CAN1SR	EF02h	CAN1: status register	0000h
CAN1TR	EF0Ah	CAN1: test register	00x0h
CAN1TR1	EF80h	CAN1: transmission request 1	0000h
CAN1TR2	EF82h	CAN1: transmission request 2	0000h
CAN2BRPER	EE0Ch	CAN2: BRP extension register	0000h
CAN2BTR	EE06h	CAN2: bit timing register	2301h
CAN2CR	EE00h	CAN2: CAN control register	0001h
CAN2EC	EE04h	CAN2: error counter	0000h
CAN2IF1A1	EE18h	CAN2: IF1 arbitration 1	0000h
CAN2IF1A2	EE1Ah	CAN2: IF1 arbitration 2	0000h
CAN2IF1CM	EE12h	CAN2: IF1 command mask	0000h
CAN2IF1CR	EE10h	CAN2: IF1 command request	0001h
CAN2IF1DA1	EE1Eh	CAN2: IF1 data A 1	0000h
CAN2IF1DA2	EE20h	CAN2: IF1 data A 2	0000h
CAN2IF1DB1	EE22h	CAN2: IF1 data B 1	0000h
CAN2IF1DB2	EE24h	CAN2: IF1 data B 2	0000h
CAN2IF1M1	EE14h	CAN2: IF1 mask 1	FFFFh
CAN2IF1M2	EE16h	CAN2: IF1 mask 2	FFFFh
CAN2IF1MC	EE1Ch	CAN2: IF1 message control	0000h

Table 64. DC characteristics (continued)

Symbol	Parameter	Test Condition	Limit Values		Unit
			Min.	Max.	
I_{PD2}	Power down supply current(11) (12) *(RTC on, main oscillator on, main voltage regulator off)*	T_A = 25°C	–	8	mA
I_{PD3}	Power down supply current (11) *(RTC on, 32 kHz oscillator on, main voltage regulator off)*	T_A = 25°C	–	1.1	mA
I_{SB1}	Stand-by supply current (13) *(RTC off, oscillators off, V_{DD} off, V_{STBY} on)*	V_{STBY} = 5.5 V $T_A = T_J$ = 25°C	–	250	µA
		V_{STBY} = 5.5 V $T_A = T_J$ = 125°C	–	500	µA
I_{SB2}	Stand-by supply current (13) *(RTC on, 32kHz oscillator on, main V_{DD} off, V_{STBY} on)*	V_{STBY} = 5.5 V T_A = 25°C	–	250	µA
		V_{STBY} = 5.5 V T_A = 125°C	–	500	µA
I_{SB3}	Stand-by supply current (13)(8) *(V_{DD} transient condition)*	–	–	2.5	mA

1. This specification is not valid for outputs which are switched to open drain mode. In this case the respective output will float and the voltage is imposed by the external circuitry.
2. Port 5 leakage values are granted for not selected A/D Converter channel. One channels is always selected (by default, after reset, P5.0 is selected). For the selected channel the leakage value is similar to that of other port pins.
3. Consult your vendor to know which version of the on-chip oscillator amplifier is enabled (Low-Power or Wide-Swing). The leakage of P2.0 is higher than other pins due to the additional logic (pass gates active only in specific test modes) implemented on input path. Pay attention to not stress P2.0 input pin with negative overload beyond the specified limits: failures in Flash reading may occur (sense amplifier perturbation). Refer to next *Figure 35* for a scheme of the input circuitry.
4. This specification is only valid during Reset, or during Hold- or Adapt-mode. Port 6 pins are only affected, if they are used for CS output and the open drain function is not enabled.
5. The maximum current may be drawn while the respective signal line remains inactive.
6. The minimum current must be drawn in order to drive the respective signal line active.
7. The power supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the Figure 36 below. This parameter is tested at V_{DDmax} and at maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}, RSTIN pin at V_{IH1min}: **this implies I/O current is not considered**. The device is doing the following:
   Fetching code from IRAM and XRAM1, accessing in read and write to both XRAM modules
   Watchdog Timer is enabled and regularly serviced
   RTC is running with main oscillator clock as reference, generating a tick interrupts every 192 clock cycles
   Four channel of XPWM are running (waves period: 2, 2.5, 3 and 4 CPU clock cycles): no output toggling
   Five General Purpose Timers are running in timer mode with prescaler equal to 8 (T2, T3, T4, T5, T6)
   ADC is in **Auto Scan Continuous Conversion mode** on all 16 channels of Port5
   All interrupts generated by XPWM, RTC, Timers and ADC are not serviced
8. Not 100% tested, guaranteed by design characterization.
9. The power supply current is a function of the operating frequency (f_{CPU} is expressed in MHz). This dependency is illustrated in the *Figure 36* below. This parameter is tested at V_{DDmax} and at maximum CPU clock frequency with all outputs disconnected and all inputs at V_{IL} or V_{IH}, RSTIN pin at V_{IH1min}: **this implies I/O current is not considered**. The device is doing the following:
   Fetching code from all sectors of IFlash, accessing in read (few fetches) and write to XRAM
   Watchdog Timer is enabled and regularly serviced
   RTC is running with main oscillator clock as reference, generating a tick interrupts every 192 clock cycles
   Four channel of XPWM are running (waves period: 2, 2.5, 3 and 4 CPU clock cycles): no output toggling
   Five General Purpose Timers are running in timer mode with prescaler equal to 8 (T2, T3, T4, T5, T6)
   ADC is in **Auto Scan Continuous Conversion mode** on all 16 channels of Port5
   All interrupts generated by XPWM, RTC, Timers and ADC are not serviced

24.8.5 Direct drive

When pins P0.15-13 (P0H.7-5) equal '011' during reset the on-chip phase locked loop is disabled, the on-chip oscillator amplifier is bypassed and the CPU clock is directly driven by the input clock signal on XTAL1 pin.

The frequency of CPU clock (f_{CPU}) directly follows the frequency of f_{XTAL} so the high and low time of f_{CPU} (i.e. the duration of an individual TCL) is defined by the duty cycle of the input clock f_{XTAL}.

Therefore, the timings given in this chapter refer to the minimum TCL. This minimum value can be calculated by the following formula:

$$TCL_{min} = 1/f_{XTAL} \times DC_{min}$$

DC= duty cycle

For two consecutive TCLs, the deviation caused by the duty cycle of f_{XTAL} is compensated, so the duration of 2TCL is always $1/f_{XTAL}$.

The minimum value TCL_{min} has to be used only once for timings that require an odd number of TCLs (1,3,...). Timings that require an even number of TCLs (2,4,...) may use the formula:

$$2TCL = 1/f_{XTAL}$$

The address float timings in Multiplexed bus mode (t_{11} and t_{45}) use the maximum duration of TCL ($TCL_{max} = 1/f_{XTAL} \times DC_{max}$) instead of $TCL_{Min.}$
Similarly to what happen for Prescaler Operation, if the bit OWDDIS in SYSCON register is cleared, the PLL runs on its free-running frequency and delivers the clock signal for the Oscillator Watchdog. If bit OWDDIS is set, then the PLL is switched off.

24.8.6 Oscillator watchdog (OWD)

An on-chip watchdog oscillator is implemented in the ST10F273E. This feature is used for safety operation with external crystal oscillator (available only when using direct drive mode with or without prescaler, so the PLL is not used to generate the CPU clock multiplying the frequency of the external crystal oscillator). This watchdog oscillator operates as following.

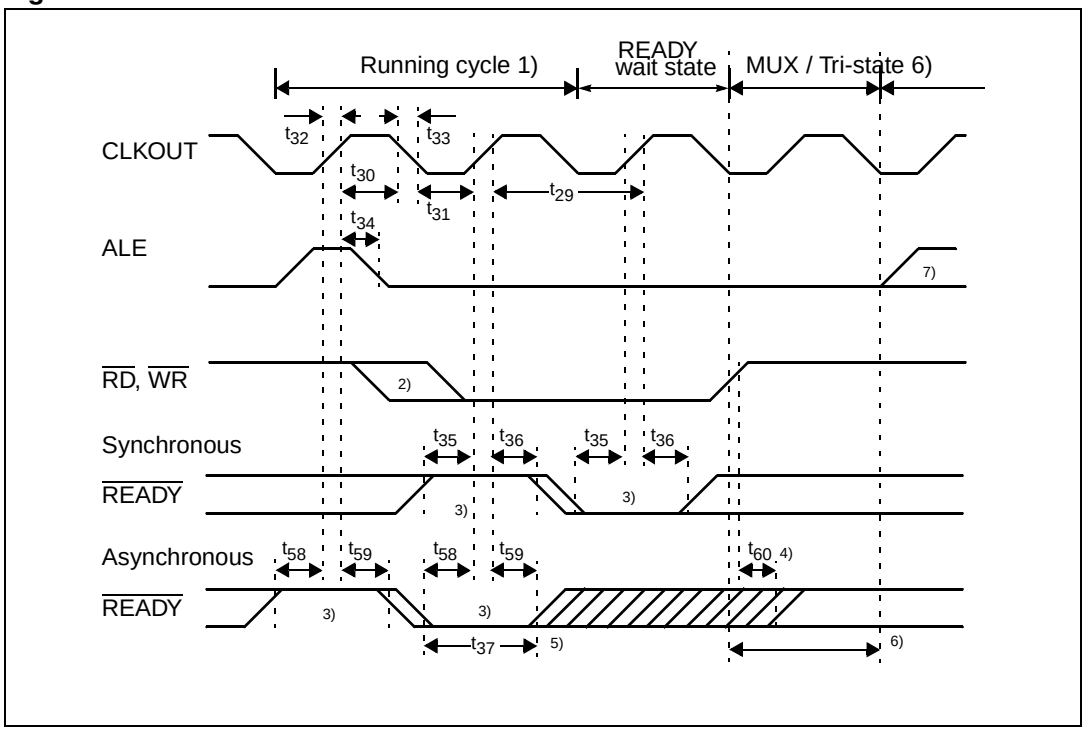
The reset default configuration enables the watchdog oscillator. It can be disabled by setting the OWDDIS (bit 4) of SYSCON register.

When the OWD is enabled, the PLL runs at its free-running frequency, and it increments the watchdog counter. On each transition of external clock, the watchdog counter is cleared. If an external clock failure occurs, then the watchdog counter overflows (after 16 PLL clock cycles).

The CPU clock signal will be switched to the PLL free-running clock signal, and the oscillator watchdog Interrupt Request is flagged. The CPU clock will not switch back to the external clock even if a valid external clock exits on XTAL1 pin. Only a hardware reset (or bidirectional Software / Watchdog reset) can switch the CPU clock source back to direct clock input.

When the OWD is disabled, the CPU clock is always the external oscillator clock (in Direct Drive or Prescaler Operation) and the PLL is switched off to decrease consumption supply current.

Figure 56. CLKOUT and $\overline{\text{READY}}$



1. Cycle as programmed, including MCTC wait states (Example shows 0 MCTC WS).
2. The leading edge of the respective command depends on RW-delay.
3. $\overline{\text{READY}}$ sampled HIGH at this sampling point generates a READY controlled wait state, $\overline{\text{READY}}$ sampled LOW at this sampling point terminates the currently running bus cycle.
4. $\overline{\text{READY}}$ may be deactivated in response to the trailing (rising) edge of the corresponding command ($\overline{\text{RD}}$ or $\overline{\text{WR}}$).
5. If the Asynchronous $\overline{\text{READY}}$ signal does not fulfill the indicated setup and hold times with respect to CLKOUT (e.g. because CLKOUT is not enabled), it must fulfill t_{37} in order to be safely synchronized. This is guaranteed, if READY is removed in response to the command (see Note 4).
6. Multiplexed bus modes have a MUX wait state added after a bus cycle, and an additional MTTC wait state may be inserted here.
   For a multiplexed bus with MTTC wait state this delay is two CLKOUT cycles, for a demultiplexed bus without MTTC wait state this delay is zero.
7. The next external bus cycle may start here.

26 Revision history

Table 83. Document revision history

Date	Revision	Changes
11-May-2006	1	Initial release.