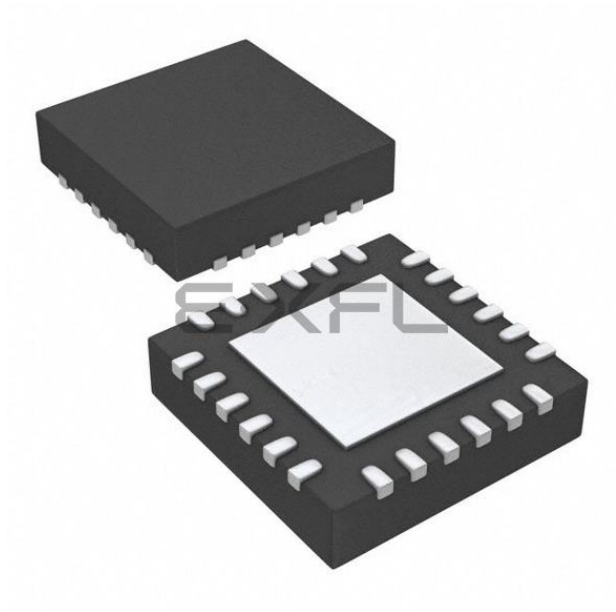


**Welcome to E-XFL.COM**

## What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

## Applications of "Embedded - Microcontrollers"

| Details | |
|---|---|
| Product Status | Active |
| Core Processor | ARM® Cortex®-M0+ |
| Core Size | 32-Bit Single-Core |
| Speed | 8MHz |
| Connectivity | I²C, SPI |
| Peripherals | Brown-out Detect/Reset, POR, PWM, WDT |
| Number of I/O | 12 |
| Program Memory Size | 32KB (32K x 8) |
| Program Memory Type | FLASH |
| EEPROM Size | 4K x 8 |
| RAM Size | 8K x 8 |
| Voltage - Supply (Vcc/Vdd) | 1.72V ~ 3.6V |
| Data Converters | - |
| Oscillator Type | Internal |
| Operating Temperature | -40°C ~ 85°C (TA) |
| Mounting Type | Surface Mount |
| Package / Case | 24-VFQFN Exposed Pad |
| Supplier Device Package | 24-HVQFN (4x4) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc8n04fhi24e |

## 2. Features and benefits

- System
  - ARM Cortex-M0+ processor running at frequencies of up to 8 MHz
  - ARM Cortex-M0+ built-in Nested Vectored Interrupt Controller (NVIC)
  - ARM Serial Wire Debug (SWD)
  - System tick timer
  - IC reset input
- Memory
  - 32 kB on-chip flash programming memory
  - 4 kB on-chip EEPROM of which 256 byte can be write protected
  - 8 kB SRAM
- Digital peripherals
  - Up to 12 General Purpose Input Output (GPIO) pins with configurable pull-up/pull-down resistors and repeater mode
  - GPIO pins which can be used as edge and level sensitive interrupt sources
  - High-current drivers/sinks (20 mA) on four GPIO pins
  - High-current drivers/sinks (20 mA) on two $I^2C$-bus pins
  - Programmable WatchDog Timer (WDT)
- Analog peripherals
  - Temperature sensor with $\pm 1.5$ °C absolute temperature accuracy between −40 °C and +85 °C
- Communication interfaces
  - NFC/RFID ISO 14443 type A interface
  - $I^2C$-bus interface supporting full $I^2C$-bus specification and fast mode with a data rate of 400 kbit/s, with multiple address recognition and monitor mode
- Energy harvesting functionality to power the LPC8N04.
- OTA firmware update using Secondary Bootloader (SBL) library (See TN00040: LPC8N04: Encrypted Over the Air (OTA) Firmware update using NFC). OTA firmware update available on Boot ROM version 0.14.
- Clock generation
  - 8 MHz internal RC oscillator, trimmed to 2 % accuracy, which is used for the system clock
  - Timer oscillator operating at 32 kHz linked to the RTC timer unit
- Power control
  - Support for 1.72 V to 3.6 V external voltages
  - The LPC8N04 can also be powered from the NFC field
  - Activation via NFC possible
  - Integrated Power Management Unit (PMU) for versatile control of power consumption
  - Four reduced power modes for ARM Cortex-M0+: sleep, deep sleep, deep power-down and battery off
  - Power gating for each analog peripheral for ultra-low power operation
  - < 50 nA IC current consumption in battery off mode at 3.0 V
  - Power-On Reset (POR)

- Unique device serial number for identification

## 3. Applications

- Configurable LED strip/christmas tree LEDs via NFC
- Smart toy/interactive robot data logger
- Buttonless/contactless control panel
- Contactless diagnostic
- NFC e-locker
- Smart manufacturing
- NFC OTA

## 4. Ordering information

**Table 1. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| LPC8N04FHI24 | HVQFN24 | plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 × 4 × 0.85 mm | SOT616-3 |

## 5. Marking

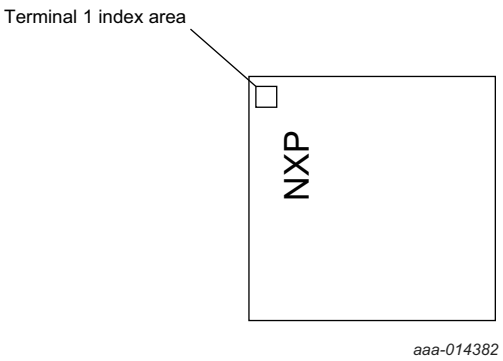



**Fig 1. HVQFN24 package marking**

The LPC8N04 HVQFN24 package has the following top-side marking:

- First line: Syww
  - yww: Date code with y = year and ww = week.
- Second line: xxxx
- Third line: LPC8N04

# 7. Pinning information

## 7.1 Pinning

### 7.1.1 HVQFN24 package

Figure 3 shows the pad layout of the LPC8N04 in the HVQFN24 package.

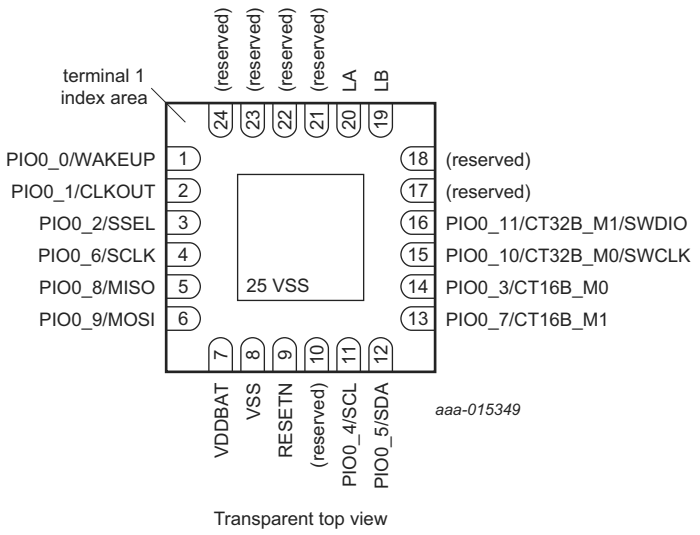



**Fig 3. Pad configuration HVQFN24**

**Table 2. Pad allocation table of the HVQFN24 package**

| Pad | Symbol | Pad | Symbol |
|---|---|---|---|
| 1 | PIO0_0/WAKEUP | 13[1] | PIO0_7/CT16B_M1 |
| 2 | PIO0_1/CLKOUT | 14[1] | PIO0_3/CT16B_M0 |
| 3 | PIO0_2/SSEL | 15[1] | PIO0_10/CT32B_M0/SWCLK |
| 4 | PIO0_6/SCLK | 16[1] | PIO0_11/CT32B_M1/SWDIO |
| 5 | PIO0_8/MISO | 17[2] | RESERVED |
| 6 | PIO0_9/MOSI | 18[2] | RESERVED |
| 7 | VDDBAT | 19 | LB |
| 8 | VSS | 20 | LA |
| 9 | RESETN | 21[2] | RESERVED |
| 10 | RESERVED | 22[2] | RESERVED |
| 11 | PIO0_4/SCL | 23[2] | RESERVED |
| 12 | PIO0_5/SDA | 24[2] | RESERVED |

[1] High source current pads; see Section 8.6.3.

[2] These pads must be tied to ground.

**Table 3. Pad description of the HVQFN24 package**

| Pad | Symbol | Type | Description |
|---|---|---|---|
| **Supply** | | | |
| 7 | VDDBAT | supply | positive supply voltage |
| 8 | VSS | supply | ground |
| **GPIO[1]** | | | |
| 1 | PIO0_0 | I/O | GPIO |
| | WAKEUP | I | deep power-down mode wake-up pin[2] |
| 2 | PIO0_1 | I/O | GPIO |
| | CLKOUT | O | clock output |
| 3 | PIO0_2 | I/O | GPIO |
| | SSEL | I | SPI/SSP serial select line |
| 14 | PIO0_3 | I/O | GPIO |
| | CT16B_M0 | O | 16-bit timer match output 0 |
| 11 | PIO0_4 | I/O | GPIO |
| | SCL | I/O | $I^2C$-bus SCL clock line |
| 12 | PIO0_5 | I/O | GPIO |
| | SDA | I/O | $I^2C$-bus SDA data line |
| 4 | PIO0_6 | I/O | GPIO |
| | SCLK | I/O | SPI/SSP serial clock line |
| 13 | PIO0_7 | I/O | GPIO |
| | CT16B_M1 | O | 16-bit timer match output 1 |
| 5 | PIO0_8 | I/O | GPIO |
| | MISO | O | SPI/SSP master-in slave-out line |
| 6 | PIO0_9 | I/O | GPIO |
| | MOSI | I | SPI/SSP master-out slave-in line |
| 15 | PIO0_10 | I/O | GPIO |
| | CT32B_M0 | O | 32-bit timer match output 0 |
| | SWCLK | I | ARM SWD clock |
| 16 | PIO0_11 | I/O | GPIO |
| | CT32B_M1 | O | 32-bit timer match output 1 |
| | SWDIO | I/O | ARM SWD I/O |
| **Radio** | | | |
| 20 | LA | A | NFC antenna/coil terminal A |
| 19 | LB | A | NFC antenna/coil terminal B |
| **Reset** | | | |
| 9 | RESETN | I | external reset input[3] |

[1] The GPIO port is a 12-bit I/O port with individual direction and function controls for each bit. The operation of port 0 pads depends on the function selected through the IOCONFIG register block.

[2] If external wake-up is enabled on this pad, it must be pulled HIGH before entering deep power-down mode and pulled LOW for a minimum of 100 μs to exit deep power-down mode.

[3] A LOW on this pad resets the device. This reset causes I/O ports and peripherals to take on their default states, and processor execution to begin at address 0. It has weak pull-up to $V_{DDBAT}$.

# 8. Functional description

## 8.1 ARM Cortex-M0+ core

Refer to the *Cortex-M0+ Devices Technical Reference Manual* (Ref. 1) for a detailed description of the ARM Cortex-M0+ processor.

The LPC8N04 ARM Cortex-M0+ core has the following configuration:

- System options
  - Nested Vectored Interrupt Controller (NVIC)
  - Fast (single-cycle) multiplier
  - System tick timer
  - Support for wake-up interrupt controller
  - Vector table remapping register
  - Reset of all registers
- Debug options
  - Serial Wire Debug (SWD) with two watchpoint comparators and four breakpoint comparators
  - Halting debug is supported

## 8.2 Memory map

Figure 4 shows the memory and peripheral address space of the LPC8N04.

The only AHB peripheral device on the LPC8N04 is the GPIO module. The APB peripheral area is 512 kB in size. Each peripheral is allocated 16 kB of space.

All peripheral register addresses are 32-bit word aligned. Byte and half-word addressing is not possible. All reading and writing are done per full word.

## 8.4 Power management

The Power Management Unit (PMU) controls the switching between available power sources and the powering of the different voltage domains in the IC.

### 8.4.1 System power architecture

The LPC8N04 accepts power from two different sources: from the external power supply pin VDDBAT, or from the built-in NFC/RFID rectifier.

The LPC8N04 has a small automatic source selector that monitors the power inputs (VBAT and VNFC, see Figure 6) as well as pin RESETN. The PSWBAT switch is kept open until a trigger is given on pin RESETN or via the NFC field. If the trigger is given, the always-on domain, VDD_ALON, itself is powered via the PSWBAT or the PSWNFC switch: via VBAT, if VBAT > 1.72 V, or VNFC. Priority is given to VBAT when both VBAT and VNFC are present.

The automatic source selector unit in the PMU decides on the powering of the internal domains based on the power source.

- If a voltage > 1.72 V is detected on VBAT and not VNFC, VBAT powers the internal domains after a trigger on pin RESETN or via NFC.
- If a voltage ≤ 1.72 V is detected on VBAT, and a higher voltage is detected on VNFC, the internal domains are powered from VNFC.
- If a voltage > 1.72 V is detected at both VBAT and VNFC, the internal domains are powered from VBAT.
- Switch over between power sources is possible. If initially both VBAT and VNFC are available, the system is powered from VBAT. If VBAT then becomes unavailable (because it is switched off externally, or by a PSWBAT/PSWNFC power switch override), the internal domains are immediately powered from VNFC. Switch over is supported in both directions.
- The user can force the selection of the VBAT input by disabling the automatic power switch, which disables the automatic source selector voltage comparator.

When on NFC power only (passive operation), connecting one or more 100 nF external capacitors in parallel to a GPIO pad, and setting that pad as an output driven to logic 1, is advised. Preferably a high-drive pin should be chosen and several pins can be connected in parallel.

PSWNFC and PSWBAT are the power switches. PSWNFC connects power to the VDD_ALON power net when an RF field is present. PSWBAT connects power from the battery when a positive edge is detected on RESETN. If no RF power is available, the PMU can open this PSWBAT switch, effectively switching off the device. After connecting VDDBAT to a power source, the PSWBAT switch is open until a rising edge is detected on RESETN or RF power is applied.

Each component of the LPC8N04 resides in one of several internal power domains, as indicated in Figure 6. The domains are VBAT, VNFC, VDD_ALON, VDD1V2 and VDD1V6. The domains VDD_ALON, VDD1V2 and VDD1V6 are powered, or not, depending on the mode of the LPC8N04. There are five modes: active, sleep, deep sleep, deep power-down and battery off.

The VDD_ALON domain contains BrownOut Detection (BOD). When enabled, if the VDD_ALON voltage drops below 1.8 V it raises a BOD interrupt.

The PMU controls the active, sleep, deep sleep and deep power-down modes, and thus the power flow to the different internal components.

The PMU has two LDOs powering the internal VDD1V2 and VDD1V6 voltage domains. LDO1V2 converts voltages in the range 1.72 V to 3.6 V into 1.22 V. LDO1V6 converts voltages in the range 1.72 V to 3.6 V into 1.6 V. Each LDO can be enabled separately. A 1.2 nF buffer capacitor is included at the input of the LDOs when powered via VNFC.

The trigger detector (not shown in Figure 6) and power gate have a leakage of less than 50 nA to allow for long shelf life before activation.

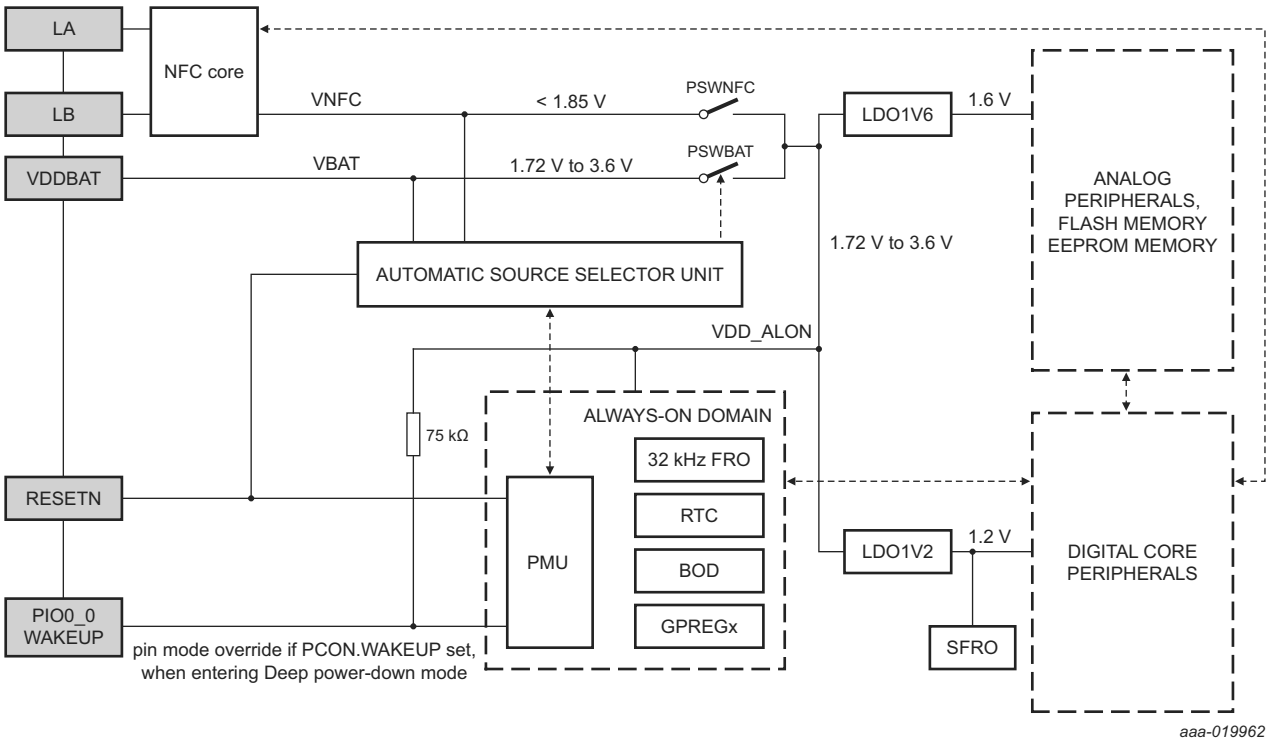



**Fig 6. LPC8N04 power architecture**

The PMU states and settings of the LDOs are summarized in Table 4, and the state transitions are shown in Figure 7.

Table 5 and Table 6 summarize the events that can influence wake-up from deep power-down or deep sleep modes (DEEPPDN or DEEPSLEEP to ACTIVE state transition).

**Table 5. State transition events for DEEPSLEEP to ACTIVE**

| Event | Description |
|---|---|
| RESETN | reset asserted |
| RTC event | if the timer reaches preset value |
| Watchdog | watchdog issues interrupt or reset |
| WAKEUP | signal on WAKEUP pin |
| RF field | RF field is detected, potential NFC command input (if set in PMU) |
| Start logic interrupt | one of the enabled start logic interrupts is asserted |

**Table 6. State transition events for DEEPPDN to ACTIVE**

| Event | Description |
|---|---|
| RESETN | reset asserted |
| RTC event | if the timer reaches preset value |
| WAKEUP | signal on WAKEUP pin (when enabled) |
| RF field | RF field is detected, potential NFC command input (if set in PMU) |

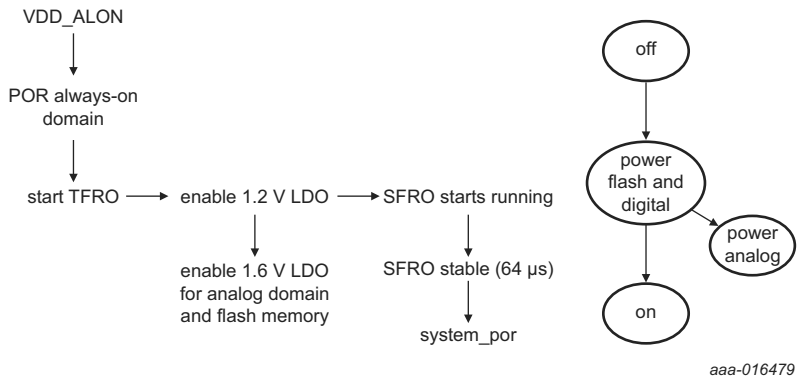



**Fig 8. LPC8N04 power-up sequence**

#### 8.4.1.1 Applying power to the PCB/system with battery for the first time

To support long shelf life without draining the battery, the LPC8N04 is not connected to an external supply pin until RESET pin is asserted and de-asserted or the NFC field is present. Once the RESET or the NFC field is applied, the LPC8N04 is powered.

### 8.4.2 Power Management Unit (PMU)

The Power Management Unit (PMU) partly resides in the digital power domain and partly in the always-on domain. The PMU controls the sleep, deep sleep and deep power-down modes and the power flow to the different internal circuit blocks. Five general-purpose registers in the PMU can be used to retain data during deep power-down mode. These registers are located in the always-on domain. The PMU also raises a BOD interrupt, if necessary, if VDD_ALON drops below 1.8 V.

The power to the different APB analog slaves is controlled through a power-down configuration register.

The power control register selects whether an ARM Cortex-M0+ controlled power-down mode (sleep mode or deep sleep mode) or the deep power-down mode is entered. It also provides the flags for sleep or deep-sleep modes and deep power-down mode respectively. In addition, it contains the overrides for the power source selection.

## 8.5 Nested Vectored Interrupt Controller (NVIC)

The Nested Vectored Interrupt Controller (NVIC) is a part of the ARM Cortex-M0+. The tight integration of the processor core and NVIC enables fast processing of interrupts, dramatically reducing the interrupt latency.

### 8.5.1 Features

- NVIC that is a part of the ARM Cortex-M0+
- Tightly coupled interrupt controller provides low interrupt latency
- Controls system exceptions and peripheral interrupts
- Four programmable interrupt priority levels with hardware priority level masking
- Software interrupt generation

### 8.5.2 Interrupt sources

Table 7 lists the interrupt sources for each peripheral function. Each peripheral device may have one or more interrupt lines to the NVIC. Each line may represent more than one interrupt source. There is no significance or priority about which line is connected where, except for certain standards from ARM.

**Table 7. Connection of interrupt source to the NVIC**

| Exception number | Vector offset | Function | Flags |
|---|---|---|---|
| 0 to 12 | - | start logic wake-up interrupts | each interrupt connected to a PIO0 input pin serves as wake-up from deep-sleep mode[1] |
| 13 | - | RFID/NFC | RFID/NFC access detected/command received/read acknowledge |
| 14 | - | RTC on/off timer | RTC on/off timer event interrupt |
| 15 | - | $I^2C$-bus | Slave Input (SI) (state change) |
| 16 | - | CT16B | 16-bit timer |
| 17 | - | PMU | power from NFC field detected |
| 18 | - | CT32B | 32-bit timer |
| 19 | - | BOD | brownout detection (power drop) |
| 20 | - | SPI/SSP | TX FIFO half empty/RX FIFO half full/ RX time-out/RX overrun |
| 21 | - | TSENS | temperature sensor end of conversion/low threshold/ high threshold |
| 22 to 25 | - | - | RESERVED |
| 26 | - | WDT | watchdog interrupt (WDINT) |
| 27 | - | flash | flash memory |
| 28 | - | EEPROM | EEPROM memory |
| 29 to 30 | - | - | RESERVED |
| 31 | - | PIO0 | GPIO interrupt status of port 0 |

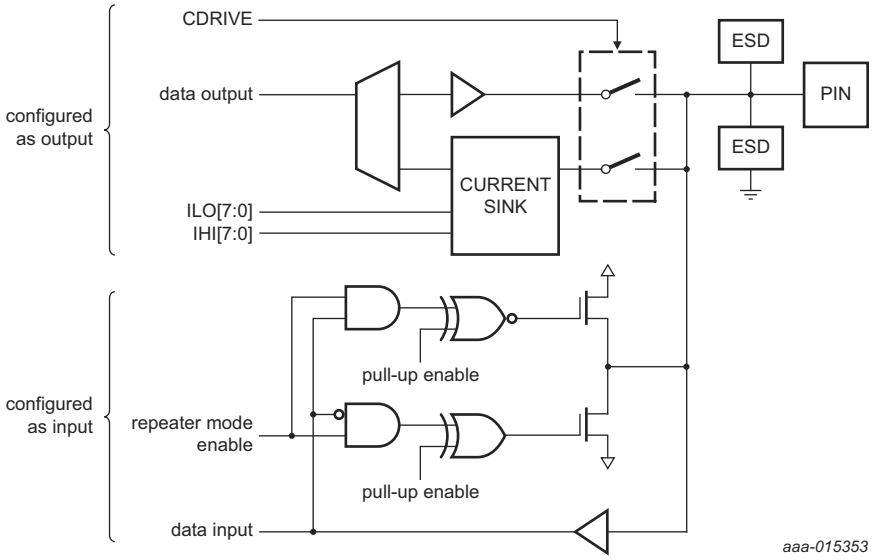



**Fig 9. Pin configuration with current source mode**

## 8.7 Fast general-purpose parallel I/O

The GPIO registers control device pins that are not connected to a specific peripheral function. Pins may be dynamically configured as inputs or outputs. Multiple outputs can be set or cleared in one write operation.

LPC8N04 uses accelerated GPIO functions:

- GPIO registers are on the ARM Cortex-M0+ I/O bus for fastest possible single-cycle I/O timing
- An entire port value can be written in one instruction
- Mask, set, and clear operations are supported for the entire port

All GPIO port pins are fixed-pin functions that are enabled or disabled on the pins by the switch matrix. Therefore each GPIO port pin is assigned to one specific pin and cannot be moved to another pin.

### 8.7.1 Features

- Bit level port registers allow a single instruction to set and clear any number of bits in one write operation
- Direction control of individual bits
- After reset, all I/Os default to GPIO inputs without pull-up or pull-down resistors. The $I^2C$-bus true open-drain pins PIO0_4 and PIO0_5 and the SWD pins PIO0_10 and PIO0_11 are exceptions
- Pull-up/pull-down configuration, repeater, and open-drain modes can be programmed through the IOCON block for each GPIO pin
- Direction (input/output) can be set and cleared individually
- Pin direction bits can be toggled

The CMDIN, DATAOUT, Status Register (SR) and SRAM are mapped in the user memory space of the RFID core. The RFID READ and WRITE commands allow wireless communication to this shared memory.

Messages can be in raw mode (user proprietary protocol) or formatted according to NFC forum type 2 NDEF messaging and ISO/IEC 11073.

## 8.11 16-bit timer

### 8.11.1 Features

One 16-bit timer with a programmable 16-bit prescaler.

- Timer operation
- Four 16-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match
  - Stop timer on match with optional interrupt generation
  - Reset timer on match with optional interrupt generation
- Up to two CT16B external outputs corresponding to the match registers with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Up to two match registers can be configured as Pulse Width Modulation (PWM) allowing the use of up to two match outputs as single edge controlled PWM outputs

### 8.11.2 General description

The peripheral clock (PCLK), which is derived from the system clock, clocks the timer. The timer can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock.

Each timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, four match registers can be used to provide a single-edge controlled PWM output on the match output pins. The use of the match registers that are not pinned out to control the PWM cycle length is recommended.

## 8.12 32-bit timer

### 8.12.1 Features

One 32-bit timer with a programmable 32-bit prescaler.

- Timer operation
- Four 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match

- Stop timer on match with optional interrupt generation
- Reset timer on match with optional interrupt generation

- Up to two CT32B external outputs corresponding to the match registers with the following capabilities:
  - Set LOW on match
  - Set HIGH on match
  - Toggle on match
  - Do nothing on match
- Up to two match registers can be configured as PWM allowing the use of up to two match outputs as single edge controlled PWM outputs

### 8.12.2 General description

The peripheral clock (PCLK), which is derived from the system clock, clocks the timer. The timer can optionally generate interrupts or perform other actions at specified timer values based on four match registers. The peripheral clock is provided by the system clock.

Each timer also includes one capture input to trap the timer value when an input signal transitions, optionally generating an interrupt.

In PWM mode, four match registers can be used to provide a single-edge controlled PWM output on the match output pins. Use of the match registers that are not pinned out to control the PWM cycle length is recommended.

## 8.13 WatchDog Timer (WDT)

If the microcontroller enters an erroneous state, the purpose of the WatchDog Timer (WDT) is to reset it within a reasonable amount of time.

When enabled, if the user program fails to feed (or reload) the WDT within a predetermined amount of time, the WDT generates a system reset.

### 8.13.1 Features

- If not periodically reloaded, it internally resets the microcontroller
- Debug mode
- Enabled by software but requires a hardware reset or a WDT reset/interrupt to be disabled
- If enabled, incorrect/incomplete feed sequence causes reset/interrupt
- Flag to indicate WDT reset
- Programmable 24-bit timer with internal prescaler
- Selectable time period from (TWDCLK $\times$ 256 $\times$ 4) to (TWDCLK $\times$ $2^{24}$ $\times$ 4) in multiples of TWDCLK $\times$ 4
- The WDT clock (WDCLK) source is a 2 MHz clock derived from the SFRO, or the external clock as set by the SYSCLKCTRL register

### 8.18.3 Erasing/programming flash

Erasing and programming are separate operations. Both are possible only on memory sectors that are unprotected and unlocked. Protect/lock information is stored inside the memory itself, so the controller is not aware of protection status. Therefore, if a program/erase operation is performed on a protected or locked sector, it does not flag an error.

**Protection —** At exit from reset, all sectors are protected against accidental modification. To allow modification, a sector must be unprotected. It can then be protected again after that the modification is performed.

**Locking —** Each flash sector has a lock bit. Lock bits can be set but cannot be cleared. Locked sectors cannot be erased and reprogrammed.

## 8.19 On-chip SRAM

The LPC8N04 contains a total of 8 kB on-chip SRAM memory configured as $256 \times 2 \times 4 \times 32$ bit.

## 8.20 On-chip EEPROM

The LPC8N04 contains a 4 kB EEPROM. This EEPROM is organized in 64 rows of $32 \times 16$-bit words. Of these rows, the last four contain calibration and test data and are locked. This data is either used by the bootloader after reset, or made accessible to the application via firmware Application Programming Interface (API).

### 8.20.1 Reading from EEPROM

Reading is done via the AHB interface. The memory is mapped on the bus address space, as a contiguous address space. Memory data words are seen on the bus using a little endian arrangement.

### 8.20.2 Writing to EEPROM

Erasing and programming is performed, as a single operation, on one or more words inside a single page.

Previous write operations have transferred the data to be programmed into the memory page buffer. The page buffer tracks which words were written to (offset within the page only). Words not written to, retain their previous content.

# 9. Limiting values

**Table 10. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | supply voltage | | –0.5 | +3.6 | V |
| $V_I$ | input voltage | normal PIO pads ($V_{DD}$ = 0.6 V) | –0.5 | +3.6 | V |
| | | high-source PIO pads | –0.5 | +5.5 | V |
| | | LA/LB pads | –0.5 | +5.5 | V |
| $I_{DD}$ | supply current | per supply pin | - | 100 | mA |
| $I_{SS}$ | ground supply current | per supply pin | - | 100 | mA |
| $I_{lu}$ | latch-up current | I/O; $-0.5V_{DD} < V_I < +1.5V_{DD}$; $T_j < 125$ °C | - | 100 | mA |
| $T_{stg}$ | storage temperature | | –40 | +125 | °C |
| $T_j$ | junction temperature | | - | 125 | °C |
| $P_{tot}$ | total power dissipation | | - | 1 | W |
| $V_{ESD}$ | electrostatic discharge voltage | human body model; all pins | –2000 | +2000 | V |
| | | charged device model; all pins | –500 | +500 | V |

# 10. Static characteristics

**Table 11. Static characteristics**

*$T_{amb}$ = −40 °C to +85 °C, unless otherwise stated.*

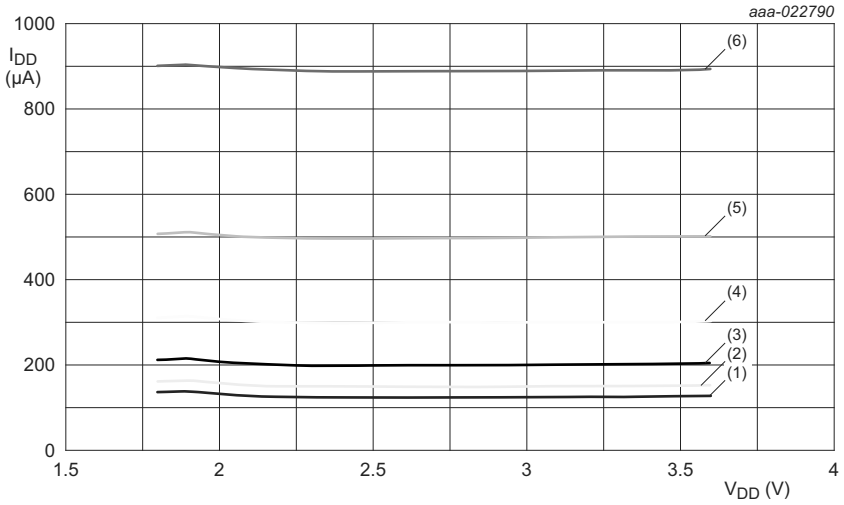
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **Supply pins** | | | | | | |
| $V_{DD}$ | supply voltage | | 1.72 | 3.0 | 3.60 | V |
| $I_{DD}$ | supply current | voltage and clock frequency dependent [1] | - | - | - | μA |
| $I_{L(off)}$ | off-state leakage current | | - | - | 50 | nA |
| $I_{DD(pd)}$ | power-down mode supply current | deep power-down mode | - | 3 | - | μA |
| **Standard GPIO pins** | | | | | | |
| $V_{IH}$ | HIGH-level input voltage | | 0.7 × $V_{DD}$ | - | - | V |
| $V_{IL}$ | LOW-level input voltage | | - | - | 0.3 × $V_{DD}$ | V |
| $V_{hys}$ | hysteresis voltage | | 0.4 | - | - | V |
| $R_{pd}$ | pull-down resistance | | - | 72 | - | kΩ |
| $R_{pu}$ | pull-up resistance | | - | 73 | - | kΩ |
| $I_S$ | source current | HIGH-level $V_{DD}$ = 1.8 V [2] | - | 2 | - | mA |
| | | HIGH-level $V_{DD}$ = 3.6 V [2] | - | 8 | - | mA |
| | | LOW-level $V_{DD}$ = 1.8 V [2] | - | 4 | - | mA |
| | | LOW-level $V_{DD}$ = 3.6 V [2] | - | 16 | - | mA |
| **High-drive GPIO pins** | | | | | | |
| $I_S$ | source current | HIGH-level $V_{DD}$ = 1.8 V [3] | 4 | - | 6 | mA |
| | | HIGH-level $V_{DD}$ = 3.6 V [3] | 13 | - | 18 | mA |
| | | LOW-level $V_{DD}$ = 1.8 V [3] | 5.5 | - | 8 | mA |
| | | LOW-level $V_{DD}$ = 3.6 V [3] | 22 | - | 32 | mA |
| **$I^2C$-bus pins** | | | | | | |
| $I_S$ | source current | LOW-level $V_{DD}$ = 1.8 V [4] | 2 | - | 8.5 | mA |
| | | LOW-level $V_{DD}$ = 3.6 V [4] | 9.5 | - | 38 | mA |
| **Brownout detect** | | | | | | |
| $V_{trip(bo)}$ | brownout trip voltage | falling $V_{DD}$ | - | 1.8 | - | V |
| | | rising $V_{DD}$ | - | 1.875 | - | V |
| $V_{hys}$ | hysteresis voltage | | - | 75 | - | mV |
| **General** | | | | | | |
| $R_{pu(int)}$ | internal pull-up resistance | on pin RESETN | - | 100 | - | kΩ |
| $C_{ext}$ | external capacitance | on pin RESETN | - | - | 1 | nF |

[1] See Figure 11.

[2] PIO0_0, PIO0_1, PIO0_2, PIO0_6, PIO0_8, PIO0_9.

[3] PIO0_3, PIO0_7, PIO0_10, PIO0_11.

[4] PIO0_4, PIO0_5.




Plot of $I_{DD}$ / $V_{DD}$ when ARM running a while-1 loop in normal mode, no NFC field present.

(1) System clock = 250 kHz
(2) System clock = 500 kHz
(3) System clock = 1 MHz
(4) System clock = 2 MHz
(5) System clock = 4 MHz
(6) System clock = 8 MHz

**Fig 11. Active current consumption**

**Table 12. Temperature sensor characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{CC(pd)}$ | power-down mode supply current | TSENS disabled | - | - | 1 | nA |
| $I_{stb}$ | standby current | TSENS enabled | - | 6 | 7 | μA |
| $I_{CC(oper)}$ | operating supply current | TSENS converting | - | 10 | 12 | μA |
| $T_{acc}$ | temperature accuracy | | −1.5 | - | +1.5 | °C |

**Note:** The absolute accuracy is valid for the factory calibration of the temperature sensor. The sensor can be user-calibrated to reach higher accuracy.

**Table 13. Antenna input characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $C_i$ | input capacitance | [1] | - | 50 | - | pF |
| $f_i$ | input frequency | | - | 13.56 | - | MHz |

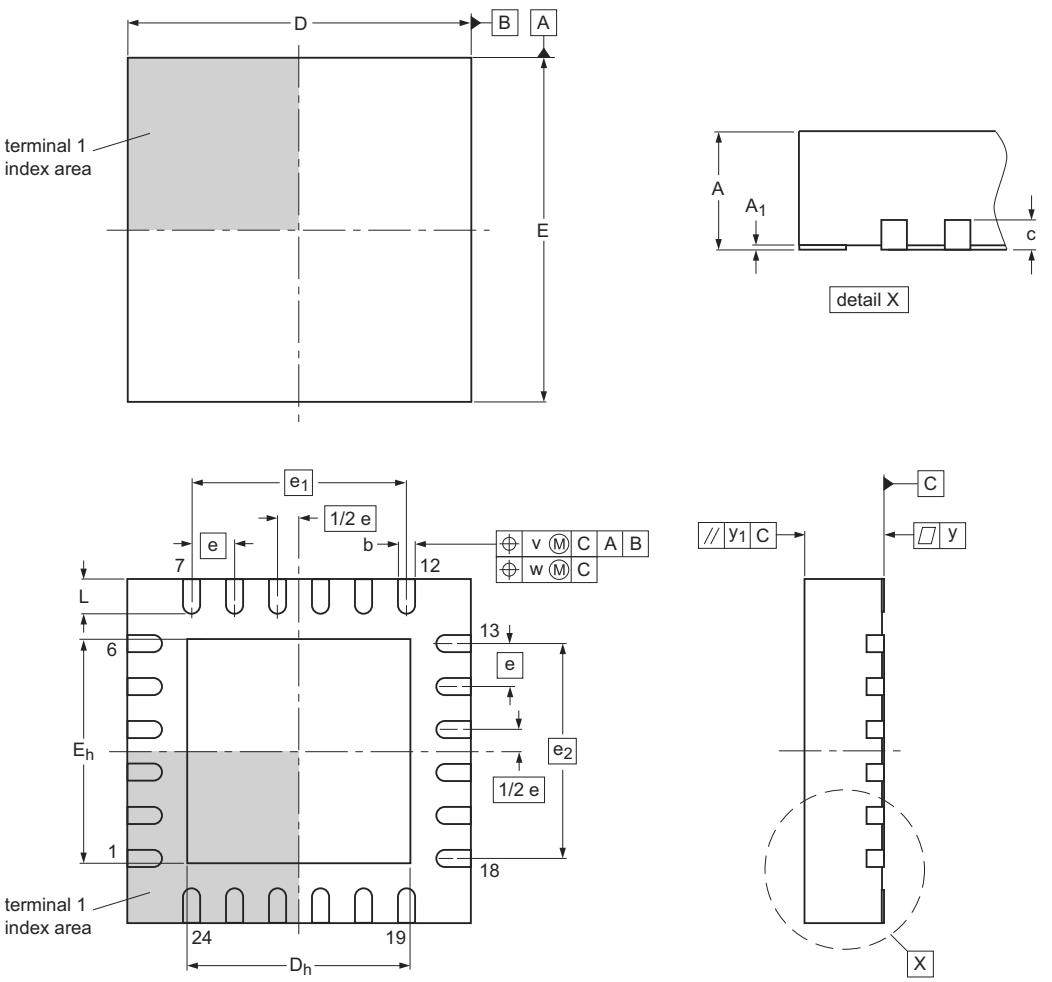
[1] $T_{amb}$ = 22 °C, f = 13.56 MHz, RMS voltage between LA and LB = 1.5 V.

**Table 14. EEPROM characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_{ret(data)}$ | data retention time | $T_{amb}$ = 22 °C | 10 | - | - | year |

# 12. Package outline

**HVQFN24: plastic thermal enhanced very thin quad flat package; no leads; 24 terminals; body 4 x 4 x 0.85 mm** **SOT616-3**




Dimensions (mm are the original dimensions)

| Unit(1) | | A(1) | $A_1$ | b | c | D(1) | $D_h$ | E(1) | $E_h$ | e | $e_1$ | $e_2$ | L | v | w | y | $y_1$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | max | 1 | 0.05 | 0.30 | | 4.1 | 2.75 | 4.1 | 2.75 | | | | 0.5 | | | | |
| | nom | | | | 0.2 | | | | | 0.5 | 2.5 | 2.5 | | 0.1 | 0.05 | 0.05 | 0.1 |
| | min | | 0.00 | 0.18 | | 3.9 | 2.45 | 3.9 | 2.45 | | | | 0.3 | | | | |

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot616-3_po

| Outline version | References | | | | European projection | Issue date |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT616-3 | | MO-220 | | | | ~~16-02-17~~ 16-07-14 |

**Fig 15. HVQFN24 package outline**

# 15. Revision history

**Table 19. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| LPC8N04 v.1.4 | 20180608 | Product data sheet | - | LPC8N04 v.1.3 |
| Modification: | • Updated Section 2 “Features and benefits”: Added text: OTA firmware update using Secondary Bootloader (SBL) library (See TN00040: LPC8N04: Encrypted Over the Air (OTA) Firmware update using NFC). OTA firmware update available on Boot ROM version 0.14.<br>• Updated Section 5 “Marking”. | | | |
| LPC8N04 v.1.3 | 20180301 | Product data sheet | - | LPC8N04 v.1.2 |
| Modification: | • Changed title to Cortex-M0+. | | | |
| LPC8N04 v.1.2 | 20180301 | Product data sheet | - | LPC8N04 v.1.1 |
| Modification: | • Added a remark to Section 8.4.1 “System power architecture”: When running without a battery, energy harvesting is limited to 2 MHz system clock. | | | |
| LPC8N04 v.1.1 | 20171211 | Product data sheet | - | LPC8N04 v.1.0 |
| Modification: | • Added text to Section 2 “Features and benefits”: Energy harvesting functionality to power the LPC8N04. | | | |
| LPC8N04 v.1.0 | 20171012 | Product data sheet | - | - |

# 18. Tables

# 19. Figures